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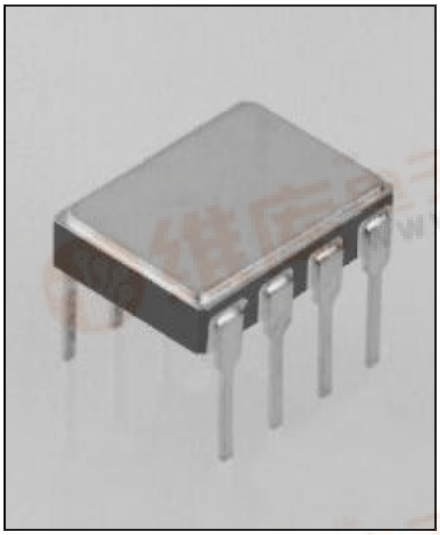
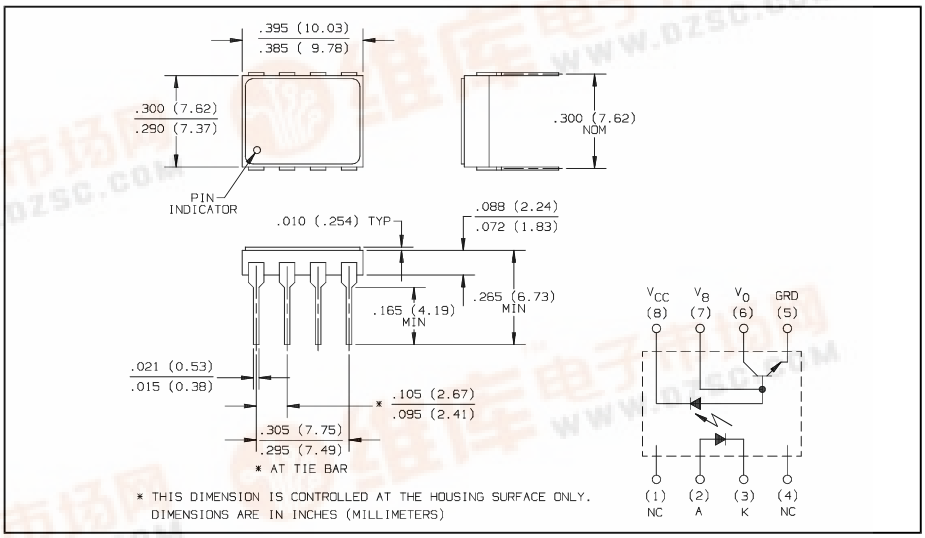
Product Bulletin HDC135
September 1996

High Speed Optocouplers
Types HDC135, HDC136, HDC135B, HDC136B





Features

- High speed
- TTL compatible
- High common mode transient immunity
- Wide bandwidth
- Open collector output

Description

Optek's HDC135 and HDC136 are high speed optocouplers, consisting of IR emitters and integrated photodetectors in hermetic side brazed dual-in-line 8 pin packages. Electrical characteristics are similar to the 6N135 and 6N136 optocouplers but with full military temperature range operation.

The HDC135B and HDC136B are high reliability optocouplers with 100% processing and Group Testing patterned after MIL-STD-883 Method 5004 and 5005 for class B.

Typical screening and lot acceptance tests are provided on page 13-4.

Minimum orders will apply to processed devices.

Absolute Maximum Ratings (No derating required up to 70° C)

Storage Temperature Range	-55° C to +150° C
Operating Temperature Range	-55° C to +125° C
Lead Soldering Temperature [1/16 inch (1.6 mm) from case for 10 seconds)	260° C
Average Input Current - I_F	25 mA(1)
Peak Output Current - I_F (50% duty cycle, 1 ms pulse width)	50 mA(2)
Peak Transient Input Current - I_F (≤ 1 µs pulse width, 300 pps)	1.0 A
Reverse Input Voltage - V_R	5.0 V
Input Power Dissipation	45 mW(3)
Average Output Current - I_O	8.0 mA
Peak Output Current	16.0 mA
Emitter-Base Reverse Voltage	5.0 V
Supply and Output Voltage - V_{CC}, V_O	-0.5 V to 15 V
Base Current - I_B	5.0 mA
Output Power Dissipation	100 mW(4)

Caution: This component is susceptible to damage from electrostatic discharge. Normal static prevention procedures should be used in handling.

Notes:
(1) Derate linearly above 70° C free-air temperature at a rate of 0.45 mA/° C.
(2) Derate linearly above 70° C free-air temperature at a rate of 0.9 mA/° C.
(3) Derate linearly above 70° C free-air temperature at a rate of 0.8 mW/° C.
(4) Derate linearly above 70° C free-air temperature at a rate of 1.8 mW/° C.
(5) CM_H is the maximum allowable dV/dt on the leading edge of a common mode pulse to assure that the output will not switch from high to low.
(6) CM_L is the maximum negative dV/dt allowable on the trailing edge of a common mode pulse to assure that the output will not switch from low to high.
(7) Test conditions represents 1 TTL unit load with 5.6 kΩ pull-up resistor.
(8) Test conditions represents 1 LSTTL unit load with a 6.1 kΩ pull-up resistor.
(9) Device considered a two-terminal device: pins 2 and 3 shorted together and pins 5, 6, 7 and 8 shorted together.

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Types HDC135, HDC136, HDC135B, HDC136B

Electrical Characteristics (Over recommended temperature T_A = -55° C to +125° C, unless otherwise noted)

SYMBOL	PARAMETER		MIN	TYP*	MAX	UNITS	TEST CONDITIONS
CTR	Current Transfer Ratio	HDC135 HDC136	7.0 19.0	19.0 25.0		% %	I_F = 16 mA, V_O = 0.40 V, V_{CC} = 4.5 V, T_A = 25° C
		HDC135 HDC136	5.0 15.0	15.0 23.0		% %	I_F = 16 mA, V_O = 0.50 V, V_{CC} = 4.5 V
V_{OL}	Logic Low Output Voltage	HDC135		0.100	0.40	V	I_F = 16 mA, I_O = 1.10 mA, V_{CC} = 4.5 V
		HDC136		0.100	0.40	V	I_F = 16 mA, I_O = 2.4 mA, V_{CC} = 4.5 V
I_{OH}	Logic High Output Current			3.0	500	nA	I_F = 0 mA, V_O = V_{CC} = 5.5 V, T_A = 25° C
				0.010	1.00	µA	I_F = 0 mA, V_O = V_{CC} = 15 V, T_A = 25° C
					50	µA	I_F = 0 mA, V_O = V_{CC} = 15 V
I_{CCL}	Logic Low Supply Current			40		µA	I_F = 16 mA, V_O = open, V_{CC} = 15 V
I_{CCH}	Logic High Supply Current			0.020	1.00	µA	I_F = 0 mA, V_O = open, V_{CC} = 15 V, T_A = 25° C
					2.0	µA	I_F = 0 mA, V_O = open, V_{CC} = 15 V
V_F	Input Forward Voltage			1.50	1.70	V	I_F = 16 mA, T_A = 25° C
$\frac{\Delta V_F}{\Delta T_A}$	Temperature Coefficient of Forward Voltage			-1.80		mV/° C	I_F = 16 mA
$\overline{BV_R}$	Input Reverse Breakdown Voltage		5.0			V	I_R = 10 µA, T_A = 25° C
C_{IN}	Input Capacitance			42		pF	f = 1 MHz, V_F = 0
I_{IO}	Input-Output Insulation Leakage Current				1.00	µA	45% Relative Humidity, t = 5 sec, V_{IO} = 1000 Vdc, T_A = 25° C (Note 9)
R_{IO}	Input-Output Resistance			10^{12}		Ω	V_{IO} = 500 Vdc (Note 9)
C_{IO}	Input-Output Capacitance			0.50		pF	f = 1 MHz (Note 9)
h_{FE}	Transistor DC Current Gain			150		—	V_O = 5 V, I_O = 3 mA
Switching Specification (T_A = 25° C) V_{CC} = 5.0 V, I_F = 16.0 mA unless otherwise noted							
t_{PHL}	Propagation Delay Time to Logic Low at Output	HDC135 HDC136		0.50 0.60	1.50 1.00	µs µs	R_L = 4.1 kΩ (Note 8) R_L = 1.90 kΩ (Note 7)
t_{PLH}	Propagation Delay Time to Logic High at Output	HDC135 HDC136		0.40 0.80	1.50 1.00	µs µs	R_L = 4.1 kΩ (Note 8) R_L = 1.90 kΩ (Note 7)
CM_H	Common Mode Transient Immunity at Logic High Level Output	HDC135 HDC136		1000 1000		V/µs V/µs	I_F = 0 mA, V_{CM} = 10 Vp-p, R_L = 4.1 kΩ (Notes 6,8) I_F = 0 mA, V_{CM} = 10 Vp-p, R_L = 1.90 kΩ (Notes 6,7)
CM_L	Common Mode Transient Immunity at Logic Low Level Output	HDC135 HDC136		-1000 -1000		V/µs V/µs	V_{CM} = 10 Vp-p, R_L = 4.1 kΩ, (Notes 5,8) V_{CM} = 10 Vp-p, R_L = 1.90 kΩ (Notes 5,7)

*

All typicals at T_A = 25° C and V_{CC} = 5 V, unless otherwise noted

HI-REL OPTO COMPONENTS

Optek reserves the right to make changes at any time in order to improve design and to supply the best product possible.