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Agilent HDMP-2689 Quad 2.125/1.0625 GBd Fibre Channel General Purpose SerDes

Data Sheet

Description

The HDMP-2689 SerDes chip transmits and receives high speed serial data over fiber optic or coaxial cable interfaces that conform to ANSI X3T11 Fibre Channel specification. It supports SerDes-only mode using a 10-bit data interface with optional 8B/10B encoding for fast backplane applications. The HDMP-2689 runs at 2.125 GBd or 1.0625 GBd data rates and provides parallel-to-serial and serial-to-parallel conversion on four independent channels contained in one package. An on-chip phase locked loop (PLL) synthesizes the high speed transmit clock from a low speed (106.25 MHz) reference. Each receiver's on-chip PLL synchronizes directly to the incoming data stream, providing clock and data recovery. Both the transmitter and receiver support differential I/O for fiber optic component interfaces, which minimizes crosstalk and maximizes signal integrity. Chip control and status are accessed via the Media Independent Interface (MII) defined in IEEE 802.3.

Features

- 1.0625GBd and 2.125 GBd serial data rates
- TX and RX data rates independently selectable for each channel
- Fibre Channel (T11) compatible
- High speed differential serial I/O with matched 50Ω impedance
- Supports Fibre Channel Protocols FC0
- Dual mode SerDes operation with 10-bit parallel data interface and optional 8B/10B encode/decode
- Standard comma recognition for positive (0011111xxx) and negative (1100000xxx) disparity
- Source-centered, double data rate clocking of receive parallel data for 1.0625 GBd and 2.125 GBd serial rates
- Source synchronous double data rate clocking of transmit parallel data for 2.125 GBd serial rate
- Source synchronous single data rate clocking of transmit parallel data for 1.0625 GBd serial rate
- MII management interface for chip control and status
- 1.8V core power supply, 2.5V power supply for SSTL_2 I/O
- Independent channel power-down for power savings
- SSTL_2 compliant parallel I/O and byte clocks
- Low transmit jitter
- Pre-emphasis on serial outputs controllable via the management interface
- Loss of signal detection
- AC-coupled differential LVPECL reference clock input
- Input equalization
- Boundary scan IEEE 1149.1 compliant
- SerDes self-test capability using PRBS or user-defined patterns
- Local internal loop back of TX serial data to RX serial data by channel
- 289-pin PBGA
- Testjet compliant

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Applications

- **Fibre Channel Arbitrated Loop**
- **Fast Serial Backplanes**

See Figure 1 for a diagram of typical applications.

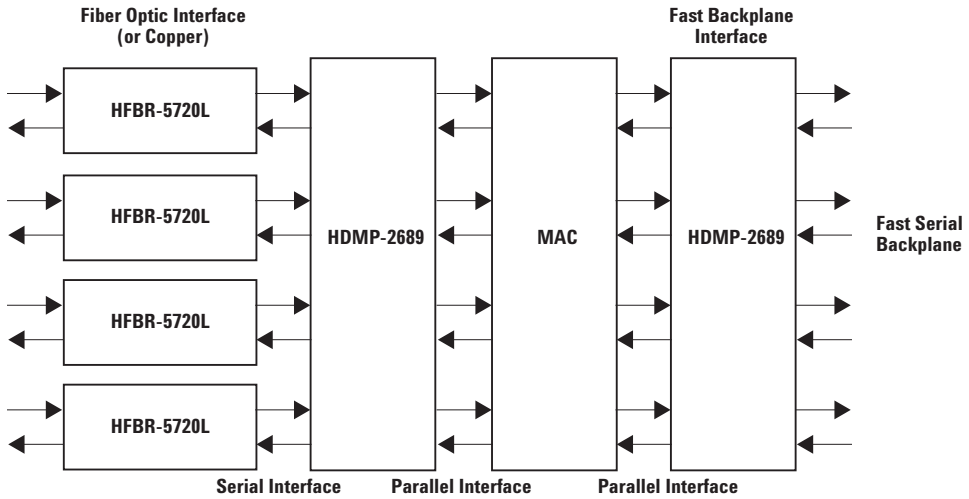


Figure 1. HDMP-2689 Typical Applications.

Functional Description

Transmitter Description

The HDMP-2689 transmitter contains four independent channels and a single TX PLL which generates the serial rate transmit clock for all of the channels. The data is optionally encoded in 8B/10B format and serialized at 1.0625 GBd (half rate) or 2.125 GBd (full rate). The high-speed outputs can be interfaced directly to copper cables or PCB traces for electrical transmission or to a separate fiber optic module for optical transmission. See Figure 2 for a block diagram.

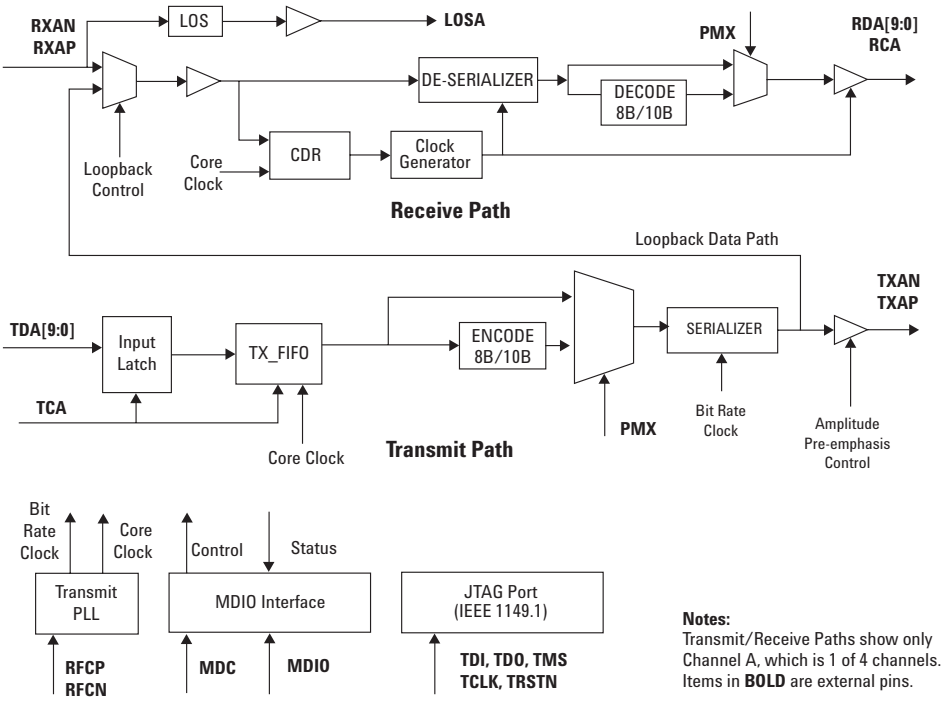


Figure 2. TX and RX Paths.

Reference Clock Input

The HDMP-2689 accepts a differential LVPECL reference clock input at 106.25 MHz (see Figure 3 for configuration). This reference clock is used by the TX PLL to acquire frequency lock and generate the base frequency of operation.

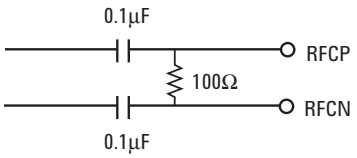


Figure 3. Reference Clock Input Configuration.

Data Input

The transmitter is designed to accept either of two formats of parallel input data:

- 9-bit data consisting of an 8-bit word plus a 1-bit K character flag (Z), encoded on chip with 8B/10B
- 10-bit data already encoded in a DC-balanced code (over a minimum length of 20 bits) such as 8B/10B

The PMX pin is set to select the data format. Depending on the format, the data may undergo encoding before serialization. See Table 1 for PMX encoding definitions and data processing.

Table 2 contains a summary of the data formats. Note that for the buffer mode (PMX=0), bit a, which corresponds to TDn9, is serialized first. For example, for K28.5 (0011111010), if the MAC's Out0 through Out9 bits correspond to 0011111010, then the HDMP-2689's TDA9 through TDA0 are connected to the MAC's Out0 through Out 9. The TDA9 bit is serialized first. Similarly on the RX side, the very first bit received is RDA9 (MSB) which is In0 for the MAC. See Figure 4 for MAC to HDMP-2689 connections. (Channel A, shown in the figure, is representative of all four channels.)

For codec mode, the MAC's Out0 through Out9 should be connected to TDA0 through TDA9. For example, if 1bc=01 1011 1101 is coming from the MAC for encoding, Out0 (assuming this is the LSB from the MAC) is 1, Out1 is 0 and so on. After encoding, the result is a comma, 0011111010 (or 1100000101), with the leading 00 (or 11) bits coming first on the serial output. The RX side behaves in a similar fashion. The parallel input data arrives on SSTL_2 inputs and is captured by data latches which are clocked by the local transmit clocks (TC[A-D]). The TX_FIFO phase aligns the data with the internal core clock.

8B/10B Encoding

The HDMP-2689 provides a global 8B/10B line coding option. The characters defined by this code ensure a DC balanced serial data stream, which enables clock recovery at the receiver. The 8B/10B code distinguishes D-characters, used for data transmission, from K-characters, used for control or protocol functions. A byte error code can be designated as the replacement data for an erroneous data word by programming bits 14 through 6 of management interface register 19.

Half Rate/Full Rate

The HDMP-2689 supports two transmit data rates as detailed in Table 3. The 10-bit wide parallel data is multiplexed into a 1.0625 GBd (half rate) or 2.125 GBd (full rate) serial data stream using internally generated high-speed clocks. The data bits are transmitted sequentially from TDn[9] to TDn[0] (bit ordering for buffer and codec modes is shown in Table 2). The output serial data rate is selected by programming bit 15 in management interface register 17.

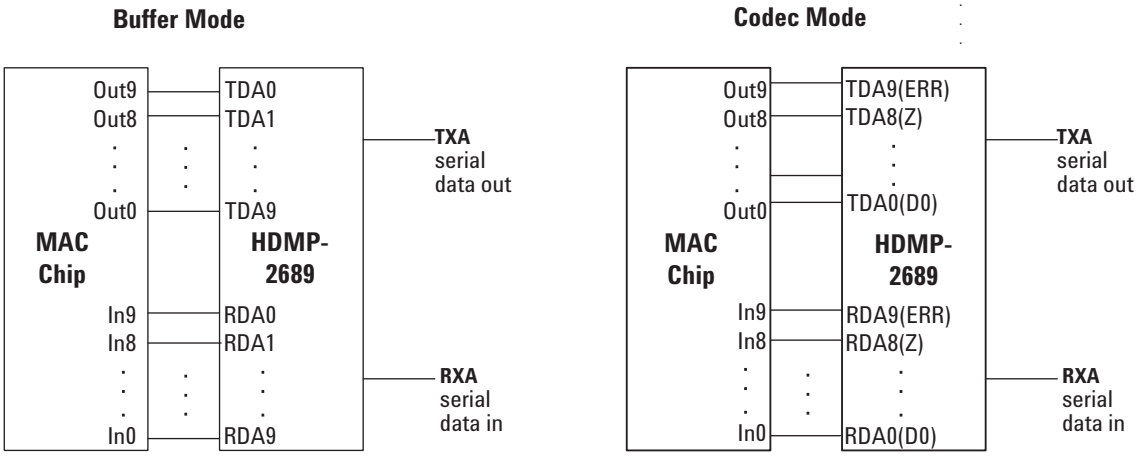


Figure 4. MAC to HDMP-2689 Interconnect.

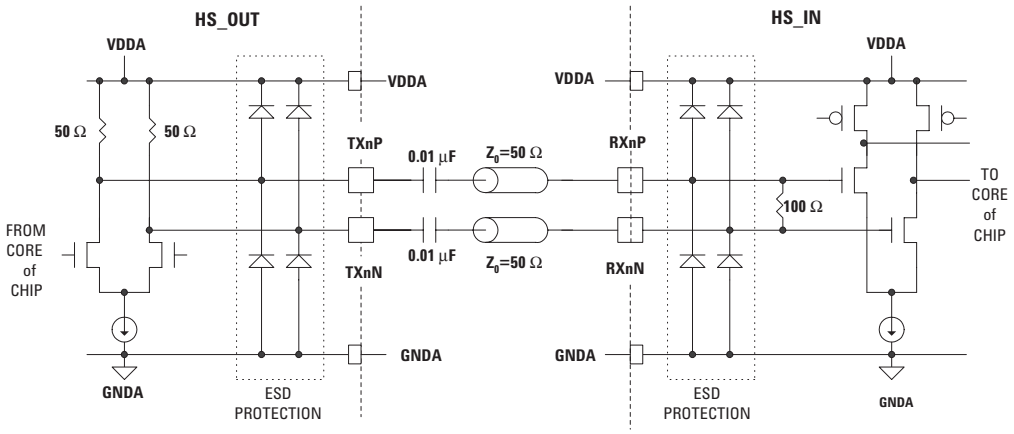
For half rate operation, the data is input in single data rate (SDR) mode. For SDR each parallel input data word is clocked in on the falling edge of the input transmit byte clock (TC[A-D]). The timing requirements are specified in Figure 9 Case A. For full rate operation, the data must be input in double data rate (DDR) mode, with one data word input on the rising edge of the input transmit byte clock (TC[A-D]) and the next word on the falling edge. Two data words are input every transmit byte clock cycle. The timing requirements for DDR operation are shown in Figure 9 Case B.

TC[A-D] always operates at 106.25 MHz.

The default settings for the HDMP-2689 are full rate operation and DDR.

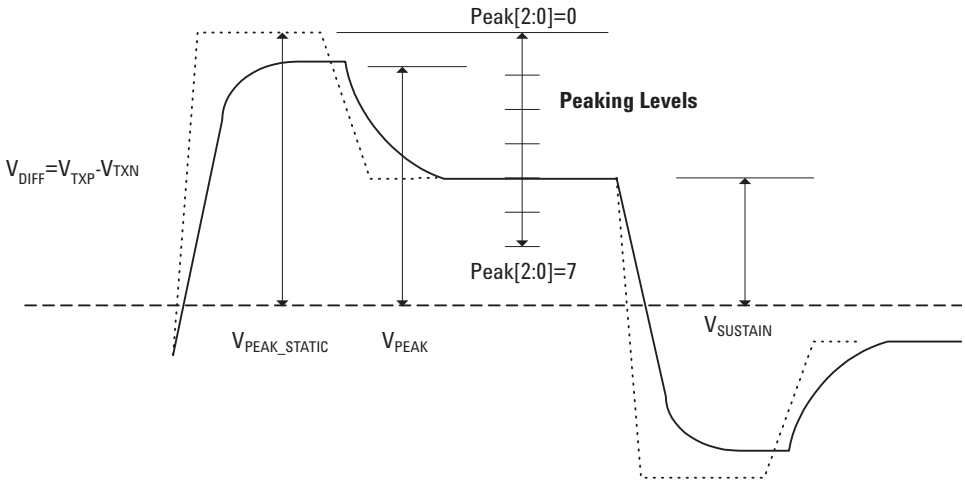
Serial Data Outputs

Through AC coupling, the high-speed outputs are capable of interfacing directly to copper cables or PCB traces for electrical transmission or to a separate fiber optic module for optical transmission (see Figure 5). These outputs include user-controllable skin-loss equalization and amplitude control to improve performance when driving copper lines. In normal operation, the serialized TDn[9:0] data is placed at TXnP/N. The output drivers provide for controllable pre-emphasis and amplitude settings by programming management interface register 26 (see Figure 6). If pre-emphasis is used, 0→1 and 1→0 transitions on TXnP/N have greater amplitude than 0→0 and 1→1 transitions. This increased amplitude counteracts the effects of skin loss and dispersion on long PCB transmission lines. The serial outputs can also be disabled through register 26.



Notes: HS_IN inputs should never be connected to ground as permanent damage to the device may result.
Capacitors may be placed at the sending or receiving end.

Figure 5. High Speed Input and Output Configurations.



Note: The peaked value at the transition edge does not reach to V_{PEAK_STATIC} value because of the reflection between driver and package. The static value can be measured as the final value of a long (longer than 2 bits) 1 or 0 pulse with zero peaking.

Figure 6. High Speed Output Pre-Emphasis.

Receiver Description

The HDMP-2689 receiver contains four independent channels, each with its own input amplifier with equalization, clock recovery PLL, deserializer, comma detection and byte clock generation. Depending on the PMX mode, the data may also pass through an 8B/10B decoder.

High Speed Input

In normal operation, serial data is accepted at RXnP/N and converted into parallel data to drive RDn[9:0]. See Figure 5 for the input configuration. In parallel loopback mode, the internal serial output signal from the transmitter section is used to generate RDn[9:0]. Loopback is discussed in more detail in the section on Test.

Receiver Loss of Signal

When the peak-to-peak differential amplitude at the RXnP/N input is too small, LOSn is set to logic 1. When the signal at RXnP/N is a valid amplitude, LOSn is set to logic 0.

If RXnP/N ≥ 300 mV peak-to-peak differential,
LOSn = logic 0

If 150 mV < RXnP/N < 300 mV peak-to-peak differential,
LOSn is undefined

If RXnP/N ≤ 150 mV peak-to-peak differential,
LOSn = logic 1

Optionally, through MII register 17, LOSn can also be forced to logic 1 if the receiver PLL is not locked.

RX PLL/Clock Recovery

The receiver frequency and phase locks onto the incoming serial data stream and recovers the bit clock. The RX PLL locks onto the input data by frequency locking onto the 106.25 MHz LVPECL reference clock and then phase locking onto the selected input data stream. The received clock locks to the incoming data or free runs at the selected frequency in the absence of incoming data. An internal signal detection circuit monitors the presence of the input and invokes phase detection as the data stream appears. Once bit locked, the receiver generates the high-speed sampling clock used to deserialize the data.

Byte Sync and Comma Detect

As the 10-bit parallel data is recovered from the high-speed serial bit stream, the first seven bits of the K28.5+ positive disparity comma character (0011111xxx) and of the K28.5- negative disparity comma character (1100000xxx) are detected. The proper parallel data edge is selected out of the bit stream so that the next comma character starts at RDn[9] in buffer mode. When a comma character is detected and realignment of the receive byte clock is necessary, the clocks are stretched (never slivered) to the next correct alignment position. The recovered clock will be aligned by the start of the next four-byte ordered set after K28.5+ or K28.5- is detected. By default, in buffer mode, the start of the next ordered set will be aligned with the falling edge of RCn. In codec mode (PMX=1), by default the RCn clock is not realigned, and the comma may appear at either edge. The default alignments may be changed by programming MII register 17. Unless comma edge alignment is disabled in MII register 17, comma characters must not be transmitted in consecutive bytes so that the receive byte clocks may maintain their proper recovered frequencies. Furthermore, RX byte align should be disabled (using MII register 24) if PRBS data is being received.

SSTL_2 Outputs

As discussed for the transmitter parallel inputs, the bit ordering is different for buffer and codec modes. See Figure 4 and earlier Data Input section for additional details.

The HDMP-2689 presents the 10-bit parallel recovered data (RDn[9:0]), properly aligned to the receive byte clock (RCn) as shown in Figure 11 and Table 5, as single-ended SSTL_2 compliant signals. The HDMP-2689 expects SSTL_2 compatible signals at the TDn[9:0] and TCn pins. See Figure 7 for a simplified schematic of the input and output drivers, and Figure 8 for the recommended termination configuration. For proper operation of the terminated SSTL_2 drivers, register 23 must be configured as described in Management Interface Registers, page 27. (Set register 23 to 0x1218). For best results use a low inductance VTERM plane to terminate the 50 Ω resistors close to the HDMP-2689 TX inputs. In addition, decouple the VTERM plane with 0.1 µF local to each 10-bit channel to reduce simultaneously switching output (SSO) noise on the inputs. The HDMP-2689 works with MAC devices whose VDDQ voltage is nominally 2.5 V. In addition, the HDMP-2689 provides a VREF output pin which may be used at the protocol IC in order to differentially detect a high or a low on RDn[9:0]. Alternatively, this voltage may be generated on the PCB using a resistor divider from VDDQ while ignoring the VREF output of the HDMP-2689.

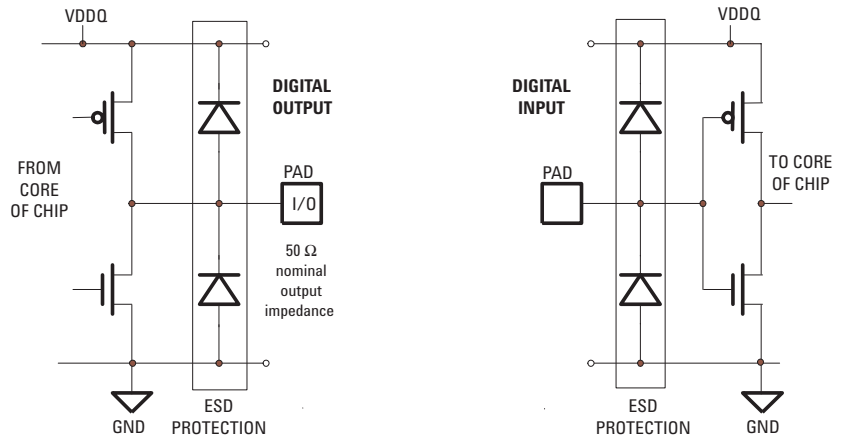


Figure 7. Simplified Schematic of SSTL_2 Input and Output Drivers.

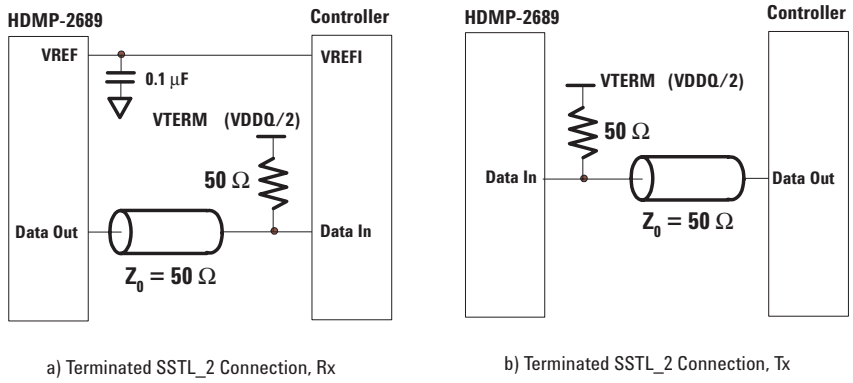


Figure 8. SSTL_2 I/O Terminations.

Data Output and Clocking Modes

Table 5 describes the receive parallel interface clocking. In both half (1.0625 GBd serial) and full (2.125 GBd serial) rate operation, the data is always presented as DDR, double data rate (See Figure 11, Cases A and B). In addition, the output clock is always source centered (SC), so the clock changes in the middle of the data period. Note that bit a, the first serial bit in a 10-bit word, corresponds to RDn9 (see Table 2).

Configuration and Reset

The HDMP-2689 is configured by a set of registers that can be accessed through the standard MII management interface defined in IEEE 802.3 clause 22. This interface is used by a management entity to control and gather status from the chip. It is a two-wire interface made up of a management data input/output signal (MDIO) and a management data clock (MDC). Figure 15 shows the relationship between MDIO and MDC. Figure 16 and Figure 17 present a more detailed description of MDIO timing. Table 8 presents the format of a management frame (for more information, refer to IEEE 802.3). A management frame consists of a minimum 32-bit preamble, a start of frame indication, an operation code, a PHY address, a register address, turnaround bits, data bits, and an idle. The order of bit transmission is left to right as shown in Table 8. MDIO timing is detailed in Table 9.

The three most significant bits of the PHY address are made up of the hard-wired address of the HDMP-2689. The two least significant bits represent the channel referenced in the frame. Two bits are sufficient to encode IDs for the four channels on the chip.

The standard management interface allows for 32 16-bit registers. The HDMP-2689 supports a subset of these registers. Management Interface Registers, pages 26–28, show the standard register definitions and specify which ones are supported in the HDMP-2689. Because the HDMP-2689 has four physical channels that operate independently, some of the registers are replicated four times, one for each channel. Other registers are common to all four channels, i.e. their bit values apply to all the channels. Still other registers are shared between the four channels, i.e. individual bits within a register apply to individual channels. The replicated registers are accessed using a PHY address made up of the three-bit chip ID and the appropriate two-bit channel ID (00, 01, 10, or 11). Common and shared registers are accessed using the chip ID and the 00 channel ID. Attempting to access common registers other than through channel A (00) must be avoided as it results in undefined behavior. The specific configuration and status information that can be set or read from HDMP-2689 is presented in the section titled Management Interface Registers. This section defines the complete assignment of management registers and specifies which registers are common to the four channels.

Reset is initiated externally with the assertion of the RSTN pin. Before asserting the RSTN pin, the power supply to the chip and the reference clock (RFCP/N) must be stable for at least 20 µs. The RSTN pin must be held low for at least 100 ns. After reset is de-asserted, 500 µs must elapse before initiating MDIO transactions (see Figure 13). Note that the transmit byte clocks (TCn) should be running and stable when reset is released to minimize the variation in transmit latency.

Power Management

The HDMP-2689 incorporates the ability to power down any channel which is unused. Both the channel and the associated output driver should be disabled by programming the unused channel's register 24, bit 0 and register 26, bit 7 both to logic 0. Additionally, the HDMP-2689 does not require a particular power turn-on sequence.

Power Supply Decoupling

Recommended power supply filtering and placement of decoupling capacitors for the HDMP-2689 are shown in Figure 22 and Figure 23.

Test

The HDMP-2689 has several features to facilitate testing, including boundary scan, SerDes self-test, and loopback for link debugging. Boundary scan is implemented according to the IEEE 1149.1 standard. The instructions listed in Table 7 are supported. The HDMP-2689 also provides self-test capabilities with user-entered patterns or on-chip generation of pseudo-random bit streams (PRBS $2^7 - 1$). The patterns can be looped back either internally or externally from the transmit serializer to the receive deserializer and are verified within the chip. These self-test mechanisms are initiated and the error status reported through the MII management interface. To run a self-test, first select the pattern or set of patterns, then configure the loopback and check the results. Once enabled, the test pattern is sent continuously. To select a user-defined pattern:

- Disable comma alignment by programming bit 1 of register 24 to logic 0.
- Program the pattern (any pattern except all 0's or all 1's) into bits 9 through 0 of register 25.
- To alternate the user pattern with its inverse, program bit 11 of register 25 to logic 1.
- Program bit 10 of register 25 to a logic 1 to enable the user register pattern to be sent.

To select PRBS data:

- Disable comma alignment by programming bit 1 of register 24 to logic 0.
- Program a non-zero seed for the pattern generator into bits 9 through 0 of register 25.
- To send the PRBS pattern inverted, program bit 11 of register 25 to logic 1.
- Program bit 12 of register 25 to a logic one to enable the PRBS pattern to be sent.
- To see the recovered PRBS data on the parallel interface, comma edge alignment should be disabled by programming bit 13 of register 17 to logic 0.

To run the self-test with either external or internal loopback:

- Set up either a user-defined pattern or PRBS data as outlined above.
- To run with internal loopback, program bit 13 of register 25 to logic 1.
- To run with external loopback, connect the high-speed output of the channel being tested (TXAP/N, TXBP/N, TXCP/N, TXDP/N) back to its high speed input (RXAP/N, RXBP/N, RXCP/N, RXDP/N). Bit 13 of register 25 must be logic 0 (default value after reset).
- Program bit 14 of register 25 to logic 0 if it is not already zero (default value after a reset). Bit 12 of register 27 (pattern failure detect) and bit 11 of register 27 (test run complete) should both now be logic 0.
- Program bit 14 of register 25 (pattern error monitor enable) to logic 1. This starts the pattern checking process. For a PRBS pattern 2 9 bytes are checked before the test is considered complete.
- Monitor bit 11 of register 27 to determine if a sufficient number of cycles have elapsed for test completion. When this bit is logic 1, bit 12 of register 27 signals pass (logic 0) or fail (logic 1).

To allow link debugging:

- Configure the HDMP-2689 for internal loopback (data provided at the parallel input is looped back to the parallel output after traversing the chip) via management interface register 25 bit 13. Note that for internal loopback in codec mode the receiver sees a loss of signal and error bit 9 (see Table 2) is set, unless the high speed inputs (ignored for internal loopback) are being driven.

Table 1. PMX Encoding Definitions.

PMX	Mode	Description
0	Buffer	TX: Inputs are phase adjusted to transmit clock and serialized MSB (a) first. RX: Serial data is byte aligned and presented with first bit (a) as MSB
1	Codec	TX: Inputs are phase adjusted, 8B/10B encoded, and serialized. RX: Serial data is byte aligned and 8B/10B decoded

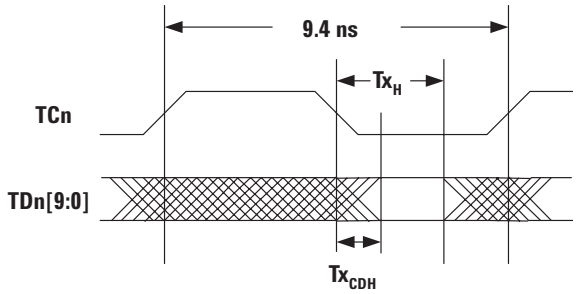
Table 2. Data Formats (TDA/RDA is representative of all Transmit and Receive Data Ports).

Pin	PMX 0 Buffer	PMX 1 Codec
TDA9/RDA9	a	ERR (RX_LOS or decoding error)
TDA8/RDA8	b	Z
TDA7/RDA7	c	D7
TDA6/RDA6	d	D6
TDA5/RDA5	e	D5
TDA4/RDA4	i	D4
TDA3/RDA3	f	D3
TDA2/RDA2	g	D2
TDA1/RDA1	h	D1
TDA0/RDA0	j	D0

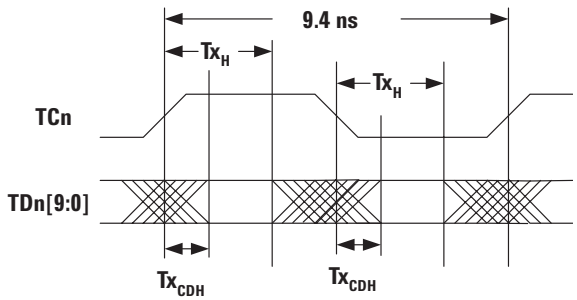
Note: See Figure 4 for a connection diagram.

Table 3. Transmitter Data Rate.

Management Register 17 Input Setting Case	Full/Half	TXnP/N Rate (GBd)	TCn Rate (MHz)
A	0	1.0625	106.25
B	1	2.125	106.25



Case A. Tx Half Rate SDR Timing



Case B. Tx Full Rate DDR Timing

Test Conditions: $V_{IH} = V_{DDQ}$, V_{IL} = GND

Figure 9. Transmitter Timing Diagram.

Table 4. HDMP-2689 Transmitter Section Timing Characteristics,
$T_C = 0°C$ to $T_C = 85°C$, $V_{DDQ} = 2.3$ to 2.7 V, $V_{DD} = 1.7$ to 1.9 V, $V_{DDA} = 1.7$ to 1.9 V

Symbol	Parameters	Units	Min	Typ	Max
1G					
Tx_{CDS}[1,2]	Clock to data skew time; the data must be stable by T_{CDS} after the clock edge to guarantee correct clocking of the data	ps			300
Tx_H[2]	Hold time; the time after the clock edge until which the data must remain stable to guarantee correct clocking of the data	ps	2000		
t_TXlat_buffer[3]	Transmitter latency; the time between the latching edge of the transmit byte clock TCn and the leading edge of the first transmitted serial output bit in buffer mode	ns bits		80 85	
t_TXlat_codec[3]	Transmitter latency; the time between the leading edge of the transmit byte clock TCn and the leading edge of the first transmitted serial output bit in codec mode	ns bits		90 95.5	
2G					
Tx_{CDS} [1,2]	Clock to data skew time; the data must be stable by T_{CDS} after the clock edge to guarantee correct clocking of the data	ps			300
Tx_H[2]	Hold time; the time after the clock edge until which the data must remain stable to guarantee correct clocking of the data	ps	2000		
t_TXlat_buffer[3]	Transmitter latency; the time between the latching edge of the transmit byte clock TCn and the leading edge of the first transmitted serial output bit in buffer mode	ns bits		65 138	
t_TXlat_codec[3]	Transmitter latency; the time between the leading edge of the transmit byte clock TCn and the leading edge of the first transmitted serial output bit in codec mode	ns bits		70 149	

Notes:
1. This clock-to-data skew time is equivalent to –300ps setup time.
2. Measurement conditions were $V_{IH} = V_{DDQ}$, V_{IL} = GND.
3. Due to the FIFO which aligns the phase of the internal chip clock with the transmit byte clock (TCn) and the asynchronous nature of the chip reset, the typical latency varies; a maximum of the typical range is given.

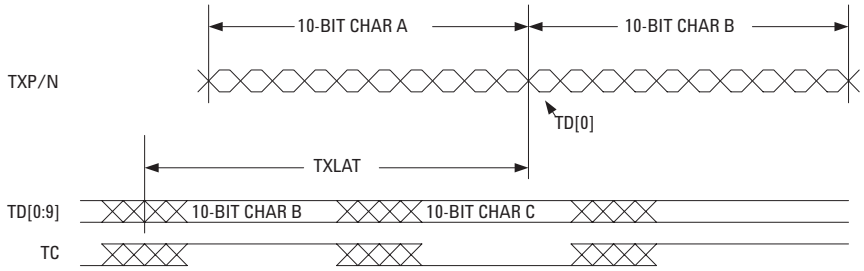
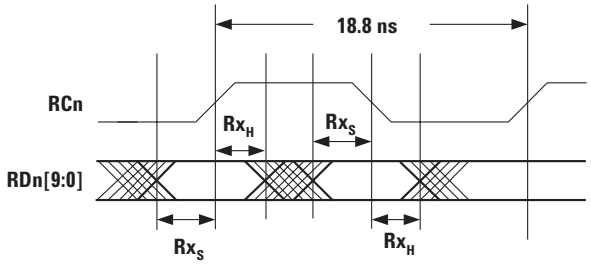


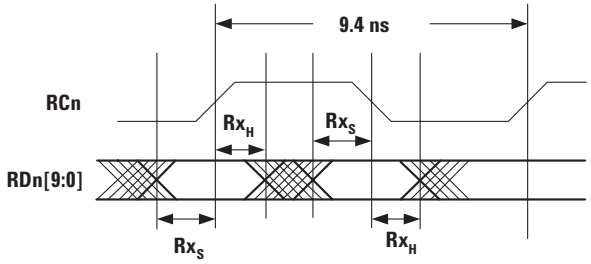
Figure 10. Transmitter Latency.

Table 5. Receiver Data Rate.

Management Register 17 Input Setting Case	Full/Half	RXnP/N Rate (GBd)	RCn Rate (MHz)
A	0	1.0625	53.125
B	1	2.125	106.25



Case A. Rx Half Rate DDR Timing



Case B. Rx Full Rate DDR Timing

Test Conditions: $V_{IH} = V_{DDQ}$, V_{IL} = GND

Figure 11. Receiver Timing Diagram.

HDMP-2689 Receiver Section Timing Characteristics,
T_C = 0°C to T_C = 85°C, V_{DDQ} = 2.3 to 2.7 V, V_{DD} = 1.7 to 1.9 V, V_{DDA} = 1.7 to 1.9 V

Symbol	Parameters	Units	Min	Typ	Max
PWreset	Width of reset pulse	ns	100		
f lockRX	The time that the RX PLL takes to frequency lock to the data after reset	µs			500
B_sync_lock	Bit Sync time after f lockRX	bits			2500
B_sync_rate	Bit Sync time after rate switch	µs			100
1G					
RX_S[1]	Setup time: the time before the clock edge that the data will be stable	ps	2700		
RX_H[1]	Hold time; the time after the clock edge until which the data will remain stable	ps	1500		
t_RXlat_buffer	Receiver latency; the timing between the leading edge of the first received serial bit of a parallel data word and the leading edge of the corresponding parallel output word in buffer mode	ns bits		50 53	
t_RXlat_codec	Receiver latency; the timing between the leading edge of the first received serial bit of a parallel data word and the leading edge of the corresponding parallel output word in codec mode	ns bits		60 64	
2G					
RX_S[1]	Setup time: the time before the clock edge that the data will be stable	ps	1200		
RX_H[1]	Hold time; the time after the clock edge until which the data will remain stable	ps	1400		
t_RXlat_buffer	Receiver latency; the timing between the leading edge of the first received serial bit of a parallel data word and the leading edge of the corresponding parallel output word in buffer mode	ns bits		30 64	
t_RXlat_codec	Receiver latency; the timing between the leading edge of the first received serial bit of a parallel data word and the leading edge of the corresponding parallel output word in codec mode	ns bits		35 75	

Notes:
1. Tested under load conditions described in Figure 12, with $V_{IH} = V_{REF} + 0.18$ and $V_{IL} = V_{REF} - 0.18$.

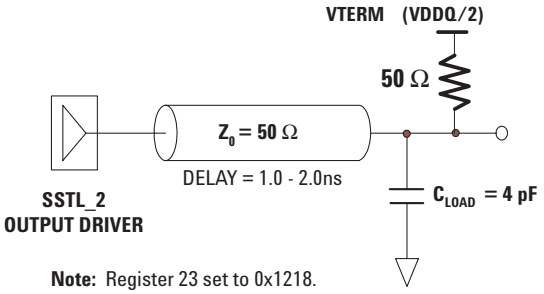


Figure 12. SSTL_2 Output Test Conditions.

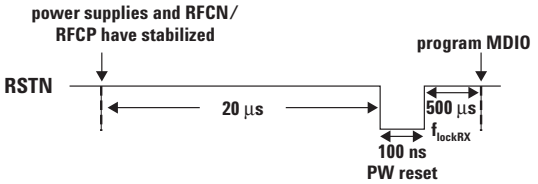


Figure 13. Externally Applied Reset (not to scale).

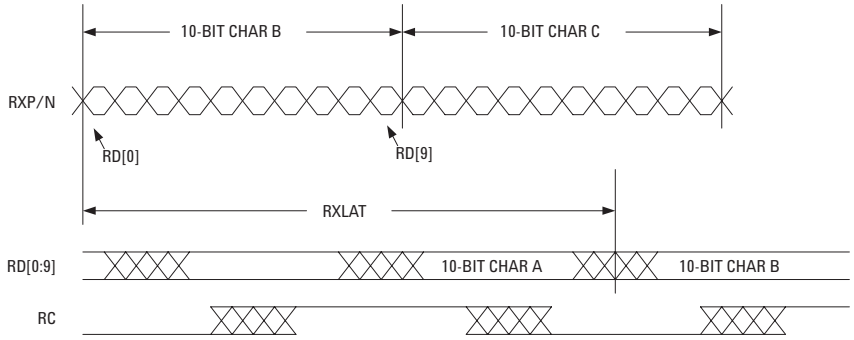


Figure 14. Receiver Latency.

Table 7. IEEE JTAG 1149.1 Instructions.

Instruction	Opcode	Description
EXTEST	00000_00000	Causes boundary JTAG registers to capture their inputs, shift, and output to pads.
SAMPLE	00000_00010	Causes boundary JTAG registers to capture their inputs.
CLAMP	00000_00100	Causes boundary JTAG registers to output their values to pads.
HIGHZ	00000_01000	Causes pads to be tri-stated.
BYPASS	11111_11111	Connects the bypass register between TDI and TDO.

Table 8. Format of a Management Frame.

	Pr	St	Op	PhyAdd	RegAdd	TA	Data	IDLE
Read	11...1	01	10	aaaaa	rrrrr	Z0	DDDDDDDDDDDDDDDD	Z
Write	11...1	01	01	aaaaa	rrrrr	10	DDDDDDDDDDDDDDDD	Z

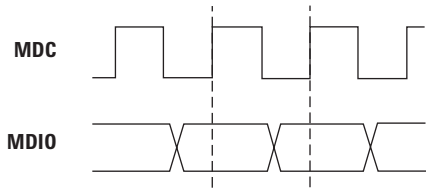


Figure 15. MDIO and MDC Timing.

Table 9. MDIO Timing Characteristics,

T_C = 0°C to T_C = 85°C, V_{DDQ} = 2.3 to 2.7 V, V_{DD} = 1.7 to 1.9 V, V_{DDA} = 1.7 to 1.9 V

Symbol	Parameters	Units	Min	Typ	Max
Driving					
T_{DELAY}	MDC rising edge to MDIO data true or MDIO released	ns	0		300
T_{MDC}	MDC frequency	MHz			2.5
Receiving					
T_{SU}	Set up time: MDIO to MDC rising edge	ns			10
T_H	Hold time: MDC rising edge to MDIO changing	ns			10

Note: For more information, see the IEEE 802.3 part 3 22.3.4, "MDIO timing relationship to MDC."

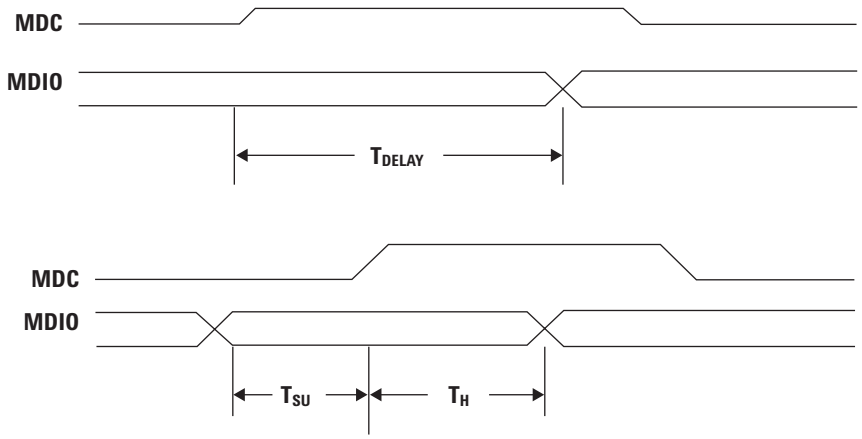
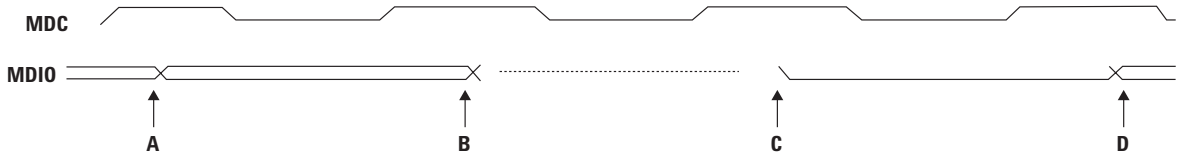


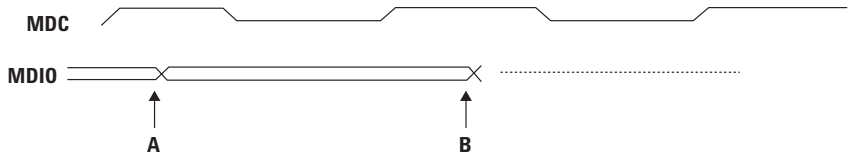
Figure 16. MDIO Timing, Driving and Receiving.



A	Station drives lsb (least significant bit) of regular address on the MDIO line
B	Station releases the MDIO line
C	Unit (HDMP-2689) drives a low on the MDIO line
D	Unit (HDMP-2689) drives bit 15 of the read register data

Note: All MDIO changes are triggered from the rising edge of MDC.

MDIO Timing, Turn Around (TA) Cycles During a Read.



A	Unit (HDMP-2689) drives lsb (least significant bit) of read register data
B	Unit (HDMP-2689) releases the MDIO line

Note: For more information, see the IEEE 802.3 Part 3 22.2.4.5. "Management Frame Structure."

MDIO Timing, Last Bit of Read Register Data, Bus Released by the HDMP-2689.

Figure 17. MDIO Timing Diagrams.

Table 10. HDMP-2689 Absolute Maximum Ratings.

Sustained operation at or beyond any of these conditions may result in long-term reliability degradation or permanent damage, and is not recommended.

Symbol	Parameters	Units	Min	Max
V_{DDQ}	I/O supply voltage	V	-0.5	4.0
V_{DD}	Supply voltage – digital core	V	-0.5	3.0
V_{DDA}	Analog supply voltage	V	-0.5	3.0
T_{STG}	Storage temperature (not biased)	°C	-55	125
T_C	Case temperature, measured at top center of the package	°C	0	95
T_J	Junction temperature	°C	0	110
V_{INHS}	High speed input voltage (single-ended)	V	-0.5	V_{DDA} + 0.6
$V_{INLVPECL}$	LVPECL input voltage (reference clock RFCP/N) (single-ended)	V	-0.5	V_{DDA} + 0.6
V_{INSSTL}	SSTL_2 input voltage	V	-0.5	V_{DDQ} + 0.8
ESD	Electrostatic Discharge, Class 1	V	-1000	1000

Table 11. Recommended Operating Conditions.

Symbol	Parameters	Units	Min	Typ	Max
V_{DDQ}	I/O supply voltage	V	2.3	2.5	2.7
V_{DD}	Supply voltage – digital core	V	1.7	1.8	1.9
V_{DDA}	Analog supply voltage	V	1.7	1.8	1.9
T_C	Case temperature, measured at top center of the package	^{0}C	0	25	85

Table 12. Guaranteed Operating Rates.

T_C = 0°C to T_C = 85°C, V_{DDQ} = 2.3 to 2.7 V, V_{DD} = 1.7 to 1.9 V, V_{DDA} = 1.7 to 1.9 V

Parallel Clock Rate (MHz)		Serial Baud Rate (GBd)		Serial Baud Rate (GBd)	
Min	Max	Min	Max	Min	Max
106.2	106.3	1.062	1.063	2.124	2.126

Table 13. Clock Specifications.

T_C = 0°C to T_C = 85°C, V_{DDQ} = 2.3 to 2.7 V, V_{DD} = 1.7 to 1.9 V, V_{DDA} = 1.7 to 1.9 V

Symbol	Parameters	Units	Min	Typ	Max
f	Reference Clock Nominal Frequency (RFCP/N)	MHz		106.25	
Symm[RFCP, RFCN]	Reference Clock Duty Cycle	%	40		60
F_{TOL_full}	Recovered Clock (RCn) to Reference Clock RFCP/N frequency tolerance	ppm	-100		100
F_{TOL_half}	Recovered Clock (RCn) to half the Reference Clock RFCP/N frequency tolerance	ppm	-100		100
Symm[RCn]	Recovered Clock Duty Cycle	%	40		60
f_{TCn}	Transmit Byte Clock Nominal Frequency	MHz		106.25	
Symm[TCn]	Transmit Byte Clock Duty Cycle	%	40		60

Note: Transmit Clock and Reference Clock must be from the same frequency source.

Table 14. HDMP-2689 Power Dissipation.

T_C = 0°C to T_C = 85°C, V_{DDQ} = 2.3 to 2.7 V, V_{DD} = 1.7 to 1.9 V, V_{DDA} = 1.7 to 1.9 V

Symbol	Parameters	Units	Min	Typ	Max
I_{VDDA} [1]	V_{DDA} current supply	mA		500	590
I_{VDDQ} [1]	V_{DDQ} current supply	mA		210	335
I_{VDD} [1]	V_{DD} current supply	mA		175	230
P_D	SerDes total power dissipation	W		1.7	2.5

Note:
1. Measurement conditions: full rate and half rate, random data. Maximum value covers both terminated and unterminated conditions.

Table 15. SSTL_2 I/O Operating Conditions.

T_C = 0°C to T_C = 85°C, V_{DDQ} = 2.3 to 2.7 V, V_{DD} = 1.7 to 1.9 V, V_{DDA} = 1.7 to 1.9 V

Symbol	Parameters	Units	Min	Typ	Max
V_{DDQ} [1]	Supply Voltage used to derive the SSTL_2 input reference voltage	V	2.3	2.5	2.7
$V_{IH\ (DC)}$	Input High voltage	V	V_{REF} + 0.18		V_{DDQ} + 0.3
$V_{IL(DC)}$	Input Low voltage	V	- 0.3		V_{REF} – 0.18
$V_{IH\ (AC)}$	Input High voltage	V	V_{REF} + 0.35		V_{DDQ} + 0.3
$V_{IL(AC)}$	Input Low voltage	V	- 0.3		V_{REF} – 0.35
V_{REF}	SSTL_2 Output reference voltage	V	1.15	1.25	1.35
V_{TERM}	Termination voltage	V	V_{REF} - 0.04	V_{REF}	V_{REF} + 0.04
V_{OH} [2]	Output High voltage	V	V_{TERM} + 0.38		
V_{OL} [2]	Output Low voltage	V			V_{TERM} – 0.38

Notes:
1. V_{DDQ} is the MAC device I/O supply voltage.
2. See Figure 12 for measurement conditions.

Table 16. HDMP-2689 CMOS I/O Operating Conditions.

T_C = 0°C to T_C = 85°C, V_{DDQ} = 2.3 to 2.7 V, V_{DD} = 1.7 to 1.9 V, V_{DDA} = 1.7 to 1.9 V, VDDQ is the FC-1MAC device I/O supply voltage.

Symbol	Parameters	Units	Min	Typ	Max
V_{IH}	Input High voltage	V	0.7 x V_{DDQ}		V_{DDQ}
V_{IL}	Input Low voltage	V	GND		0.3 x V_{DDQ}
V_{OH}	Output High voltage	V	V_{DDQ} – 0.1		
V_{OL}	Output Low voltage	V	GND		0.4

Table 17. HDMP-2689 AC Electrical Specifications.

$T_C = 0°C$ to $T_C = 85°C$, $V_{DDQ} = 2.3$ to 2.7 V, $V_{DD} = 1.7$ to 1.9 V, $V_{DDA} = 1.7$ to 1.9 V

Symbol	Parameters	Units	Min	Typ	Max
$t_{r,\ RFCP/N}$	RFCP/N LVPECL input rise time, $V_{IL,\ LVPECL}$ to $V_{IH,\ LVPECL}$	ns		1.5	
$t_{f,RFCP/N}$	RFCP/N LVPECL input fall time, $V_{IH,\ LVPECL}$ to $V_{IL,\ LVPECL}$	ns		1.5	
$t_{rd,\ HS_OUT}$ [1, 5]	HS_OUT differential rise time, 20% to 80%	ps		150	
$t_{fd,\ HS_OUT}$ [1, 5]	HS_OUT differential fall time, 80% to 20%	ps		150	
$t_{r,SSTL}$ [2,3]	SSTL output rise time, $V_{OL,\ SSTL}$ to $V_{OH,\ SSTL}$	ns			2.3
$t_{f,SSTL}$ [2,3]	SSTL output fall time, $V_{OH,\ SSTL}$ to $V_{OL,\ SSTL}$	ns			1.5
V_{IP,HS_IN} [4]	HS_IN input pk-pk differential voltage	V	0.3		1.6
V_{PK,HS_OUT} [1, 5]	HS_OUT output pk-pk differential voltage, (Z_0= 50Ω)[1]	V	725	880	1050
$V_{Sustain,HS_OUT}$ [1. 5]	HS_OUT output sustain level differential voltage, (Z_0= 50Ω)[1]	V	675	830	1000
$V_{IP,\ LVPECL}$	RFCP, RFCN input swing (single ended)	V	200		V_{DDA}

Notes:
1. Measured with 2 pF capacitive load.
2. See Figure 12 for test conditions.
3. SSTL_2 AC Input Signals meet JEDEC Standard No. JESD8-9A test conditions (minimum slew rate 1.0V/ns). See JEDEC Table 3.
4. Note LOS pin description.
5. Measured at default settings, maximum amplitude and medium peaking (11111011).

Table 18. HDMP-2689 Transmitter Section Output Jitter Characteristics.

$T_C = 0°C$ to $T_C = 85°C$, $V_{DDQ} = 2.3$ to 2.7 V, $V_{DD} = 1.7$ to 1.9 V, $V_{DDA} = 1.7$ to 1.9 V

Symbol	Parameters	Units	Min	Typ	Max
RJ[1]	Random Jitter at TXnP/N (1s deviation of 50% crossing point)	ps		4	
DJ[2]	Deterministic Jitter at TXnP/N (peak to peak), K28.5+/K28.5- pattern	ps		10	
DJ[3]	Deterministic Jitter at TXnP/N (peak to peak), CRPAT pattern	ps		15	
TJ	Total Jitter (TJ=DJ+14*RJ) (K28.5+/K28.5- pattern)	ps		66	
J	Jitter Tolerance		Fibre Channel compliant		

Notes:
1. Defined by Fibre Channel specifications X3.230 – 1994 FC-PH, Annex A section A4.4 (oscilloscope method) and tested using setup shown in Figure 20.
2. Defined by Fibre Channel specifications X3.230 – 1994 FC-PH, Annex A section A4.4 and tested using the set up shown in Figure 20.
3. Defined by Fibre Channel Technical Report "Methodologies for Jitter specifications," Annex B, and tested using the set up shown in Figure 20.

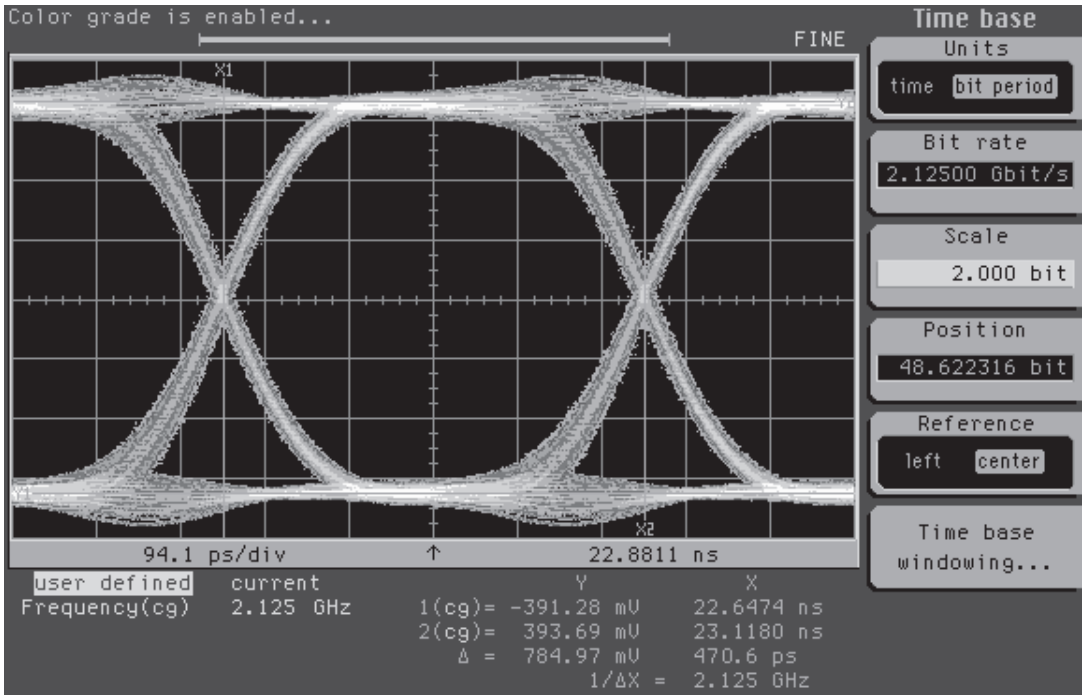


Figure 18. Serial Output Eye Diagram.

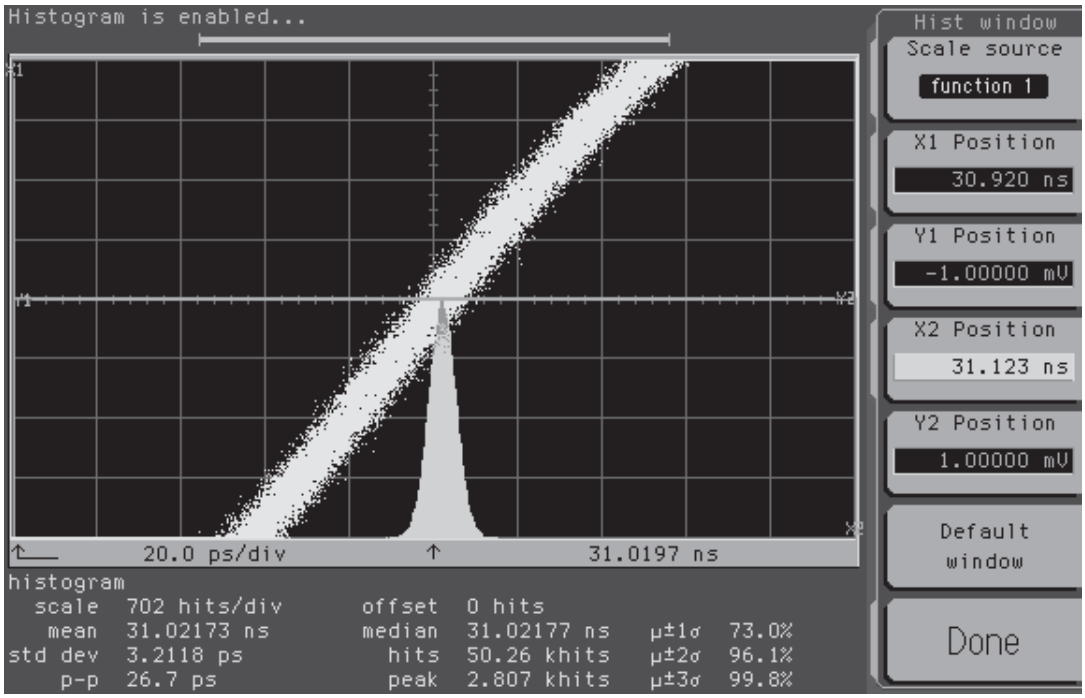


Figure 19. Serial Output Random Jitter with TX pre-emphasis off.

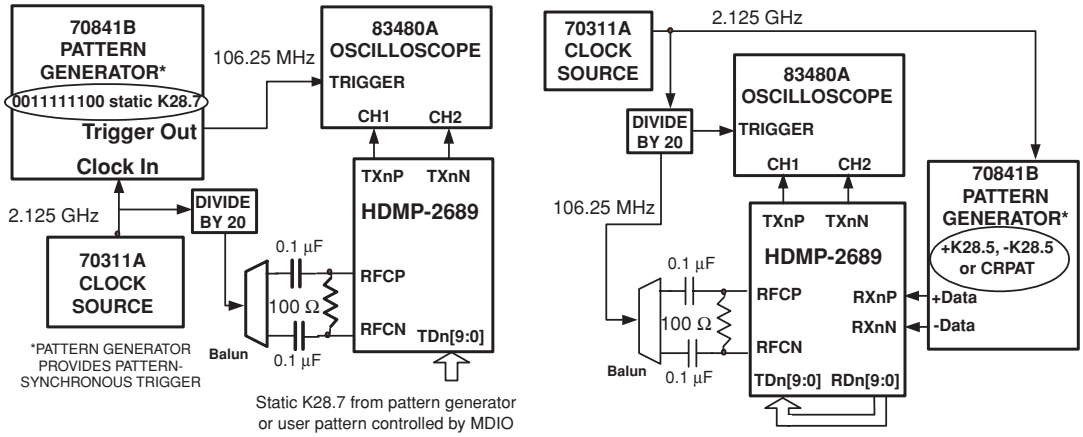


Figure 20. Transmitter DJ and RJ Measurement Method.

Table 19 . Pin Input Capacitance.

Symbol	Parameters	Units	Min	Typ	Max
CINPUT	Input Capacitance on SSTL Input pins	pF		1.1	

Package Information

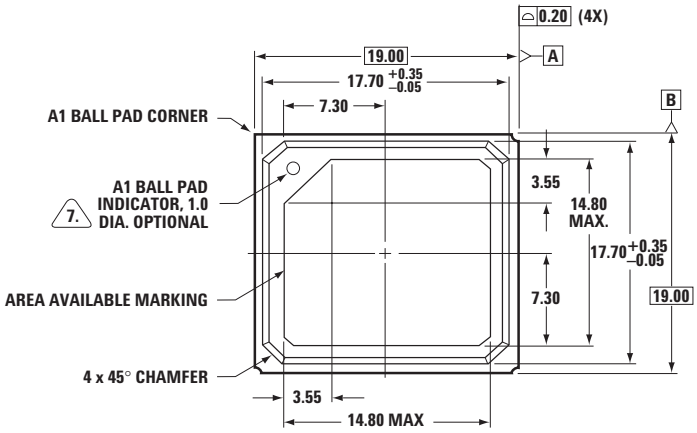
Package Thermal Characteristics

Symbol	Parameter	Units	Typ	Max
P_{Dmax}	Power Dissipation	W		2.5
θ_{JA}[1]	Thermal Resistance: Junction to Ambient Air Flow (LFPM)			
	0	°C/W		27.8
	200	°C/W		24.3
	400	°C/W		23.1
	600	°C/W		22.1
Ψ_{JT}[2]	Thermal Characterization parameter: Junction to package top	°C/W		4.8
Ψ_{JB}[3]	Thermal Characterization parameter: Junction to board	°C/W		19.3

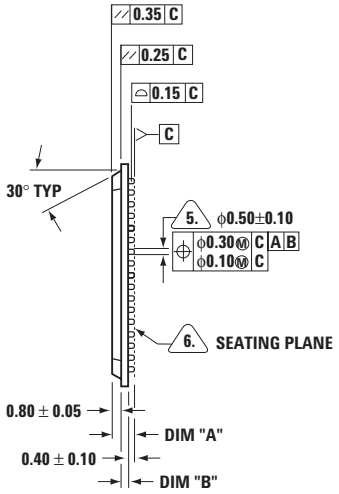
Notes:

Based on independent package testing done by Agilent,

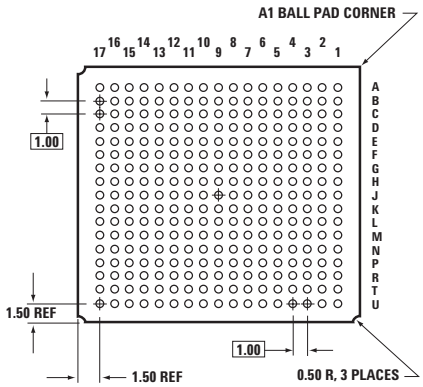
1. θ_{JA} is based on thermal measurement in still air environment at 25°C on a standard 4 x 4" FR4 PCB as specified in EIA/JESD 51-9.
2. Ψ_{JT} is used to determine the actual junction temperature in a given application, using the following equation:
   $T_J = \Psi_{JT} \times P_D + T_T$ where T_T is the measured temperature on top center of the package (also known as Case temperature, Tc) and P_D is the power being dissipated.
3. Ψ_{JB} is used to determine the actual junction temperature in a given application, using the following equation:
   $T_J = \Psi_{JB} \times P_D + T_B$ where T_B is measured board temperature, along the side of package at center on board surface and P_D is the power being dissipated.



TOP VIEW



SIDE VIEW

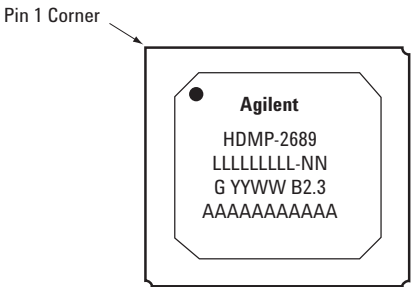


BOTTOM VIEW
289 Solder Balls

4	1.76±0.21	0.56±0.06	STANDARD
NO. LAYERS	DIM "A"	DIM "B"	NOTES
PBGA THICKNESS SCHEDULE			

NOTES: UNLESS OTHERWISE SPECIFIED

1. All dimensions and tolerances conform to ASME Y14.5M-1994.
2. The basic solder ball grid pitch is 1.00 mm.
3. Solder ball matrix size is 17 x 17.
4. Number of solder balls is 289.
5. Dimension is measured at the maximum solder ball diameter. Parallel to primary datum C.
6. Primary datum C and seating plane are defined by the spherical crowns of the solder balls.
7. A1 ball pad corner I.D. for plate mold: marked by laser. Auto mold: dimple formed by mold cap.
8. This drawing conforms to the JEDEC registered outline MS-034/A.



Marking Diagram:

Text Code	**Description**	
LLLLLLLLL NN	LLLLLLLLL=Wafer Lot Number	NN=Wafer Number
B2.3	Die Revision	
G YYWW	G=Supplier Code	
	Date Code (YY=YEAR, WW=WEEK)	
AAAAAAAAAAA	Country of Assembly	

Figure 21. Package Layout and Marking Top View.

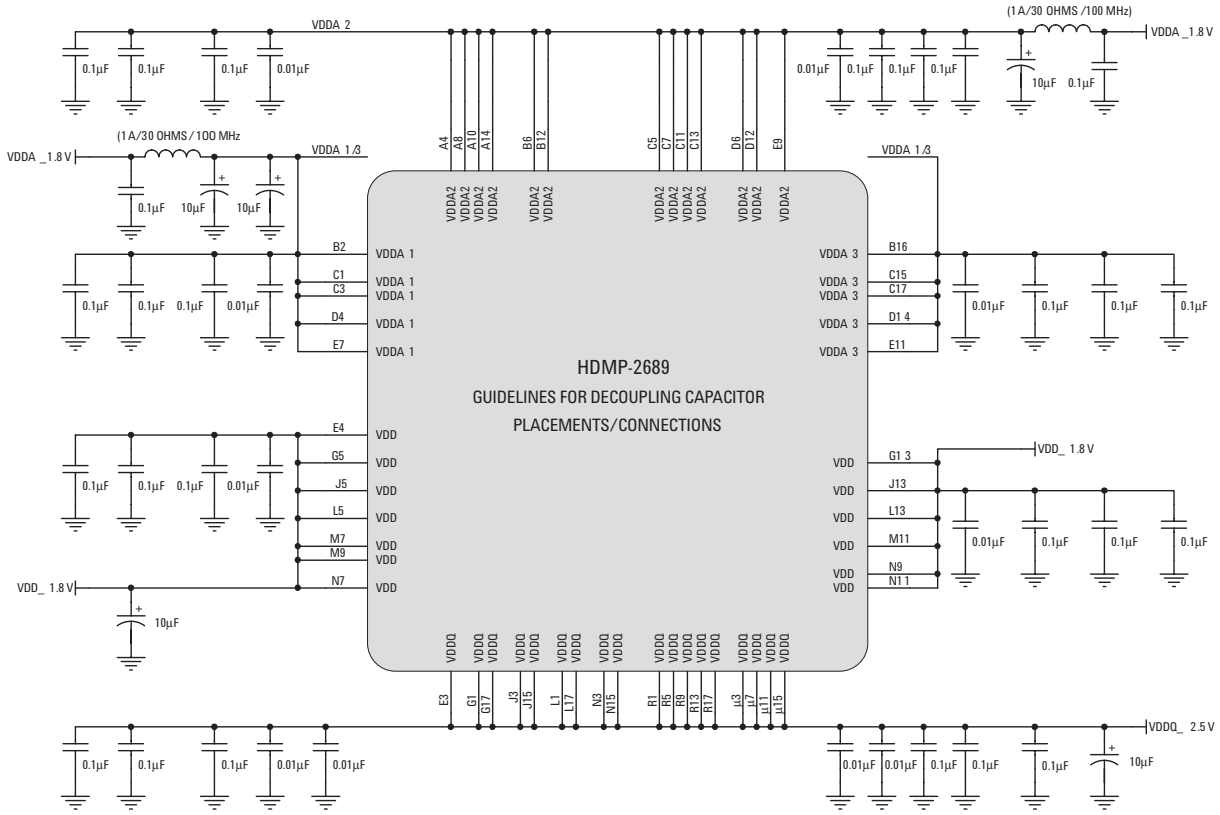


Figure 22. Guidelines for Decoupling Capacitor Connections.

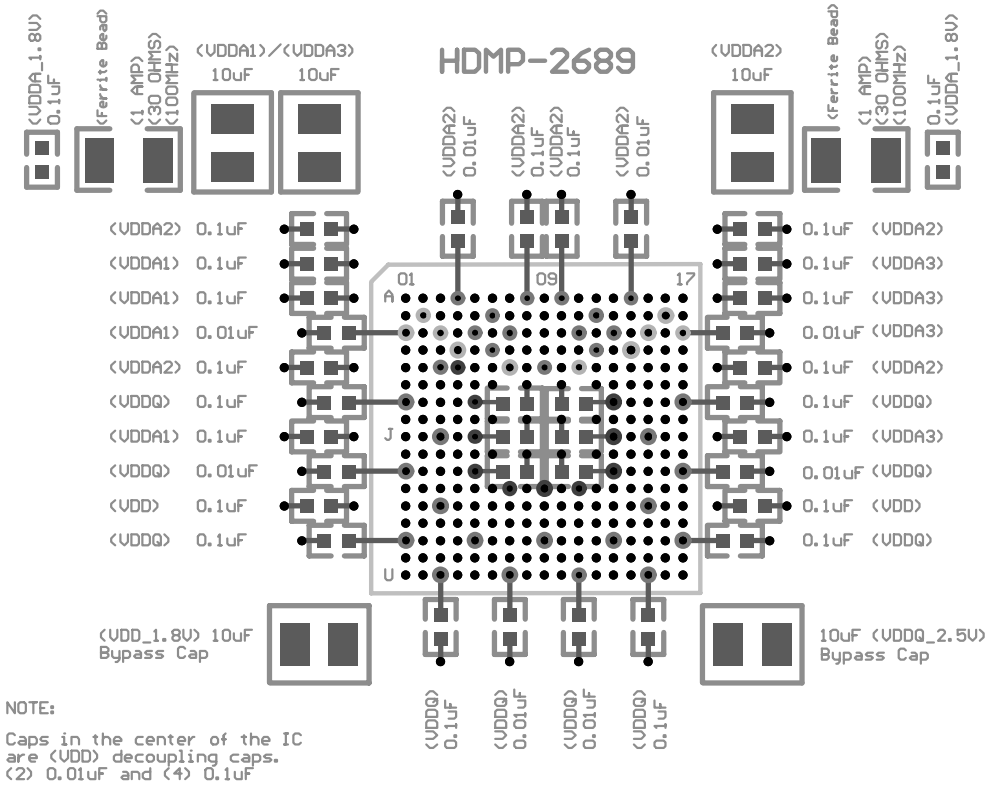


Figure 23. Recommended Decoupling Capacitor Placement.

Pin Diagram

Transceiver Pinout (Top View) (Rev 1.0)
19 mm x 19 mm body, 17 mm by 17 mm array, 289 pins populated, 1 mm ball pitch

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	
A	RXAP	GNDA	RXBP	VDDA2	TXAP	GNDA	TXBP	VDDA2	RFCP	VDDA2	TXCP	GNDA	TXDP	VDDA2	RXCP	GNDA	RXDP	A
B	RXAN	VDDA1	RXBN	GNDA	TXAN	VDDA2	TXBN	GNDA	RFCN	GNDA	TXCN	VDDA2	TXDN	GNDA	RXCN	VDDA3	RXDN	B
C	VDDA1	GNDA	VDDA1	GNDA	VDDA2	GNDA	VDDA2	N/C	GNDA	N/C	VDDA2	GNDA	VDDA2	GNDA	VDDA3	GNDA	VDDA3	C
D	GNDIN	RSVN1	GNDA	VDDA1	GNDA	VDDA2	GNDA	GNDA	GNDA	RREFA	GNDA	VDDA2	GNDA	VDDA3	GNDA	GND	PMX	D
E	GNDD	RSVN2	VDDQ	VDD	GNDA	GNDA	VDDA1	GNDA	VDDA2	GNDA	VDDA3	GNDA	GNDA	GNDIN	N/C	N/C	GNDD	E
F	TCLK	TMS	TDO	TDI	RSTN	GNDA	GNDA	GNDA	GNDA	GNDA	GNDA	GNDA	VREF	GND	DVAD2	DVAD1	DVAD0	F
G	VDDQ	LOSA	GNDD	TRSTN	VDD	GND	GND	GND	GND	GND	GND	GND	VDD	MDIO	MDC	LOSD	VDDQ	G
H	RDA9	RDA8	RDA7	RDA6	GND	GND	GND	GND	GND	GND	GND	GND	GNDIN	RCD	RDD7	RDD8	RDD9	H
J	GNDD	RDA5	VDDQ	RCA	VDD	GND	GND	GND	GND	GND	GND	GND	VDD	RDD3	VDDQ	RDD6	GNDD	J
K	RDA4	RDA3	RDA0	TDA7	GND	GND	GND	GND	GND	GND	GND	GND	GND	TDD7	RDD0	RDD4	RDD5	K
L	VDDQ	RDA1	GNDD	TDA4	VDD	GND	GND	GND	GND	GND	GND	GND	VDD	TDD4	GNDD	RDD1	VDDQ	L
M	RDA2	TDA8	TCA	TDA2	LOSB	GNDIN	VDD	GND	VDD	GND	VDD	GNDIN	LOSC	TDD2	TCD	TDD8	RDD2	M
N	GNDD	TDA6	VDDQ	RDB9	GNDD	RDB4	VDD	GNDIN	VDD	GNDIN	VDD	RCC	GNDD	RDC9	VDDQ	TDD6	GNDD	N
P	TDA9	TDA3	TDA0	RDB7	RDB5	RDB1	TDB8	TDB4	TDB0	TCC	TDC9	RDC2	RDC6	RDC7	TDD0	TDD3	TDD9	P
R	VDDQ	TDA1	GNDD	RDB3	VDDQ	TDB9	GNDD	TDB3	VDDQ	TDC4	GNDD	RDC0	VDDQ	RDC5	GNDD	TDD1	VDDQ	R
T	TDA5	RDB8	RCB	RDB2	TDB7	TDB6	TCB	TDB2	TDC0	TDC3	TDC5	TDC6	TDC8	RDC3	RDC4	RDC8	TDD5	T
U	GNDD	RDB6	VDDQ	RDB0	GNDD	TDB5	VDDQ	TDB1	GNDD	TDC1	VDDQ	TDC2	GNDD	TDC7	VDDQ	RDC1	GNDD	U
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	

Notes:
GND, GNDIN, and GNDD may be connected together.
GNDA is recommended to be on a separate plane.

I/O Type Definitions

I/O Type	Definition
I-CMOS	CMOS input
I/O-CMOS	CMOS bi-directional
O-CMOS	CMOS output
I-LVPECL	LVPECL input
O-SSTL2	SSTL_2 output
I-SSTL2	SSTL_2 input
HS_IN	High speed input
HS_OUT	High speed output
I-ANLG	Analog input
O-ANLG	Analog output
O-PVT	PVT output
S	Power supply or ground
N/C	No connection, must be floating

Pin List

I/O DEFINITION

Name	Pin	Type	Signal
RSTN	F05	I-CMOS	Chip Reset (FIFO Clear): Active Low
DVAD0 DVAD1 DVAD2	F17 F16 F15	I-CMOS	Device Address Input: 3 Bit input address with DVAD2 as MSB. Full address is the Device Address followed by the 2 bit Channel Address.
PMX	D17	I-CMOS	Enable CODEC or buffer mode (see Table 1)
N/C	C08, C10, E15, E16	N/C	No Connect: must be left floating.
MDIO	G14	I/O-CMOS	MDIO Input/Output: Used to read/write the MDIO registers.
MDC	G15	I-CMOS	MDIO Clock: Input clock to the MDIO control block.
RFCP RFCN	A09 B09	I-LVPECL	Differential Reference Input Clock: RFCP (+) and RFCN (-) is the106.25 MHz differential clock pins supplied to the IC. The clock ismultiplied up to generate the serial bit clock and other internal clocks. This is a LVPECL input and assumes AC coupling and 100Ω differentialinput termination into the pad (see Figure 3).
RCA RCB RCC RCD	J04 T03 N12 H14	O-SSTL2	Receiver Byte Clocks: Each receiver drives a 106.25 MHz or 53.125 MHz receive byte clock RCn.
LOSA LOSB LOSC LOSD	G02 M05 M13 G16	O-SSTL2	RX_LOS, Channels A–D: Receive channel loss of signal. If RXnP/N ≥ 300mV peak-to-peak differential, LOSn = logic 0 If 150 mV < RXnP/N < 300mV, LOSn undefined If RXnP/N ≤ 150 mV peak-to-peak differential, LOSn = logic 1
RDA0 RDA1 RDA2 RDA3 RDA4 RDA5 RDA6 RDA7 RDA8 RDA9	K03 L02 M01 K02 K01 J02 H04 H03 H02 H01	O-SSTL2	Receive Data Pins, Channel A: Parallel data on this bus is valid on the rising and falling edge of RCA. See Table 2 for interpretation of this bus under different PMX settings. (See Figure 8 for termination)
RDB0 RDB1 RDB2 RDB3 RDB4 RDB5 RDB6 RDB7 RDB8 RDB9	U04 P06 T04 R04 N06 P05 U02 P04 T02 N04	O-SSTL2	Receive Data Pins, Channel B: Parallel data on this bus is valid on the rising and falling edge of RCB. See Table 2 for interpretation of this bus under different PMX settings. (See Figure 8 for termination)
RDC0 RDC1 RDC2 RDC3 RDC4 RDC5 RDC6 RDC7 RDC8 RDC9	R12 U16 P12 T14 T15 R14 P13 P14 T16 N14	O-SSTL2	Receive Data Pins, Channel C: Parallel data on this bus is valid on the rising and falling edge of RCC. See Table 2 for interpretation of this bus under different PMX settings. (See Figure 8 for termination)

Pin List, continued

I/O DEFINITION			
Name	**Pin**	**Type**	**Signal**
RDD0	K15	O-SSTL2	Receive Data Pins, Channel D: Parallel data on this bus is valid on the rising and falling edges of RCD. See Table 2 for interpretation of this bus under different PMX settings. (See Figure 8 for termination)
RDD1	L16		
RDD2	M17		
RDD3	J14		
RDD4	K16		
RDD5	K17		
RDD6	J16		
RDD7	H15		
RDD8	H16		
RDD9	H17		
RXAP	A01	HS_IN	Received Serial Data Inputs: 0.01 µF AC-coupled high-speed differential inputs (see Figyre 5).
RXAN	B01		
RXBP	A03		
RXBN	B03		
RXCP	A15		
RXCN	B15		
RXDP	A17		
RXDN	B17		
TXAP	A05	HS_ OUT	Transmitted Serial Data Outputs: 0.01 µF AC-coupled high-speed differential inputs (see Figyre 5). Note, if high speed output driver is disabled, then both outputs are held at Logic 1.
TXAN	B05		
TXBP	A07		
TXBN	B07		
TXCP	A11		
TXCN	B11		
TXDP	A13		
TXDN	B13		
TCA	M03	I-SSTL2	Transmit Byte Clock: These pins are used to latch transmit data for channels A, B, C, D into the IC. Must have the same frequency as reference clock.
TCB	T07		
TCC	P10		
TCD	M15		
TDI	F04	I-CMOS	Scan Test Interface: TDI is the test data input, TDO is the test data output, TMS is the test mode select, TCLK is the test clock, and TRSTN is the test reset pin (active low).
TDO	F03	O-CMOS	
TMS	F02	I-CMOS	
TCLK	F01	I-CMOS	
TRSTN	G04	I-CMOS	
TDA0	P03	I-SSTL2	Data Inputs: Parallel data on this bus is clocked in by TCA. See timing diagram in Figure 9. See Table 2 for interpretation of this bus under different PMX settings.
TDA1	R02		
TDA2	M04		
TDA3	P02		
TDA4	L04		
TDA5	T01		
TDA6	N02		
TDA7	K04		
TDA8	M02		
TDA9	P01		
TDB0	P09	I-SSTL2	Data Inputs: Parallel data on this bus is clocked in by TCB. See timing diagram in Figure 9. See Table 2 for interpretation of this bus under different PMX settings.
TDB1	U08		
TDB2	T08		
TDB3	R08		
TDB4	P08		
TDB5	U06		
TDB6	T06		
TDB7	T05		
TDB8	P07		
TDB9	R06		

Pin List, continued

I/O DEFINITION			
Name	**Pin**	**Type**	**Signal**
TDC0 TDC1 TDC2 TDC3 TDC4 TDC5 TDC6 TDC7 TDC8 TDC9	T09 U10 U12 T10 R10 T11 T12 U14 T13 P11	I-SSTL2	Data Inputs: Parallel data on this bus is clocked in by TCC. See timing diagram in Figure 9. See Table 2 for interpretation of this bus under different PMX settings.
TDD0 TDD1 TDD2 TDD3 TDD4 TDD5 TDD6 TDD7 TDD8 TDD9	P15 R16 M14 P16 L14 T17 N16 K14 M16 P17	I-SSTL2	Data Inputs: Parallel data on this bus is clocked in by TCD. See timing diagram in Figure 9. See Table 2 for interpretation of this bus under different PMX settings.
VREF	F13	O-ANLG	Parallel Side Voltage Reference: SSTL_2 output reference voltage, VREF
RREFA	D10	O-ANLG	Analog Voltage Reference: Pin used to connect to an external 12KΩ (1% or better tolerance) reference resistor, which is connected to ground.
RSVN1	D02	I-CMOS	Reserved – Active Low: This is intended for vendor specific functions. Tied to V_{DDQ} in normal operation.
RSVN2	E02	I-CMOS	Reserved – Active Low: This is intended for vendor specific functions. Tied to V_{DDQ} in normal operation.
RSV1	F14	I-CMOS	Reserved – Active High: This is intended for vendor specific functions. Tied to GND in normal operation.
VDD	E04, G05, G13, J05, J13, L05, L13, M07, M09, M11, N07, N09, N11	S	Power Supply: Normally 1.8 volts. Used for core digital logic.
VDDA1	B02, C01 C03, D04 E07		High Speed I/O Supply: Normally 1.8 volts. Used only for the last stage of the high-speed transmitter I/O cells (HS_IN/HS_OUT). Due to high current transitions, this supply should be well bypassed to a ground plane.
VDDA2	A04, A08 A10, A14 B06, B12 C05, C07 C11, C13 D06, D12 E09		VDDA1, VDDA3: Supplies for high-speed differential inputs. VDDA2: Supply for high-speed differential outputs.
VDDA3	B16, C15 C17, D14 E11		
VDDQ	E03, G01, G17, J03, J15, L01, L17, N03, N15, R01, R05, R09, R13, R17, U03, U07, U11, U15	S	Digital I/O Supply: Normally 2.5 volts for SSTL_2 I/O pads.

Pin List, continued

I/O DEFINITION			
Name	**Pin**	**Type**	**Signal**
GNDIN	D01, E14, H13, M06, M12, N08 N10		Receiver Ground: Supply used for input receiver.
GNDD	E01, E17, G03, J01, J17, L03, L15, N01 N05, N13 N17, R03 R07, R11 R15, U01 U05, U09 U13, U17	S	Dirty Ground: Supply used by all the N-drivers on the digital pad ring. Keeps ground bounce away from the GND supply.
GND	D16, G06, G07, G08, G09, G10, G11, G12, H05, H06, H07, H08, H09, H10, H11, H12, J06, J07, J08, J09, J10, J11, J12, K05, K06, K07, K08, K09, K10, K11, K12, K13, L06, L07, L08, L09, L10, L11, L12, M08, M10	S	Ground: Supply used by the digital portion of the pad ring and by the core.
GNDA	A02, A06 A12, A16 B04, B08 B10, B14 C02, C04 C06, C09 C12, C14 C16, D03 D05, D07 D08, D09 D11, D13 D15, E05 E06, E08 E10, E12 E13, F06 F07, F08 F09, F10 F11, F12	S	Analog Ground: Used for TX and RX grounds.

Management Interface Registers

Notes: All registers from 0 to 31 not mentioned below are reserved and should not be accessed.
RO means read only (any value written will be discarded).
RW means the value can be read or written.
Reserved RW means the value should always be written with the indicated default value.

The 2689 responds to four consecutive device addresses, corresponding to the four channels of the device. For example, if the DVAD[0:2] input pins are set to 101, then channel A responds to 101**00**, channel B responds to 101**01**, channel C responds to 101**10**, and channel D responds to 101**11**. Any information which is not specific to one channel (this includes the information in registers 2, 3, and 19) is obtained and/or set via channel A (in this example, device address 10100). These registers all contain "(common)" in their description. Accessing the common registers through any channel other than channel A results in undefined behavior and must be avoided.

Reg 2	**PHY_ID part A (common)**	**Default**	**Mode**
15:0	Organization ID	16'h0033	RO

Reg 3	**PHY_ID part B (common)**	**Default**	**Mode**
15:10	Organization ID	6'h0B	RO
9:4	Manufacturer's Model No.	6'h03	RO
3:0	Rev. No.	4'h1	RO

Registers 2 and 3 are static values that identify the part, and should be read from channel A. They are read-only values.

Reg 17	**Speed and Configuration**	**Default**	**Mode**
15	Transmit Full/Half Speed Control (1=Full)	1	RW
14	Receive Full/Half Speed Control (1=Full)	1	RW
13	Enable Comma Edge Alignment (1: Aligned to particular edge, 0: No specific alignment)	Inverse of PMX pad value	RW
12	Comma Edge Alignment (1: positive edge, 0: negative edge)	0	RW
11	Enable Internal Loopback (same function as register 25, bit 13)	0	RW
10	Include CDR Lock in RX_LOS	0	RW
9:0	Reserved	10'h0	Reserved RW

The transmit full/half speed control is used to set the transmit path of a channel to either a 2.125 GBd serial rate (when set to logic one) or a 1.0625 GBd serial rate. The receive full/half speed control is used to set the receive path of a channel to either a 2.125 GBd serial rate (when set to logic one) or a 1.0625 GBd serial rate. If RX Byte Align Enable (register 24, bit 1) is set (1), then setting Enable Comma Edge Align will cause the recovered clock output for this channel to be aligned such that the comma characters from an ordered set will be always be clocked on the positive edge of RCn (when Comma Edge Alignment is 1), or the negative edge of RCn (when Comma Edge Alignment is 0). Note that this should only be used if the spacing of comma containing control codes is appropriate, as for example in Fibre Channel code sets. The enable loopback bit causes the high speed serial data output to be looped back internally to the high speed deserializer if the bit is set to logic one. This causes the data input to the high-speed input to be ignored. Bit 10 causes the RX PLL loss of CDR (clock data recovery) lock bit to be included in the LOSn signal. The default is that LOSn is determined solely by signal amplitude detection on the serial data inputs.

Reg 19	**9 Bit Error Code (common)**	**Default**	**Mode**
15	Reserved	0	Reserved RW
14:6	Nine Bit Error Code[8:0]	9'h1FE	RW
5:0	Reserved	6'h00	Reserved RW

Register 19 is only applicable in codec mode (PMX=1) and contains the error code output by the 8B/10B decoder when an invalid code or disparity error is detected. When this occurs, pins RDA[8:0] will contain the nine bit error code, and RDA[9] will be asserted to one. On the transmit side, if an invalid K code is clocked into the TDA[9:0] pins, the nine bit error code will be encoded and transmitted. This is a common register: data written to channel A is used for all channels.

Management Interface Registers, continued

Reg 20	Rx Loss of Signal	Default	Mode
15	RX Loss of Signal (reset to 0)	N/A	RO
14:0	Reserved	N/A	RO

Register 20 is the RX loss of signal. It is equivalent to the LOSn pins, for channels A through D, respectively.

Reg 22	PVT Status Register (common)	Default	Mode
15:11	Reserved	5'b00000	RO
10:6	NEN[4:0]	5'b10000	RO
5	Reserved	0	RO
4:0	PEN[4:0]	5'b10000	RO

Register 22 is used to check the drive strengths for the SSTL_2 drivers.

Reg 23	PVT Control Register (common)	Default	Mode
15:13	Reserved	3'b000	Reserved RW
12	Enable Fixed PVT	0	RW
11	Reserved	0	Reserved RW
10:6	NEN[4:0]	5'b00000	RW
5	Reserved	0	Reserved RW
4:0	PEN[4:0]	5'b00000	RW

Register 23 is used to set the drive strength for the SSTL_2 drivers. The pull-up and pull-down drive strengths are set separately through PEN and NEN. For proper operation of terminated SSTL_2 drivers, set PEN to 5'b11000 and NEN to 5'b01000 and set bit 12 to 1'b1. In other words, set register 23 to 16'b0001001000011000 (0x1218). If the reserved bits are not set to zero, unpredictable behavior will occur.

Reg 24	Serdes Configuration Reg 1	Default	Mode
15:2	Reserved	14'h0000	RW
1	RX Byte Align Enable	1	RW
0	SerDes Channel Enable	1	RW

Register 24 includes writeable configuration of a channel's deserializer. Bits 15 through 2 are reserved. Bit 1, when set to logic one, causes the channel to byte align to commas, that is, the deserializer will determine the beginning of a 10 bit byte based upon when it recognizes a comma in the serial data stream. When bit 1 is set to zero, it will randomly determine the beginning of a byte in the serial data stream and will not realign when commas subsequently arrive in the serial data stream. Bit 0 is used to power down both the channel's serializer and deserializer when set to logic 0. When bit 0 is set to logic 0, bit 7 in register 26 must also be set to logic 0 to turn off the associated output driver, minimizing power and ensuring the high speed output is not left in an undefined state.

Management Interface Registers, continued

Reg 25	Serdes Configuration Reg 2	Default	Mode
15	Reserved	0	Reserved RW
14	Pattern Error Monitor Enable	0	RW
13	Test Loopback Enable	0	RW
12	PRBS Enable	0	RW
11	Pattern Toggle Enable	0	RW
10	User Register Enable	0	RW
9:0	User Register[9:0]	10'h0FA	RW

Register 25 includes writeable configuration for self-test. See the "Test" section under the functional description.

Reg 26	Serdes Configuration Reg 3	Default	Mode
15:11	TX Amplitude[4:0]	5'h1F	RW
10:8	TX Peak[2:0]	3'h3	RW
7	TX Output Driver Enable	1	RW
6:0	Reserved	7'h00	Reserved Rw

Register 26 includes writeable configuration of a channel's serializer. Bits 15 through 11 and 10 through 8 are used to set the pre-emphasis on the serial output. These values determine the signal amplitude in the bit time immediately after a transition on the high speed output and in subsequent bit times. Bit 7, when set to logic one, enable channel to drive the data onto the serial output. When set to logic zero, the serial outputs are pulled high and the data is not driven out.

Reg 27	Serdes Status	Default	Mode
15:13	Reserved	3'b000	R0
12	Pattern Failure Detect	1	RO
11	Test Run Complete	0	RO
10:0	Reserved	11'h000	RO

Register 27 includes read only status of self test information. See the "Test" section under the functional description. Bits 10 through 0 are reserved.

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