

DATA SHEET

For a complete data sheet, please also download:

- The IC04 LOCMOS HE4000B Logic Family Specifications HEF, HEC
- The IC04 LOCMOS HE4000B Logic Package Outlines/Information HEF, HEC

HEF40162B

MSI

4-bit synchronous decade counter
with synchronous reset

Product specification
File under Integrated Circuits, IC04

January 1995

4-bit synchronous decade counter with synchronous reset

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DESCRIPTION

The HEF40162B is a fully synchronous edge-triggered 4-bit decade counter with a clock input (CP), four synchronous parallel data inputs (P_0 to P_3), four synchronous mode control inputs (parallel enable ($\overline{PE}$), count enable parallel (CEP), count enable trickle (CET) and synchronous reset ($\overline{SR}$)), buffered outputs from all four bit positions (O_0 to O_3) and a terminal count output (TC).

Operation is synchronous and occurs on the LOW to HIGH transition of CP. When $\overline{PE}$ is LOW, the next LOW to HIGH transition of CP loads data into the counter from P_0 to P_3 . When $\overline{PE}$ is HIGH, the next LOW to HIGH transition of CP

advances the counter to its next state only if both CEP and CET are HIGH; otherwise no change occurs in the state of the counter. TC is HIGH when the state of the counter is 9 ($O_0 = O_3 = \text{HIGH}$, $O_1 = O_2 = \text{LOW}$) and when CET is HIGH. A LOW on $\overline{SR}$ sets all outputs (O_0 to O_3 and TC) LOW on the next LOW to HIGH transition of CP, independent of the state of all other synchronous mode control inputs (CEP, CET and $\overline{PE}$). Multistage synchronous counting is possible without additional components by using a carry look-ahead counting technique; in this case, TC is used to enable successive cascaded stages. CEP, CET, $\overline{PE}$ and $\overline{SR}$ must be stable only during the set-up time before the LOW to HIGH transition of CP.

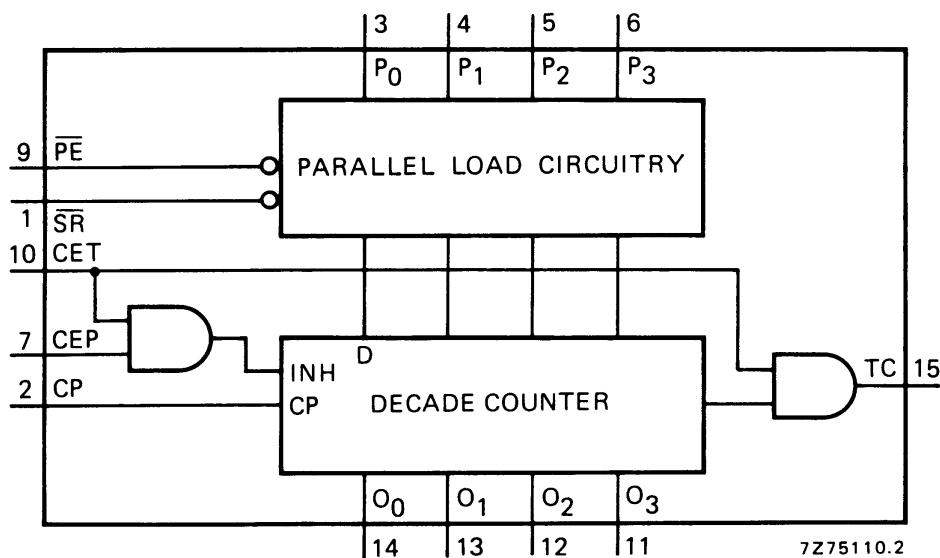


Fig.1 Functional diagram.

FAMILY DATA, I_{DD} LIMITS category MSI

See Family Specifications

4-bit synchronous decade counter with
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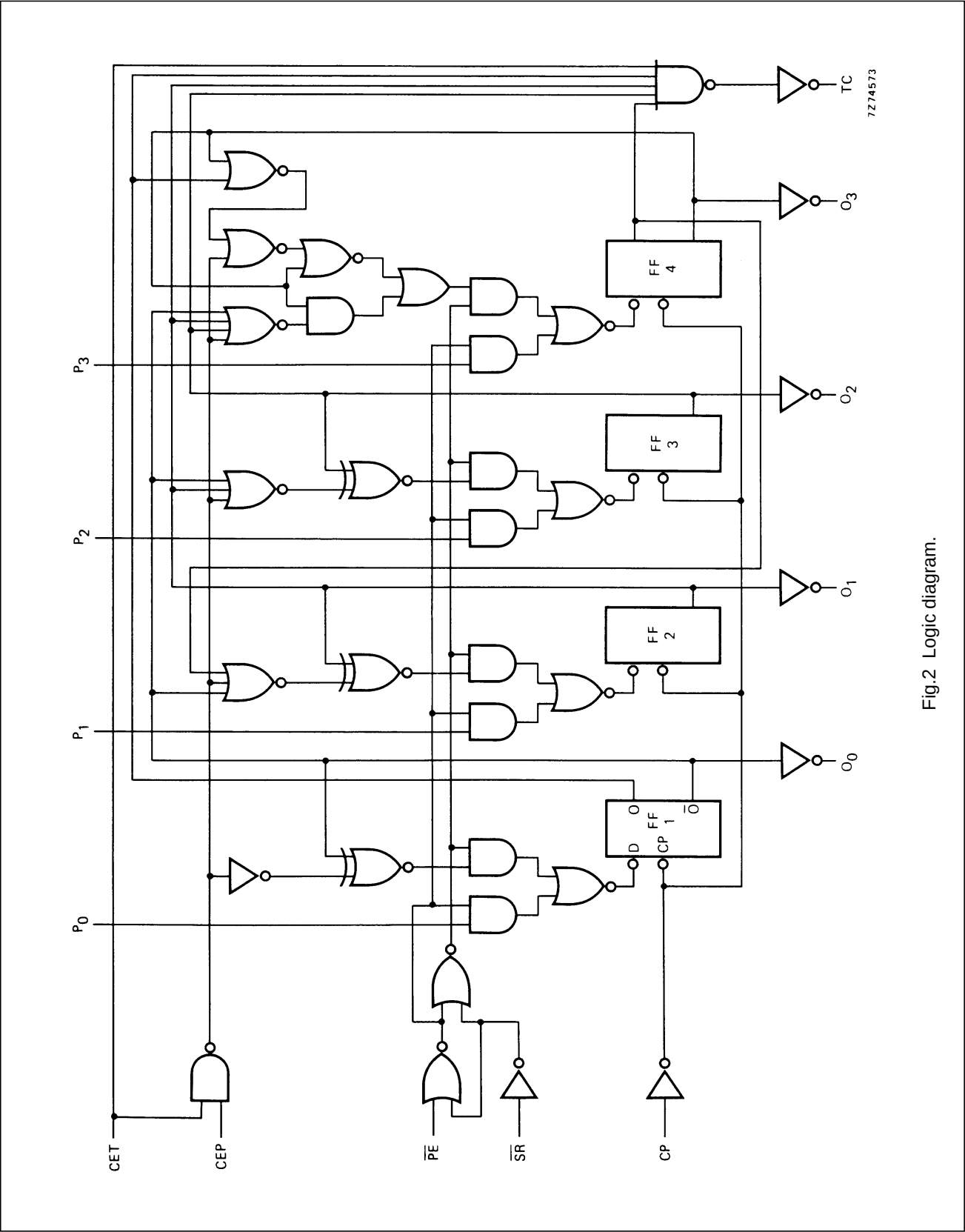
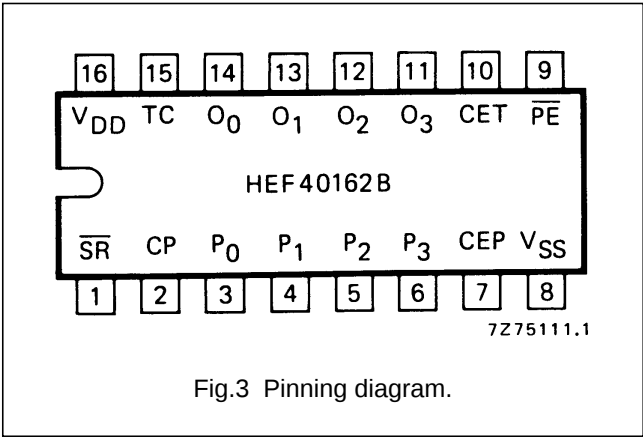


Fig.2 Logic diagram.

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PINNING

$\overline{PE}$ parallel enable input
 P_0 to P_3 parallel data inputs
CEP count enable parallel input
CET count enable trickle input
CP clock input (LOW to HIGH, edge-triggered)
 $\overline{SR}$ synchronous reset input (active LOW)
 O_0 to O_3 parallel outputs
TC terminal count output

HEF40162BP(N): 16-lead DIL; plastic (SOT38-1)
HEF40162BD(F): 16-lead DIL; ceramic (cerdip) (SOT74)
HEF40162BT(D): 16-lead SO; plastic (SOT109-1)
(): Package Designator North America

SYNCHRONOUS MODE SELECTION

$\overline{SR}$	$\overline{PE}$	CEP	CET	MODE
H	L	X	X	preset
H	H	L	X	no change
H	H	X	L	no change
H	H	H	H	count
L	X	X	X	reset

Notes

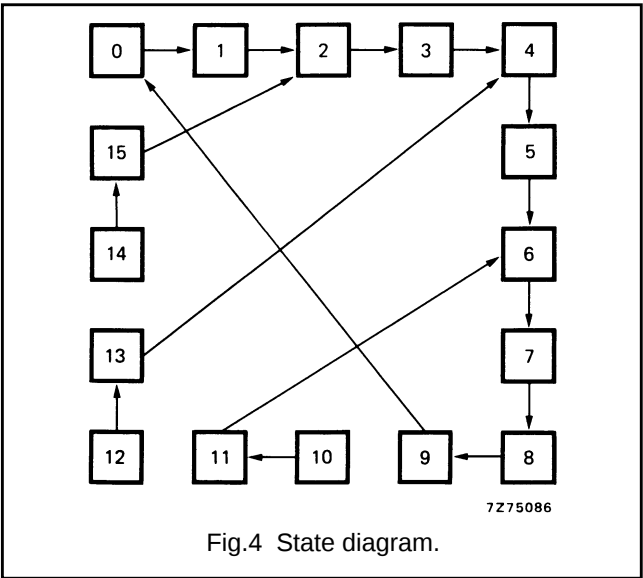
- H = HIGH state (the more positive voltage)
- L = LOW state (the less positive voltage)
- X = state is immaterial

TERMINAL COUNT GENERATION

CET	$(O_0 \cdot \overline{O_1} \cdot \overline{O_2} \cdot O_3)$	TC
L	L	L
L	H	L
H	L	L
H	H	H

Note

- $TC = CET \cdot O_0 \cdot \overline{O_1} \cdot \overline{O_2} \cdot O_3$



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AC CHARACTERISTICS

$V_{SS} = 0$ V; $T_{amb} = 25$ °C; input transition times ≤ 20 ns

	V_{DD} V	TYPICAL FORMULA FOR P (μ W)	
Dynamic power dissipation per package (P)	5 10 15	$1\,200 f_i + \sum (f_o C_L) \times V_{DD}^2$ $5\,600 f_i + \sum (f_o C_L) \times V_{DD}^2$ $16\,000 f_i + \sum (f_o C_L) \times V_{DD}^2$	where f_i = input freq. (MHz) f_o = output freq. (MHz) C_L = load capacitance (pF) $\sum (f_o C_L)$ = sum of outputs V_{DD} = supply voltage (V)

AC CHARACTERISTICS

$V_{SS} = 0$ V; $T_{amb} = 25$ °C; $C_L = 50$ pF; input transition times ≤ 20 ns

	V_{DD} V	SYMBOL	MIN.	TYP.	MAX.	TYPICAL EXTRAPOLATION FORMULA
Propagation delays CP $\rightarrow$ O _n HIGH to LOW	5 10 15	t_{PHL}		110 45 30	220 90 60 ns	$83\text{ ns} + (0,55\text{ ns/pF}) C_L$ $34\text{ ns} + (0,23\text{ ns/pF}) C_L$ $22\text{ ns} + (0,16\text{ ns/pF}) C_L$
LOW to HIGH	5 10 15	t_{PLH}		115 45 35	230 95 65 ns	$88\text{ ns} + (0,55\text{ ns/pF}) C_L$ $34\text{ ns} + (0,23\text{ ns/pF}) C_L$ $27\text{ ns} + (0,16\text{ ns/pF}) C_L$
CP $\rightarrow$ TC HIGH to LOW	5 10 15	t_{PHL}		130 55 35	260 105 75 ns	$103\text{ ns} + (0,55\text{ ns/pF}) C_L$ $44\text{ ns} + (0,23\text{ ns/pF}) C_L$ $27\text{ ns} + (0,16\text{ ns/pF}) C_L$
LOW to HIGH	5 10 15	t_{PLH}		140 55 40	280 115 80 ns	$113\text{ ns} + (0,55\text{ ns/pF}) C_L$ $44\text{ ns} + (0,23\text{ ns/pF}) C_L$ $32\text{ ns} + (0,16\text{ ns/pF}) C_L$
CET $\rightarrow$ TC HIGH to LOW	5 10 15	t_{PHL}		105 50 35	210 100 75 ns	$78\text{ ns} + (0,55\text{ ns/pF}) C_L$ $39\text{ ns} + (0,23\text{ ns/pF}) C_L$ $27\text{ ns} + (0,16\text{ ns/pF}) C_L$
LOW to HIGH	5 10 15	t_{PLH}		90 35 25	185 70 50 ns	$63\text{ ns} + (0,55\text{ ns/pF}) C_L$ $24\text{ ns} + (0,23\text{ ns/pF}) C_L$ $17\text{ ns} + (0,16\text{ ns/pF}) C_L$
Output transition times HIGH to LOW	5 10 15	t_{THL}		60 30 20	120 60 40 ns	$10\text{ ns} + (1,0\text{ ns/pF}) C_L$ $9\text{ ns} + (0,42\text{ ns/pF}) C_L$ $6\text{ ns} + (0,28\text{ ns/pF}) C_L$
LOW to HIGH	5 10 15	t_{TLH}		60 30 20	120 60 40 ns	$10\text{ ns} + (1,0\text{ ns/pF}) C_L$ $9\text{ ns} + (0,42\text{ ns/pF}) C_L$ $6\text{ ns} + (0,28\text{ ns/pF}) C_L$

4-bit synchronous decade counter with synchronous reset

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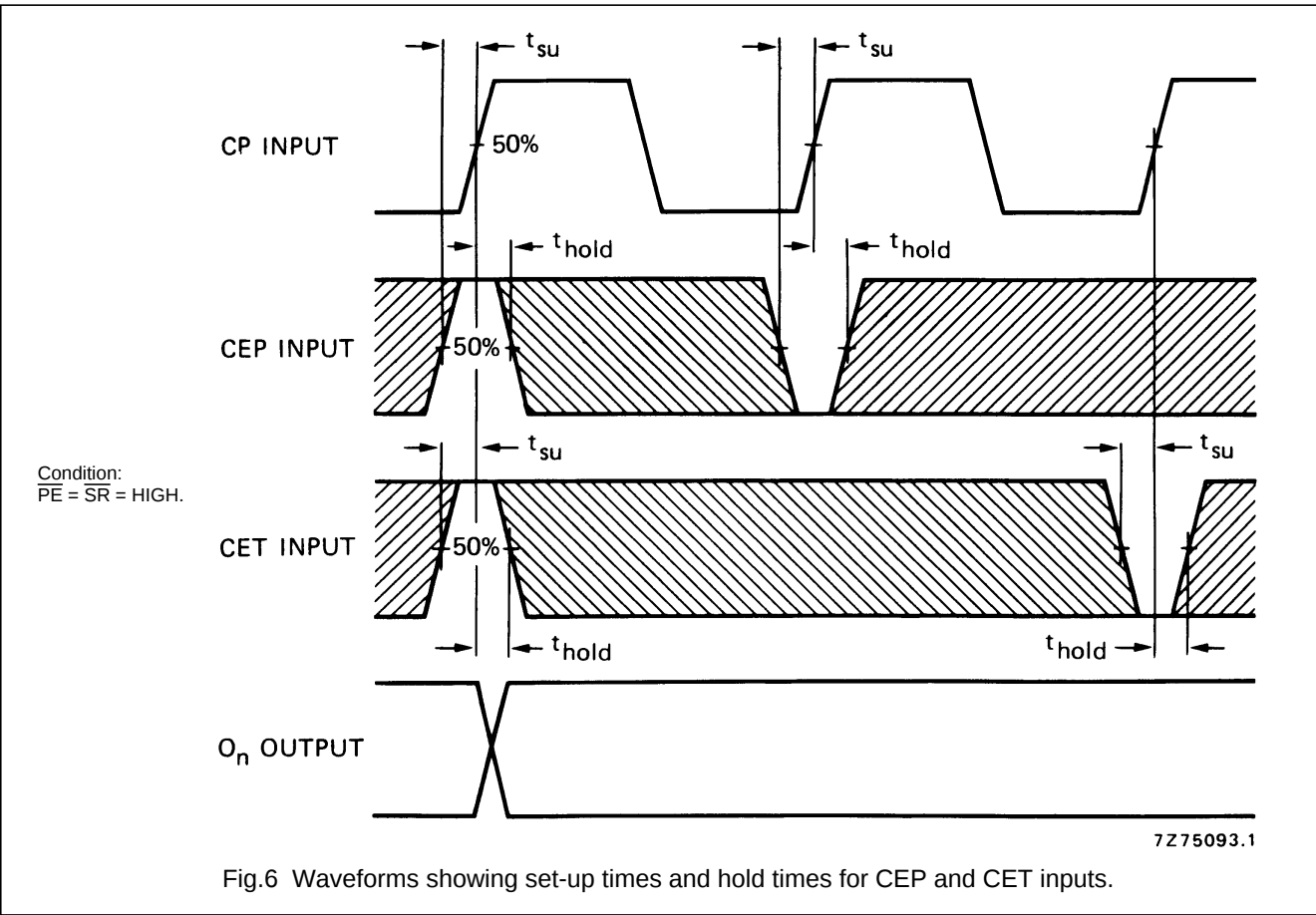
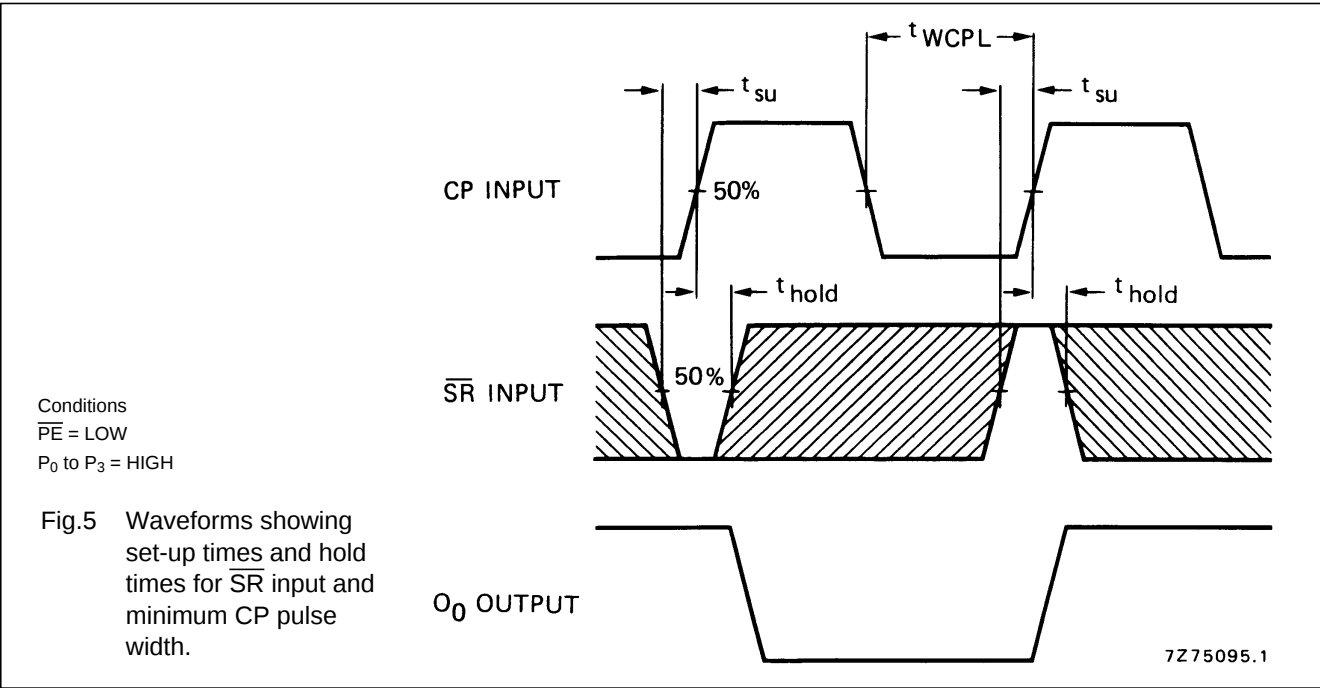
AC CHARACTERISTICS

$V_{SS} = 0$ V; $T_{amb} = 25$ °C; $C_L = 50$ pF; input transition times ≤ 20 ns

	V_{DD} V	SYMBOL	MIN.	TYP.	MAX.	
Minimum clock pulse width; LOW	5	t_{WCPL}	100	50	ns	see also waveforms Figs 5, 6, 7 and 8
	10		40	20	ns	
	15		30	15	ns	
Set-up times $P_n \rightarrow CP$	5	t_{su}	110	55	ns	
	10		40	20	ns	
	15		30	15	ns	
$\overline{PE} \rightarrow CP$	5	t_{su}	120	60	ns	
	10		40	20	ns	
	15		25	10	ns	
CEP, CET $\rightarrow CP$	5	t_{su}	260	130	ns	
	10		100	50	ns	
	15		70	35	ns	
$\overline{SR} \rightarrow CP$	5	t_{su}	50	25	ns	
	10		20	10	ns	
	15		15	10	ns	
Hold times $P_n \rightarrow CP$	5	t_{hold}	20	-35	ns	
	10		10	-10	ns	
	15		5	-10	ns	
$\overline{PE} \rightarrow CP$	5	t_{hold}	15	-45	ns	
	10		5	-15	ns	
	15		5	-10	ns	
CEP, CET $\rightarrow CP$	5	t_{hold}	25	-105	ns	
	10		15	-35	ns	
	15		10	-25	ns	
$\overline{SR} \rightarrow CP$	5	t_{hold}	15	-10	ns	
	10		5	-5	ns	
	15		5	0	ns	
Maximum clock pulse frequency	5	f_{max}	2,5	5	MHz	
	10		7	14	MHz	
	15		9	18	MHz	

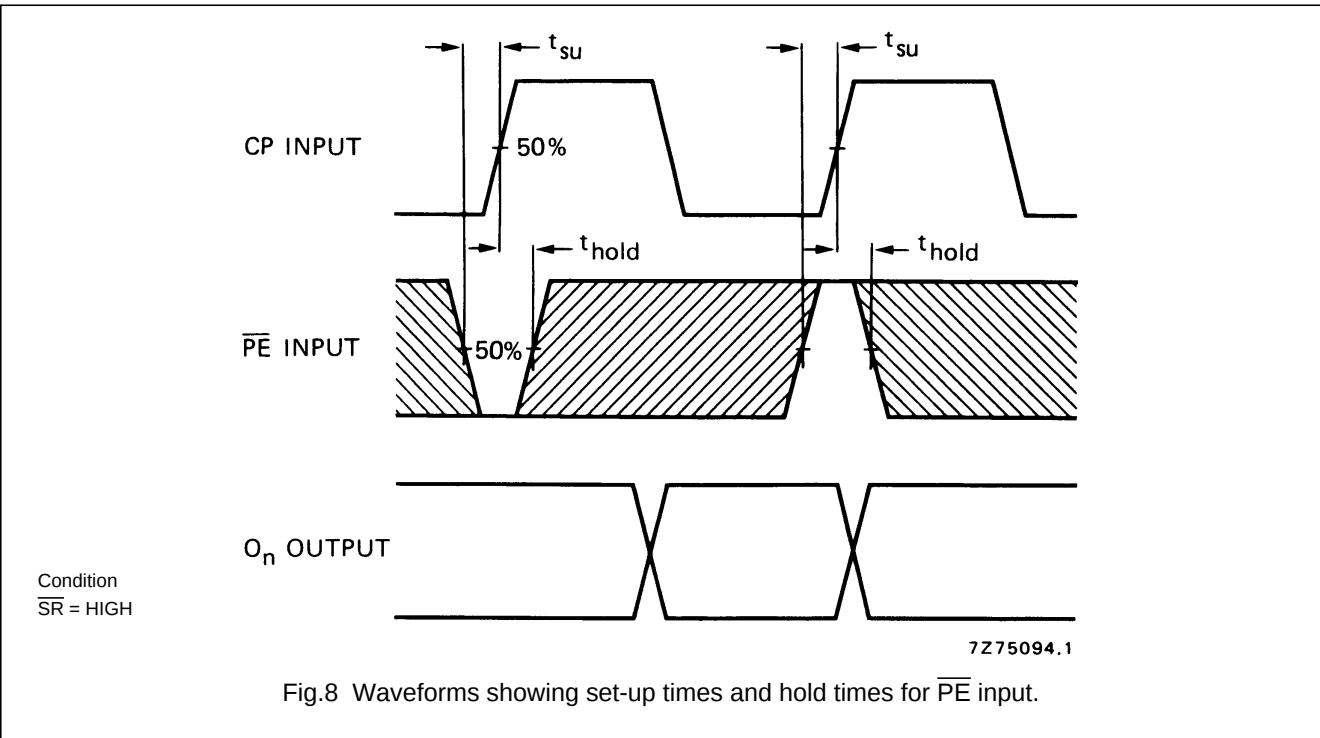
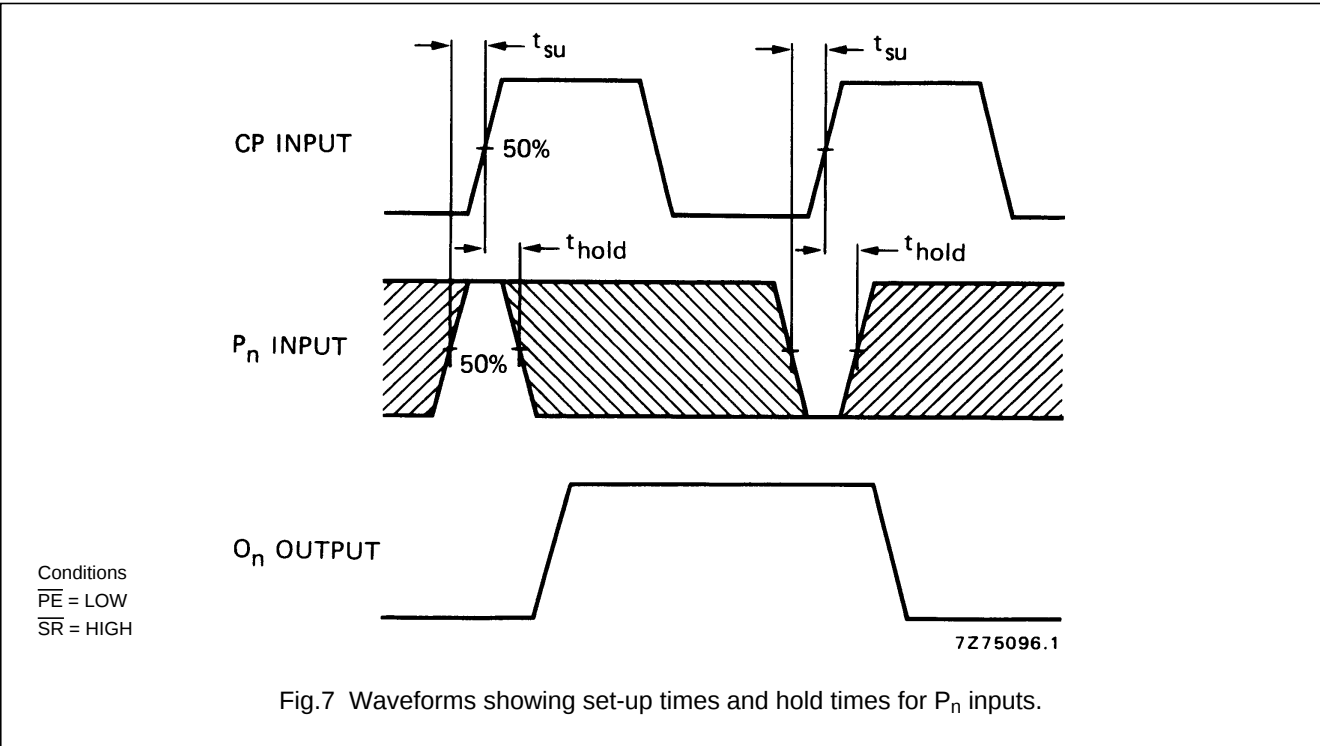
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Note
Set-up and hold times are shown as positive values but may be specified as negative values.

4-bit synchronous decade counter with synchronous reset

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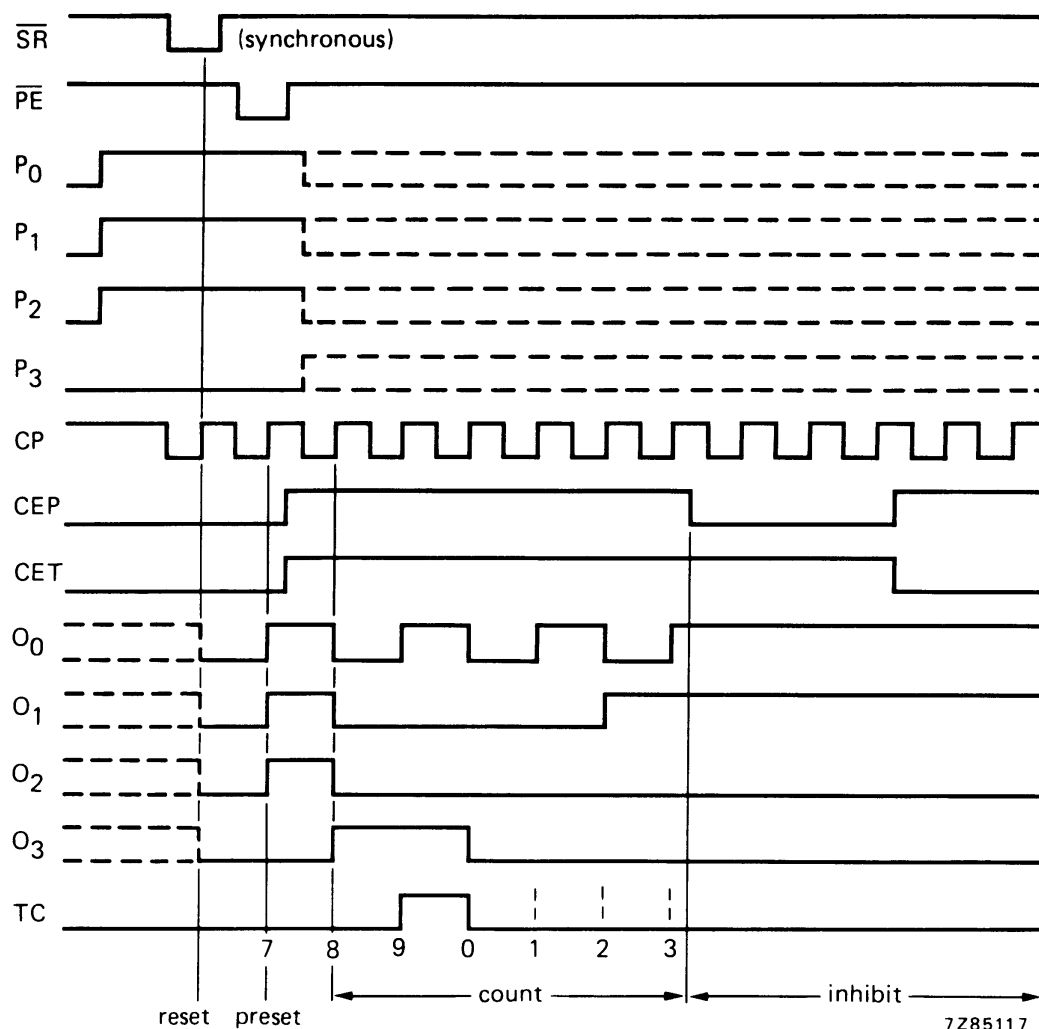


Fig.9 Timing diagram.

APPLICATION INFORMATION

An example of an application for the HEF40162B is:

- Programmable decade counter.

4-bit synchronous decade counter with
synchronous reset

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