查询HEF4020B供应商 捷多邦，专业PCB打样工厂，24小时加急出货

DATA SHEET

For a complete data sheet, please also download:

- The IC04 LOCMOS HE4000B Logic Family Specifications HEF, HEC
- The IC04 LOCMOS HE4000B Logic Package Outlines/Information HEF, HEC

HEF4020B
MSI
14-stage binary counter

Product specification
File under Integrated Circuits, IC04

January 1995

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Philips Semiconductors

PHILIPS PHILIPS

14-stage binary counter

HEF4020B
MSI

DESCRIPTION

The HEF4020B is a 14-stage binary ripple counter with a clock input ($\overline{CP}$), an overriding asynchronous master reset input (MR) and twelve fully buffered outputs (O_0, O_3 to O_{13}). The counter advances on the HIGH to LOW transition of $\overline{CP}$. A HIGH on MR clears all counter stages and forces all outputs LOW, independent of the state of $\overline{CP}$. Each counter stage is a static toggle flip-flop. A feature of the HEF4020B is: high speed (typ. 35 MHz at V_{DD} = 15 V).

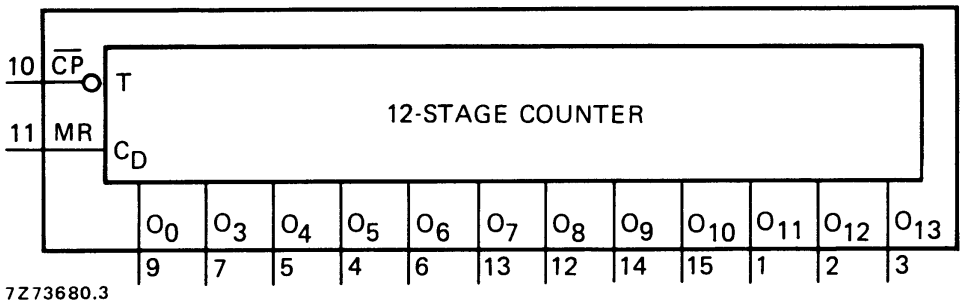

Fig.1 Functional diagram.

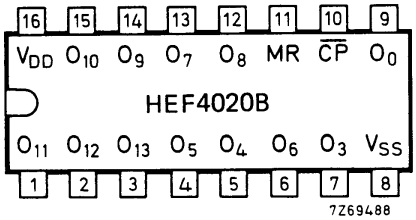

Fig.2 Pinning diagram.

HEF4020BP(N): 16-lead DIL; plastic (SOT38-1)

HEF4020BD(F): 16-lead DIL; ceramic (cerdip) (SOT74)

HEF4020BT(D): 16-lead SO; plastic (SOT109-1)

( ): Package Designator North America

PINNING

$\overline{CP}$	clock input (HIGH to LOW edge triggered)
MR	master reset input (active HIGH)
O_0, O_3 to O_{13}	parallel outputs

FAMILY DATA, I_{DD} LIMITS category MSI

See Family Specifications

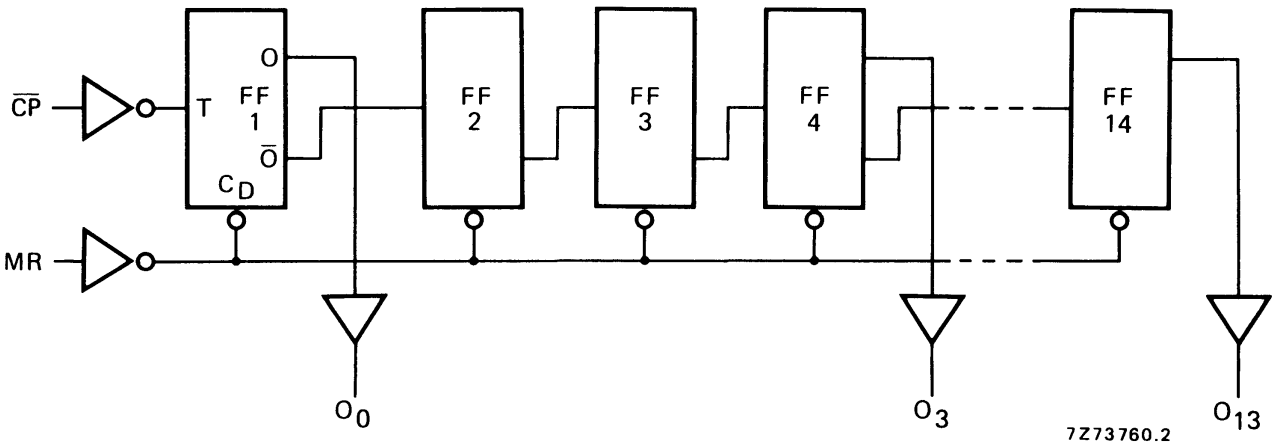

Fig.3 Logic diagram.

AC CHARACTERISTICS

V_{SS} = 0 V; T_{amb} = 25 °C; C_L = 50 pF; input transition times ≤ 20 ns; see also waveforms Fig.4

	V_{DD} V	SYMBOL	MIN.	TYP.	MAX.		TYPICAL EXTRAPOLATION FORMULA
Propagation delays							
$\overline{CP} \rightarrow O_0$	5			105	210	ns	78 ns + (0,55 ns/pF) C_L
HIGH to LOW	10	t_{PHL}		45	90	ns	34 ns + (0,23 ns/pF) C_L
	15			30	65	ns	22 ns + (0,16 ns/pF) C_L
	5			105	210	ns	78 ns + (0,55 ns/pF) C_L
LOW to HIGH	10	t_{PLH}		50	95	ns	39 ns + (0,23 ns/pF) C_L
	15			35	70	ns	27 ns + (0,16 ns/pF) C_L
$O_n \rightarrow O_n + 1$	5			80	160	ns	53 ns + (0,55 ns/pF) C_L
HIGH to LOW	10	t_{PHL}		30	60	ns	19 ns + (0,23 ns/pF) C_L
	15			20	40	ns	12 ns + (0,16 ns/pF) C_L
	5			70	140	ns	43 ns + (0,55 ns/pF) C_L
LOW to HIGH	10	t_{PLH}		25	50	ns	14 ns + (0,23 ns/pF) C_L
	15			20	40	ns	12 ns + (0,16 ns/pF) C_L
$MR \rightarrow O_n$	5			180	360	ns	153 ns + (0,55 ns/pF) C_L
HIGH to LOW	10	t_{PHL}		90	180	ns	79 ns + (0,23 ns/pF) C_L
	15			70	140	ns	62 ns + (0,16 ns/pF) C_L
Output transition times	5			60	120	ns	10 ns + (1,0 ns/pF) C_L
HIGH to LOW	10	t_{THL}		30	60	ns	9 ns + (0,42 ns/pF) C_L
	15			20	40	ns	6 ns + (0,28 ns/pF) C_L
	5			60	120	ns	10 ns + (1,0 ns/pF) C_L
LOW to HIGH	10	t_{TLH}		30	60	ns	9 ns + (0,42 ns/pF) C_L
	15			20	40	ns	6 ns + (0,28 ns/pF) C_L
Minimum clock	5		50	25		ns	
pulse width; HIGH	10	t_{WCPH}	25	15		ns	
	15		20	10		ns	
Minimum MR	5		130	65		ns	
pulse width; HIGH	10	t_{WMRH}	95	50		ns	
	15		90	45		ns	
Recovery time	5		115	60		ns	
for MR	10	t_{RMR}	65	35		ns	
	15		55	25		ns	
Maximum clock	5		5	10		MHz	
pulse frequency	10	f_{max}	13	25		MHz	
	15		18	35		MHz	

	V_{DD} V	TYPICAL FORMULA FOR P (μW)	
Dynamic power dissipation per package (P)	5	$600\ f_i + \sum (f_o\ C_L) \times V_{DD}^2$	where f_i = input freq. (MHz) f_o = output freq. (MHz) C_L = load cap. (pF) $\sum (f_o C_L)$ = sum of outputs V_{DD} = supply voltage (V)
	10	$2\ 800\ f_i + \sum (f_o\ C_L) \times V_{DD}^2$	
	15	$8\ 200\ f_i + \sum (f_o\ C_L) \times V_{DD}^2$	

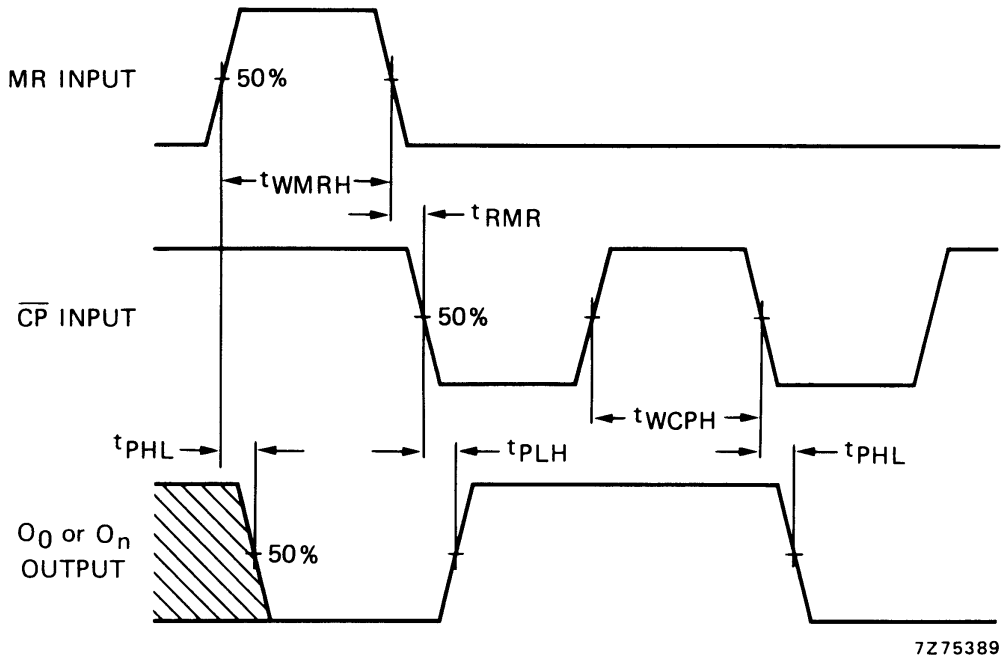

Fig.4 Waveforms showing propagation delays for MR to O_n and $\overline{CP}$ to O_0, minimum MR and $\overline{CP}$ pulse widths.

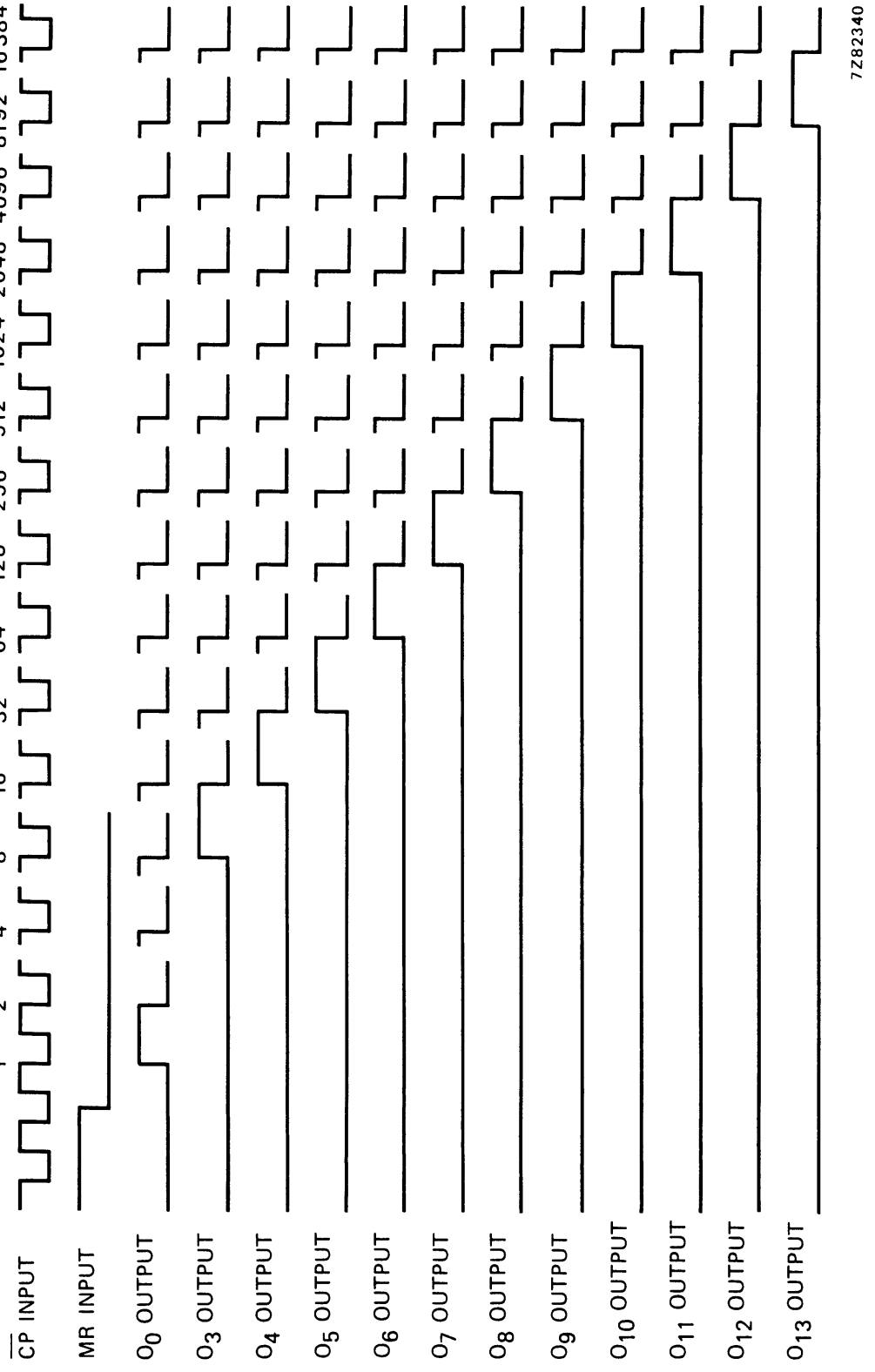

Fig.5 Timing diagram.