360MHz, Low Power, Video Operational Amplifier with Output Limiting

The HFA1135 is a high speed, low power current feedback amplifier build with Intersil's proprietary complementary bipolar UHF-1 process. This amplifier features user programmable output limiting, via the V_H and V_L pins.

The HFA1135 is the ideal choice for high speed, low power applications requiring output limiting (e.g. flash A/D drivers), especially those requiring fast overdrive recovery times. The limiting function allows the designer to set the maximum and minimum output levels to protect downstream stages from damage or input saturation. The sub-nanosecond overdrive recovery time ensures a quick return to linear operation following an overdrive condition.

Component and composite video systems also benefit from this operational amplifier's performance, as indicated by the gain flatness, and differential gain and phase specifications.

The HFA1135 is a low power, high performance upgrade for the CLC501 and CLC502.

Ordering Information

PART NUMBER (BRAND)	TEMP. RANGE (^oC)	PACKAGE	PKG. NO.
HFA1135IB (H1135I)	-40 to 85	8 Ld SOIC	M8.15
HFA1135IB96 (H1135I)	-40 to 85	8 Ld SOIC Tape and Reel	M8.15
HFA11XXEVAL	DIP Evaluation Board for High Speed Op Amps		

Features

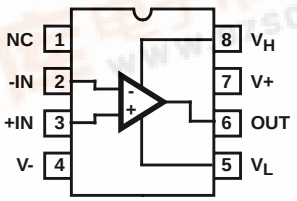
- User Programmable Output Voltage Limiting
- Fast Overdrive Recovery . . . . . <1ns
- Low Supply Current 6.8mA
- High Input Impedance 2MΩ
- Wide -3dB Bandwidth 360MHz
- Very Fast Slew Rate 1200V/µs
- Gain Flatness (to 50MHz) . . . . . ±0.07dB
- Differential Gain 0.02%
- Differential Phase . . . . . 0.04 Degrees
- Pin Compatible Upgrade to CLC501 and CLC502

Applications

- Flash A/D Drivers
- High Resolution Monitors
- Professional Video Processing
- Video Digitizing Boards/Systems
- Multimedia Systems
- RGB Preamps
- Medical Imaging
- Hand Held and Miniaturized RF Equipment
- Battery Powered Communications

Pinout

HFA1135
(SOIC)
TOP VIEW



Absolute Maximum Ratings $T_A = 25^oC$

Voltage Between V+ and V- 11V
DC Input Voltage . . . . . V_{SUPPLY}
Differential Input Voltage 8V
Output Current (Note 1) . . . . . Short Circuit Protected
30mA Continuous
60mA ≤ 50% Duty Cycle
ESD Rating . . . . . >600V

Thermal Information

Thermal Resistance (Typical, Note 1)	θ_{JA} ($^oC/W$)
SOIC Package	165

Maximum Junction Temperature (Die Only) . . . . . 175^oC
Maximum Junction Temperature (Plastic Package) . . . . . 150^oC
Maximum Storage Temperature Range . . . . . -65^oC to 150^oC
Maximum Lead Temperature (Soldering 10s) . . . . . 300^oC
(SOIC - Lead Tips Only)

Operating Conditions

Temperature Range . . . . . -40^oC to 85^oC

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

1. θ_{JA} is measured with the component mounted on a low effective thermal conductivity test board in free air. See Tech Brief TB379 for details.

Electrical Specifications $V_{SUPPLY} = \pm5V$, $A_V = +1$, $R_F = 510\Omega$ (Note 3), $R_L = 100\Omega$, Unless Otherwise Specified

PARAMETER	TEST CONDITIONS	(NOTE 2) TEST LEVEL	TEMP. (^oC)	MIN	TYP	MAX	UNITS
INPUT CHARACTERISTICS							
Input Offset Voltage		A	25	-	2	5	mV
		A	Full	-	3	8	mV
Average Input Offset Voltage Drift		B	Full	-	1	10	$\mu V/^oC$
Input Offset Voltage Common-Mode Rejection Ratio	$\Delta V_{CM} = \pm1.8V$	A	25	47	50	-	dB
	$\Delta V_{CM} = \pm1.8V$	A	85	45	48	-	dB
	$\Delta V_{CM} = \pm1.2V$	A	-40	45	48	-	dB
Input Offset Voltage Power Supply Rejection Ratio	$\Delta V_{PS} = \pm1.8V$	A	25	50	54	-	dB
	$\Delta V_{PS} = \pm1.8V$	A	85	47	50	-	dB
	$\Delta V_{PS} = \pm1.2V$	A	-40	47	50	-	dB
Non-Inverting Input Bias Current		A	25	-	6	15	µA
		A	Full	-	10	25	µA
Non-Inverting Input Bias Current Drift		B	Full	-	5	60	$nA/^oC$
Non-Inverting Input Bias Current Power Supply Sensitivity	$\Delta V_{PS} = \pm1.8V$	A	25	-	0.5	1	µA/V
	$\Delta V_{PS} = \pm1.8V$	A	85	-	0.8	3	µA/V
	$\Delta V_{PS} = \pm1.2V$	A	-40	-	0.8	3	µA/V
Non-Inverting Input Resistance	$\Delta V_{CM} = \pm1.8V$	A	25	0.8	2	-	MΩ
	$\Delta V_{CM} = \pm1.8V$	A	85	0.5	1.3	-	MΩ
	$\Delta V_{CM} = \pm1.2V$	A	-40	0.5	1.3	-	MΩ
Inverting Input Bias Current		A	25	-	0.1	4	µA
		A	Full	-	3	8	µA
Inverting Input Bias Current Drift		B	Full	-	60	200	$nA/^oC$
Inverting Input Bias Current Common-Mode Sensitivity	$\Delta V_{CM} = \pm1.8V$	A	25	-	3	6	µA/V
	$\Delta V_{CM} = \pm1.8V$	A	85	-	4	8	µA/V
	$\Delta V_{CM} = \pm1.2V$	A	-40	-	4	8	µA/V
Inverting Input Bias Current Power Supply Sensitivity	$\Delta V_{PS} = \pm1.8V$	A	25	-	2	5	µA/V
	$\Delta V_{PS} = \pm1.8V$	A	85	-	4	8	µA/V
	$\Delta V_{PS} = \pm1.2V$	A	-40	-	4	8	µA/V
Inverting Input Resistance		C	25	-	40	-	Ω
Input Capacitance (Either Input)		C	25	-	1.6	-	pF

Electrical Specifications V_{SUPPLY} = ±5V, A_V = +1, R_F = 510Ω (Note 3), R_L = 100Ω, Unless Otherwise Specified **(Continued)**

PARAMETER	TEST CONDITIONS	(NOTE 2) TEST LEVEL	TEMP. (^oC)	MIN	TYP	MAX	UNITS
Input Voltage Common Mode Range (Implied by V_{IO} CMRR, $+R_{IN}$, and $-I_{BIAS}$ CMS tests)		A	25, 85	±1.8	±2.4	-	V
		A	-40	±1.2	±1.7	-	V
Input Noise Voltage Density (Note 5)	f = 100kHz	B	25	-	3.5	-	nV/√Hz
Non-Inverting Input Noise Current Density (Note 5)	f = 100kHz	B	25	-	2.5	-	pA/√Hz
Inverting Input Noise Current Density (Note 5)	f = 100kHz	B	25	-	20	-	pA/√Hz
TRANSFER CHARACTERISTICS							
Open Loop Transimpedance Gain (Note 5)	A_V = -1	C	25	-	500	-	kΩ
AC CHARACTERISTICS A_V = +2, R_F = 250Ω, Unless Otherwise Specified							
-3dB Bandwidth (V_{OUT} = 0.2V_{P-P}, Note 5)	A_V = +1, R_F = 1.5kΩ	B	25	-	660	-	MHz
	A_V = +2, R_F = 250Ω	B	25	-	360	-	MHz
	A_V = +2, R_F = 330Ω	B	25	-	315	-	MHz
	A_V = -1, R_F = 330Ω	B	25	-	290	-	MHz
Full Power Bandwidth (V_{OUT} = 5V_{P-P} at A_V = +2/-1, 4V_{P-P} at A_V = +1, Note 5)	A_V = +1, R_F = 1.5kΩ	B	25	-	90	-	MHz
	A_V = +2, R_F = 250Ω	B	25	-	130	-	MHz
	A_V = -1, R_F = 330Ω	B	25	-	170	-	MHz
Gain Flatness (to 25MHz, V_{OUT} = 0.2V_{P-P}, Note 5)	A_V = +1, R_F = 1.5kΩ	B	25	-	±0.10	-	dB
	A_V = +2, R_F = 250Ω	B	25	-	±0.02	-	dB
	A_V = +2, R_F = 330Ω	B	25	-	±0.02	-	dB
Gain Flatness (to 50MHz, V_{OUT} = 0.2V_{P-P}, Note 5)	A_V = +1, R_F = 1.5kΩ	B	25	-	±0.22	-	dB
	A_V = +2, R_F = 250Ω	B	25	-	±0.07	-	dB
	A_V = +2, R_F = 330Ω	B	25	-	±0.03	-	dB
Minimum Stable Gain		A	Full	-	1	-	V/V
OUTPUT CHARACTERISTICS R_F = 510Ω, Unless Otherwise Specified							
Output Voltage Swing (Note 5)	A_V = -1, R_L = 100Ω	A	25	±3	±3.4	-	V
		A	Full	±2.8	±3	-	V
Output Current (Note 5)	A_V = -1, R_L = 50Ω	A	25, 85	50	60	-	mA
		A	-40	28	42	-	mA
Output Short Circuit Current		B	25	-	90	-	mA
Closed Loop Output Resistance (Note 5)	DC, A_V = +2, R_F = 250Ω	B	25	-	0.07	-	Ω
Second Harmonic Distortion (A_V = +2, R_F = 250Ω, V_{OUT} = 2V_{P-P}, Note 5)	10MHz	B	25	-	-50	-	dBc
	20MHz	B	25	-	-45	-	dBc
Third Harmonic Distortion (A_V = +2, R_F = 250Ω, V_{OUT} = 2V_{P-P}, Note 5)	10MHz	B	25	-	-50	-	dBc
	20MHz	B	25	-	-45	-	dBc
TRANSIENT CHARACTERISTICS A_V = +2, R_F = 250Ω, Unless Otherwise Specified							
Rise and Fall Times (V_{OUT} = 0.5V_{P-P}, Note 5)	Rise Time	B	25	-	0.81	-	ns
	Fall Time	B	25	-	1.25	-	ns
Overshoot (Note 4) (V_{OUT} = 0 to 0.5V, V_{IN} t_{RISE} = 2.5ns)	+OS	B	25	-	3	-	%
	-OS	B	25	-	5	-	%
Overshoot (Note 4) (V_{OUT} = 0.5V_{P-P}, V_{IN} t_{RISE} = 2.5ns)	+OS	B	25	-	2	-	%
	-OS	B	25	-	10	-	%
Slew Rate (V_{OUT} = 4V_{P-P}, A_V = +1, R_F = 1.5kΩ)	+SR	B	25	-	875	-	V/µs
	-SR (Note 6)	B	25	-	510	-	V/µs
Slew Rate (V_{OUT} = 5V_{P-P}, A_V = +2, R_F = 250Ω)	+SR	B	25	-	1530	-	V/µs
	-SR (Note 6)	B	25	-	850	-	V/µs

Electrical Specifications V_{SUPPLY} = ±5V, A_V = +1, R_F = 510Ω (Note 3), R_L = 100Ω, Unless Otherwise Specified **(Continued)**

PARAMETER	TEST CONDITIONS	(NOTE 2) TEST LEVEL	TEMP. (^oC)	MIN	TYP	MAX	UNITS
Slew Rate (V_{OUT} = 5V_{P-P}, A_V = -1, R_F = 330Ω)	+SR	B	25	-	2300	-	V/µs
	-SR (Note 6)	B	25	-	1200	-	V/µs
Settling Time (V_{OUT} = +2V to 0V step, Note 5)	To 0.1%	B	25	-	23	-	ns
	To 0.05%	B	25	-	33	-	ns
	To 0.02%	B	25	-	45	-	ns
VIDEO CHARACTERISTICS A_V = +2, R_F = 250Ω, Unless Otherwise Specified							
Differential Gain (f = 3.58MHz)	R_L = 150Ω	B	25	-	0.02	-	%
	R_L = 75Ω	B	25	-	0.03	-	%
Differential Phase (f = 3.58MHz)	R_L = 150Ω	B	25	-	0.04	-	Degrees
	R_L = 75Ω	B	25	-	0.06	-	Degrees
OUTPUT LIMITING CHARACTERISTICS A_V = +2, R_F = 250Ω, V_H = +1V, V_L = -1V, Unless Otherwise Specified							
Limit Accuracy (Note 5)	V_{IN} = ±2V, A_V = -1, R_F = 510Ω	A	Full	-125	25	125	mV
Overdrive Recovery Time (Note 5)	V_{IN} = ±1V	B	25	-	0.8	-	ns
Negative Limit Range		B	25	-5.0 to +2.5			V
Positive Limit Range		B	25	-2.5 to +5.0			V
Limit Input Bias Current		A	25	-	50	200	µA
		A	Full	-	80	200	µA
POWER SUPPLY CHARACTERISTICS							
Power Supply Range		C	25	±4.5	-	±5.5	V
Power Supply Current (Note 5)		A	Full	6.4	6.9	7.3	mA

NOTES:

2. Test Level: A. Production Tested; B. Typical or Guaranteed Limit Based on Characterization; C. Design Typical for Information Only.
3. The optimum feedback resistor for the HFA1135 at A_V = +1 is 1.5kΩ. The Production Tested parameters are tested with R_F = 510Ω because the HFA1135 shares test hardware with the HFA1105 amplifier.
4. Undershoot dominates for output signal swings below GND (e.g., 0.5V_{P-P}), yielding a higher overshoot limit compared to the V_{OUT} = 0V to 0.5V condition. See the “Application Information” section for details.
5. See Typical Performance Curves for more information.
6. Slew rates are asymmetrical if the output swings below GND (e.g., a bipolar signal). Positive unipolar output signals have symmetric positive and negative slew rates comparable to the +SR specification. See the “Application Information” section, and the pulse response graphs for details.

Application Information

Relevant Application Notes

The following Application Notes pertain to the HFA1135:

- AN9653-Use and Application of Output Limiting Amplifiers
- AN9752-Sync Stripper and Sync Inserter for Composite Video
- AN9787-An Intuitive Approach to Understanding Current Feedback Amplifiers
- AN9420-Current Feedback Amplifier Theory and Applications
- AN9663-Converting from Voltage Feedback to Current Feedback Amplifiers

These publications may be obtained from Intersil’s web site (www.intersil.com) or via our AnswerFAX system.

Optimum Feedback Resistor

Although a current feedback amplifier’s bandwidth dependency on closed loop gain isn’t as severe as that of a voltage feedback amplifier, there can be an appreciable decrease in bandwidth at higher gains. This decrease may be minimized by taking advantage of the current feedback amplifier’s unique relationship between bandwidth and R_F. All current feedback amplifiers require a feedback resistor, even for unity gain applications, and R_F, in conjunction with the internal compensation capacitor, sets the dominant pole of the frequency response. Thus, the amplifier’s bandwidth is inversely proportional to R_F. The HFA1135 design is optimized for a 250Ω R_F at a gain of +2. Decreasing R_F decreases stability, resulting in excessive peaking and overshoot (Note: Capacitive feedback will cause the same

problems due to the feedback impedance decrease at higher frequencies). At higher gains the amplifier is more stable, so R_F can be decreased in a trade-off of stability for bandwidth.

The table below lists recommended R_F values, and the expected bandwidth, for various closed loop gains.

TABLE 1. OPTIMUM FEEDBACK RESISTOR

GAIN (A_V)	R_F (Ω)	BANDWIDTH (MHz)
-1	330	290
+1	1.5k	660
+2	250 330	360 315
+5	180	200
+10	250	90

Non-inverting Input Source Impedance

For best operation, the DC source impedance seen by the non-inverting input should be ≥50Ω. This is especially important in inverting gain configurations where the non-inverting input would normally be connected directly to GND.

Pulse Undershoot and Asymmetrical Slew Rates

The HFA1135 utilizes a quasi-complementary output stage to achieve high output current while minimizing quiescent supply current. In this approach, a composite device replaces the traditional PNP pulldown transistor. The composite device switches modes after crossing 0V, resulting in added distortion for signals swinging below ground, and an increased undershoot on the negative portion of the output waveform (see Figures 9, 13, and 17). This undershoot isn't present for small bipolar signals, or large positive signals. Another artifact of the composite device is asymmetrical slew rates for output signals with a negative voltage component. The slew rate degrades as the output signal crosses through 0V (see Figures 9, 13, and 17), resulting in a slower overall negative slew rate. Positive only signals have symmetrical slew rates as illustrated in the large signal positive pulse response graphs (see Figures 7, 11, and 15).

PC Board Layout

This amplifier's frequency response depends greatly on the care taken in designing the PC board. **The use of low inductance components such as chip resistors and chip capacitors is strongly recommended, while a solid ground plane is a must!**

Attention should be given to decoupling the power supplies. A large value (10µF) tantalum in parallel with a small value (0.1µF) chip capacitor works well in most cases.

Terminated microstrip signal lines are recommended at the input and output of the device. Capacitance directly on the output must be minimized, or isolated as discussed in the next section.

Care must also be taken to minimize the capacitance to ground at the amplifier's inverting input (-IN), as this capacitance causes gain peaking, pulse overshoot, and if large enough, instability. To reduce this capacitance, the designer should remove the ground plane under traces connected to -IN, and keep connections to -IN as short as possible.

An example of a good high frequency layout is the Evaluation Board shown in Figure 2.

Driving Capacitive Loads

Capacitive loads, such as an A/D input, or an improperly terminated transmission line degrade the amplifier's phase margin resulting in frequency response peaking and possible oscillations. In most cases, the oscillation can be avoided by placing a resistor (R_S) in series with the output prior to the capacitance.

Figure 1 details starting points for the selection of this resistor. The points on the curve indicate the R_S and C_L combinations for the optimum bandwidth, stability, and settling time, but experimental fine tuning is recommended. Picking a point above or to the right of the curve yields an overdamped response, while points below or left of the curve indicate areas of underdamped performance.

R_S and C_L form a low pass network at the output, thus limiting system bandwidth well below the amplifier bandwidth of 660MHz (A_V = +1). By decreasing R_S as C_L increases (as illustrated by the curves), the maximum bandwidth is obtained without sacrificing stability. In spite of this, bandwidth still decreases as the load capacitance increases. For example, at A_V = +1, R_S = 50Ω, C_L = 20pF, the overall bandwidth is 170MHz, but the bandwidth drops to 45MHz at A_V = +1, R_S = 10Ω, C_L = 330pF.

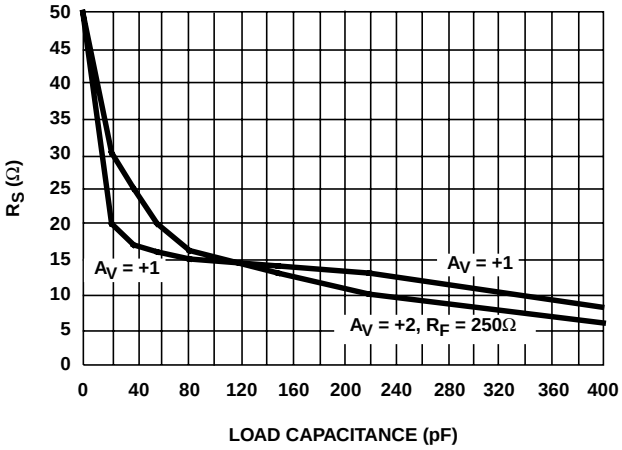


FIGURE 1. RECOMMENDED SERIES RESISTOR vs LOAD CAPACITANCE

Evaluation Board

The performance of the HFA1135 may be evaluated using the HFA11XX evaluation board (part number HFA11XXEVAL). Please contact your local sales office for information. When evaluating this amplifier at a gain of +2, the two 510Ω gain setting resistors on the evaluation board should be changed to 250Ω.

The layout and schematic of the board are shown in Figure 2.

NOTE: The SOIC version may be evaluated in the DIP board by using a SOIC-to-DIP adapter such as Aries Electronics part number 08-350000-10.

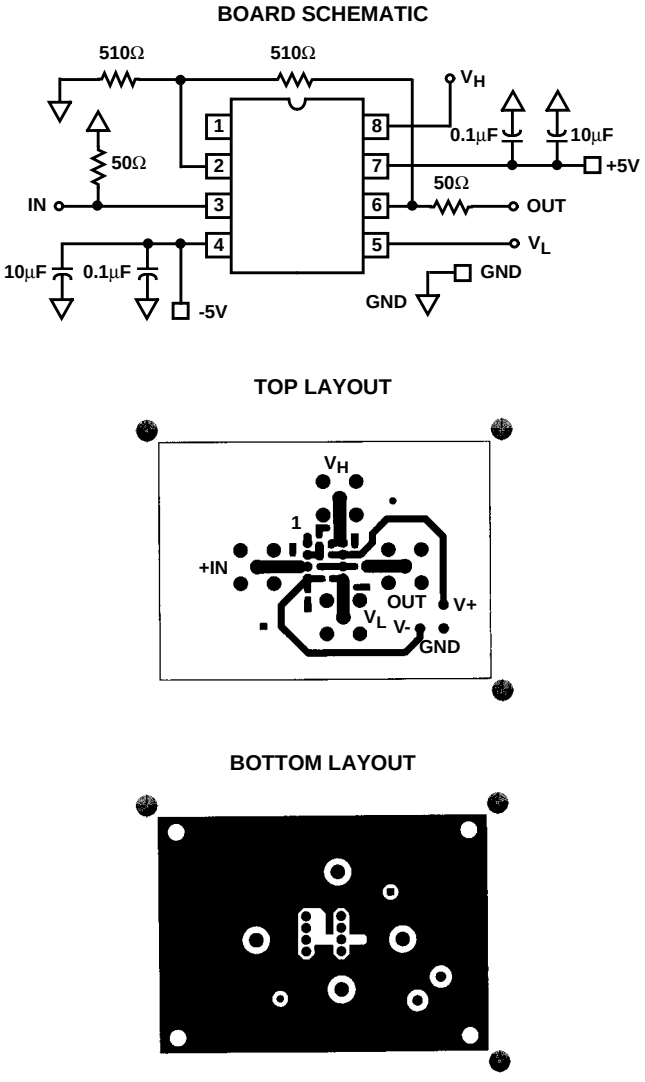


FIGURE 2. EVALUATION BOARD SCHEMATIC AND LAYOUT

Limiting Operation

General

The HFA1135 features user programmable output clamps to limit output voltage excursions. Limiting action is obtained by applying voltages to the V_H and V_L terminals (pins 8 and 5) of the amplifier. V_H sets the upper output limit, while V_L sets the lower limit level. If the amplifier tries to drive the output above V_H, or below V_L, the clamp circuitry limits the output voltage at V_H or V_L (± the limit accuracy), respectively. The low input bias currents of the limit pins allow them to be driven by simple resistive divider circuits, or active elements such as amplifiers or DACs.

Limit Circuitry

Figure 3 shows a simplified schematic of the HFA1135 input stage, and the high limit (V_H) circuitry. As with all current feedback amplifiers, there is a unity gain buffer (Q_{X1} - Q_{X2}) between the positive and negative inputs. This buffer forces -IN to track +IN, and sets up a slewing current of:

$$I_{SLEW} = (V_{-IN} - V_{OUT})/R_F + V_{-IN}/R_G$$

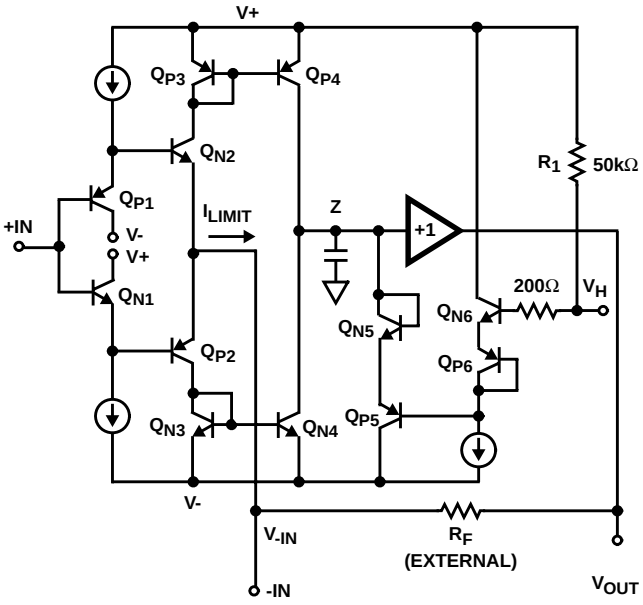


FIGURE 3. HFA1135 SIMPLIFIED V_H LIMIT CIRCUITRY

This current is mirrored onto the high impedance node (Z) by Q_{X3}-Q_{X4}, where it is converted to a voltage and fed to the output via another unity gain buffer. If no limiting is utilized, the high impedance node may swing within the limits defined by Q_{P4} and Q_{N4}. Note that when the output reaches its quiescent value, the current flowing through -IN is reduced to only that small current ($-I_{BIAS}$) required to keep the output at the final voltage.

Tracing the path from V_H to Z illustrates the effect of the limit voltage on the high impedance node. V_H decreases by $2V_{BE}$ (Q_{N6} and Q_{P6}) to set up the base voltage on Q_{P5}. Q_{P5} begins to conduct whenever the high impedance node reaches a voltage equal to Q_{P5}'s base voltage + $2V_{BE}$ (Q_{P5} and Q_{N5}). Thus, Q_{P5} limits node Z whenever Z reaches V_H. R_1 provides a pull-up network to ensure functionality with the limit inputs floating. A similar description applies to the symmetrical low limit circuitry controlled by V_L.

When the output is limited, the negative input continues to source a slewing current (I_{LIMIT}) in an attempt to force the output to the quiescent voltage defined by the input. Q_{P5} must sink this current while limiting, because the -IN current is always mirrored onto the high impedance node. The limiting current is calculated as:

$$I_{LIMIT} = (V_{-IN} - V_{OUT\ LIMITED})/R_F + V_{-IN}/R_G.$$

As an example, a unity gain circuit with V_{IN} = 2V, and V_H = 1V, would have I_{LIMIT} = (2V - 1V)/1.5kΩ + 2V/∞ = 667µA ($R_G = \infty$ for unity gain applications). Note that I_{CC} increases by I_{LIMIT} when the output is limited.

Limit Accuracy

The limited output voltage will not be exactly equal to the voltage applied to V_H or V_L. Offset errors, mostly due to VBE mismatches, necessitate a limit accuracy parameter which is found in the device specifications. Limit accuracy is a function of the limiting conditions. Referring again to Figure 3, it can be seen that one component of limit accuracy is the V_{BE} mismatch between the Q_{X6} transistors, and the Q_{X5} transistors. If the transistors always ran at the same current level there would be no V_{BE} mismatch, and no contribution to the inaccuracy. The Q_{X6} transistors are biased at a constant current, but as described earlier, the current through Q_{X5} is equivalent to I_{LIMIT}. V_{BE} increases as I_{LIMIT} increases, causing the limited output voltage to increase as well. I_{LIMIT} is a function of the overdrive level ($(A_V \times V_{IN} - V_{LIMIT}) / V_{LIMIT}$), so limit accuracy degrades as the overdrive increases. For example, accuracy degrades from +15mV to +70mV when the overdrive increases from 100% to 200% (A_V = +2, V_H = 500mV, R_F = 250Ω).

Consideration must also be given to the fact that the limit voltages have an effect on amplifier linearity. The “Linearity Near Limit Voltage” curves, Figures 34 and 35, illustrate the impact of several limit levels on linearity.

Limit Range

Unlike some competitor devices, both V_H and V_L have usable ranges that cross 0V. While V_H must be more positive than V_L, both may be positive or negative, within the range restrictions indicated in the specifications. For example, the HFA1135 could be limited to ECL output levels by setting V_H = -0.8V and V_L = -1.8V. V_H and V_L may be connected to the same voltage (GND for instance) but the result won’t be a DC output voltage from an AC input signal. A 150mV - 200mV AC signal will still be present at the output.

Recovery from Overdrive

The output voltage remains at the limit level as long as the overdrive condition remains. When the input voltage drops below the overdrive level (V_{LIMIT}/A_V) the amplifier returns to linear operation. A time delay, known as the Overdrive Recovery Time, is required for this resumption of linear operation. Overdrive recovery time is defined as the difference between the amplifier’s propagation delay exiting limiting and the amplifier’s normal propagation delay, and it is a strong function of the overdrive level. Figure 36 details the overdrive recovery time for various limit and overdrive levels.

Benefits of Output Limiting

The plots of “Pulse Response Without Limiting” and “Pulse Response With Limiting” (Figures 4 and 5) highlight the advantages of output limiting. Besides the obvious benefit of constraining the output swing to a defined range, limiting the output excursions also keeps the output transistors from saturating, which prevents unwanted saturation artifacts from distorting the output signal. Output limiting also takes advantage of the HFA1135’s ultra-fast overdrive recovery time, reducing the recovery time from 2.3ns to 0.3ns, based on the amplifier’s normal propagation delay of 1.2ns.

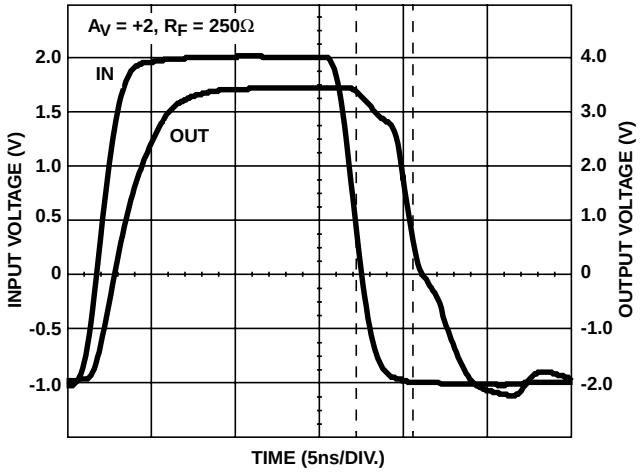


FIGURE 4. PULSE RESPONSE WITHOUT LIMITING

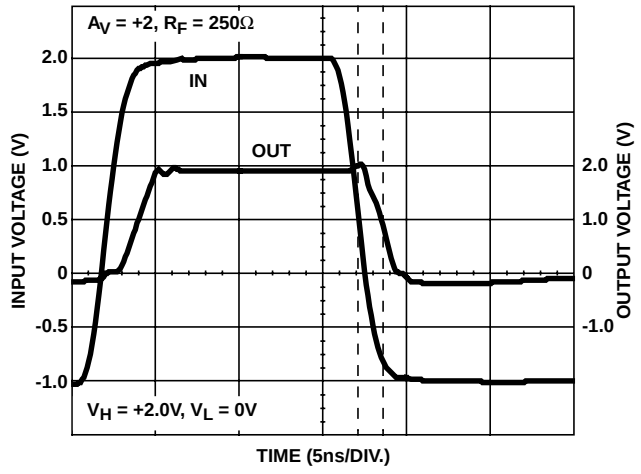


FIGURE 5. PULSE RESPONSE WITH LIMITING

Typical Performance Curves

V_{SUPPLY} = ±5V, T_A = 25°C, R_F = Value From the Optimum Feedback Resistor Table, R_L = 100Ω, Unless Otherwise Specified

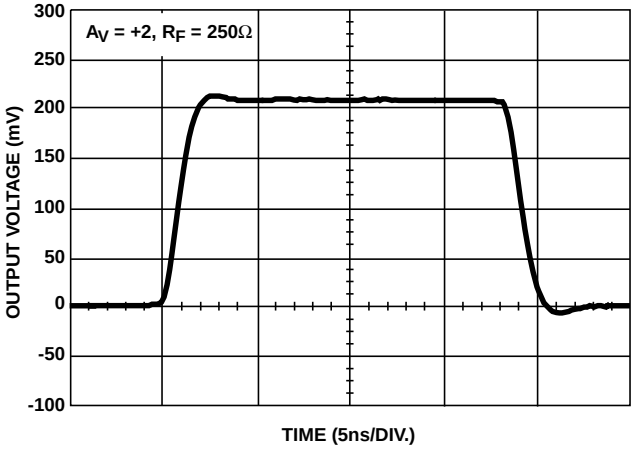


FIGURE 6. SMALL SIGNAL POSITIVE PULSE RESPONSE

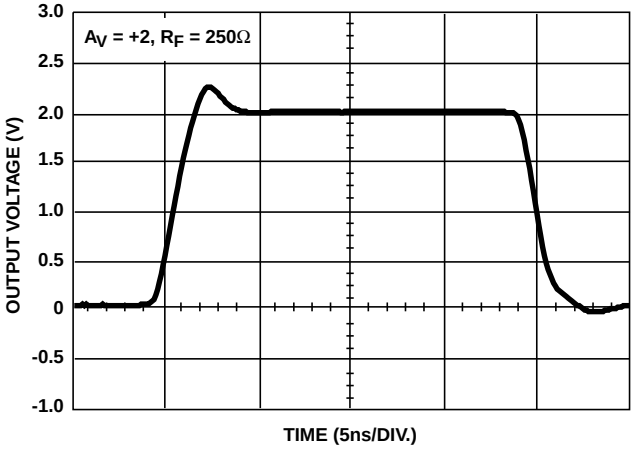


FIGURE 7. LARGE SIGNAL POSITIVE PULSE RESPONSE

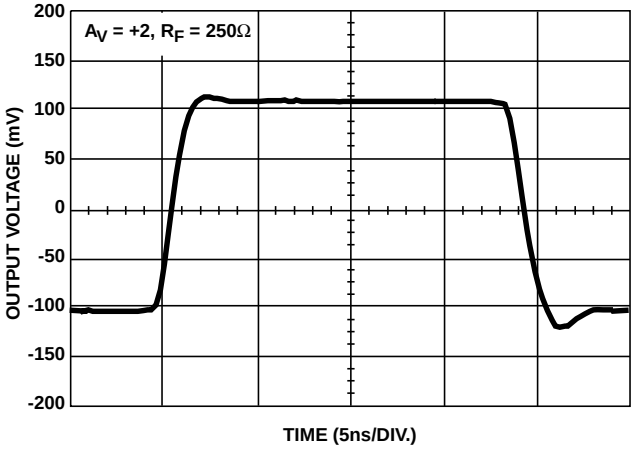


FIGURE 8. SMALL SIGNAL BIPOLAR PULSE RESPONSE

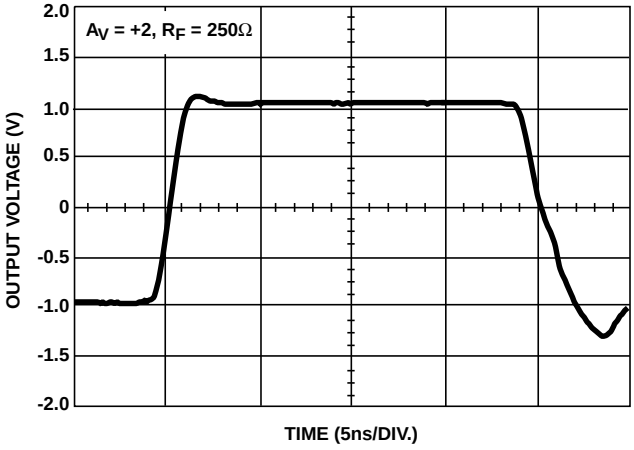


FIGURE 9. LARGE SIGNAL BIPOLAR PULSE RESPONSE

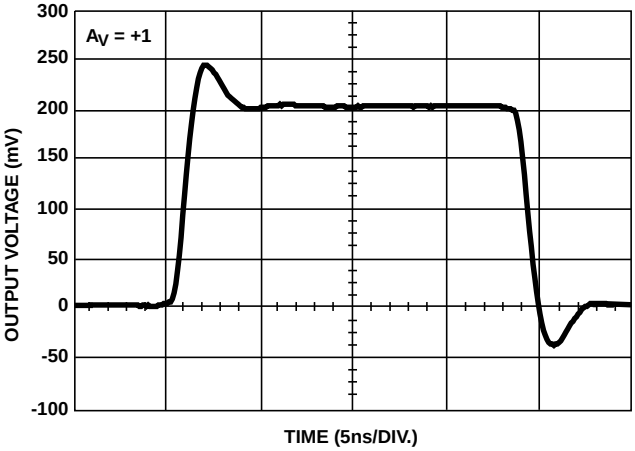


FIGURE 10. SMALL SIGNAL POSITIVE PULSE RESPONSE

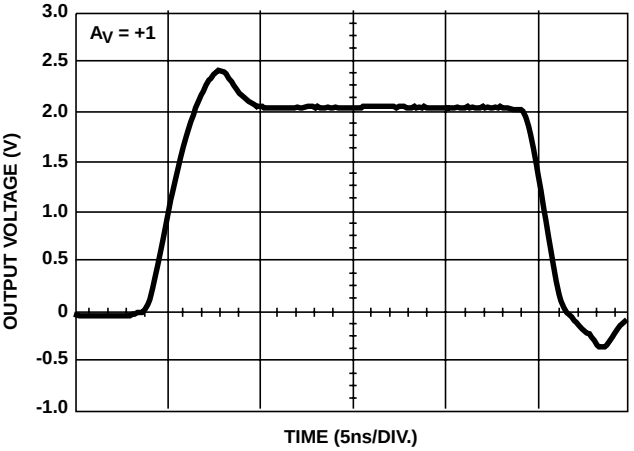


FIGURE 11. LARGE SIGNAL POSITIVE PULSE RESPONSE

Typical Performance Curves

V_{SUPPLY} = ±5V, T_A = 25°C, R_F = Value From the Optimum Feedback Resistor Table, R_L = 100Ω, Unless Otherwise Specified **(Continued)**

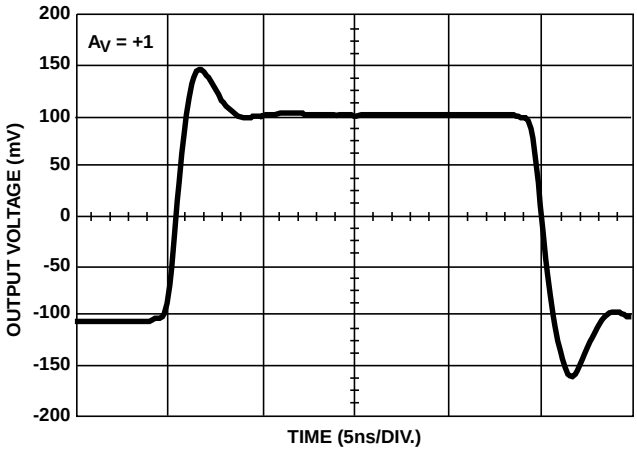


FIGURE 12. SMALL SIGNAL BIPOLAR PULSE RESPONSE

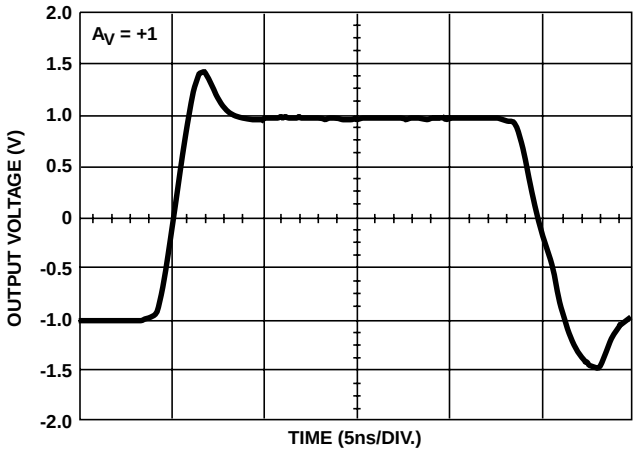


FIGURE 13. LARGE SIGNAL BIPOLAR PULSE RESPONSE

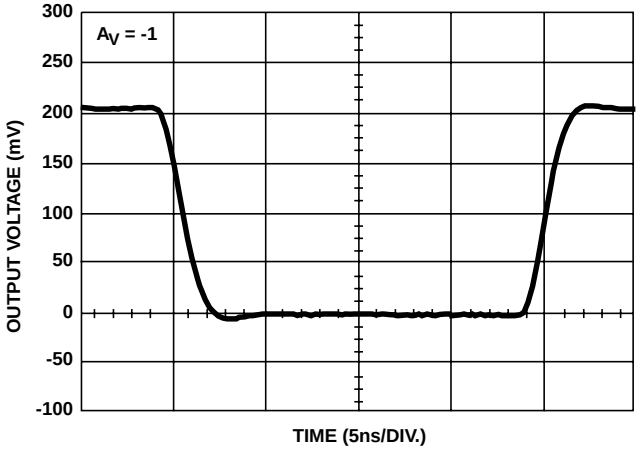


FIGURE 14. SMALL SIGNAL POSITIVE PULSE RESPONSE

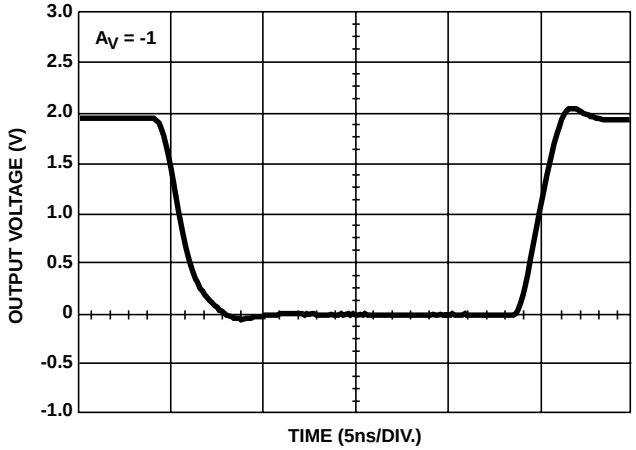


FIGURE 15. LARGE SIGNAL POSITIVE PULSE RESPONSE

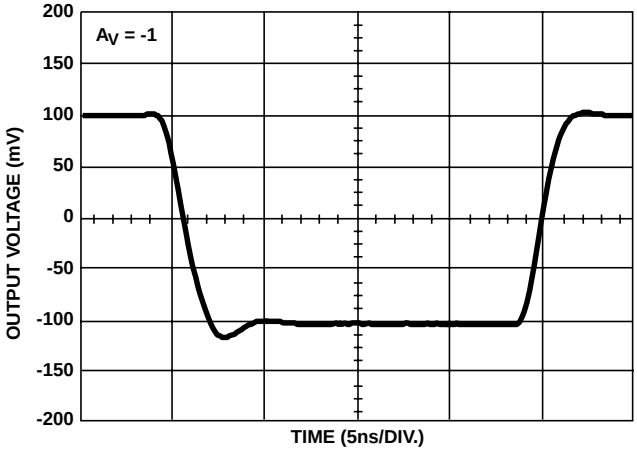


FIGURE 16. SMALL SIGNAL BIPOLAR PULSE RESPONSE

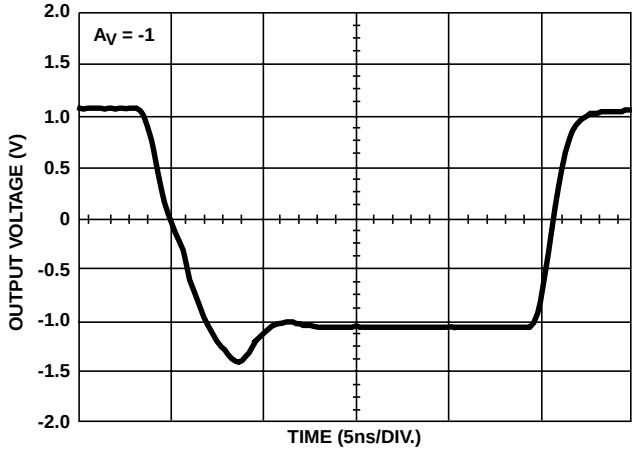


FIGURE 17. LARGE SIGNAL BIPOLAR PULSE RESPONSE

Typical Performance Curves

V_{SUPPLY} = ±5V, T_A = 25°C, R_F = Value From the Optimum Feedback Resistor Table, R_L = 100Ω, Unless Otherwise Specified **(Continued)**

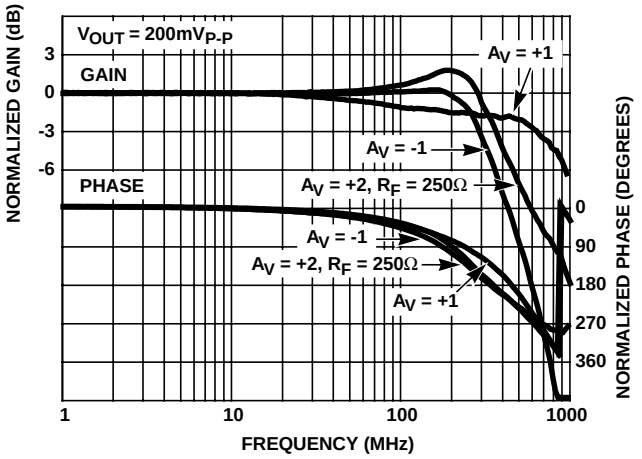


FIGURE 18. FREQUENCY RESPONSE

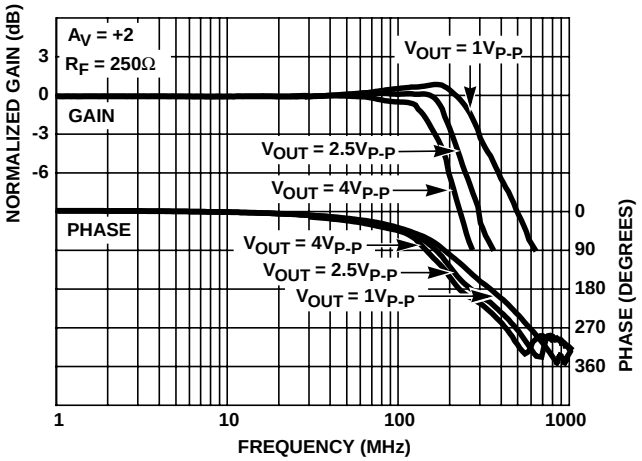


FIGURE 19. FREQUENCY RESPONSE FOR VARIOUS OUTPUT VOLTAGES

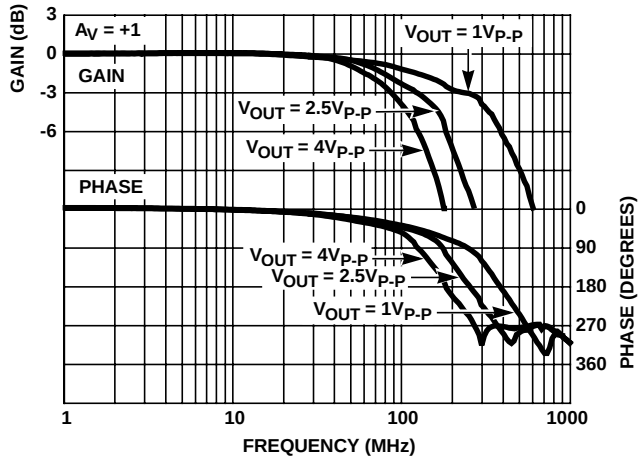


FIGURE 20. FREQUENCY RESPONSE FOR VARIOUS OUTPUT VOLTAGES

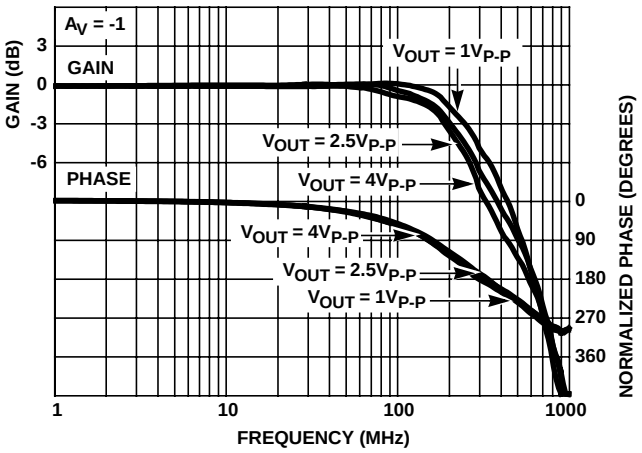


FIGURE 21. FREQUENCY RESPONSE FOR VARIOUS OUTPUT VOLTAGES

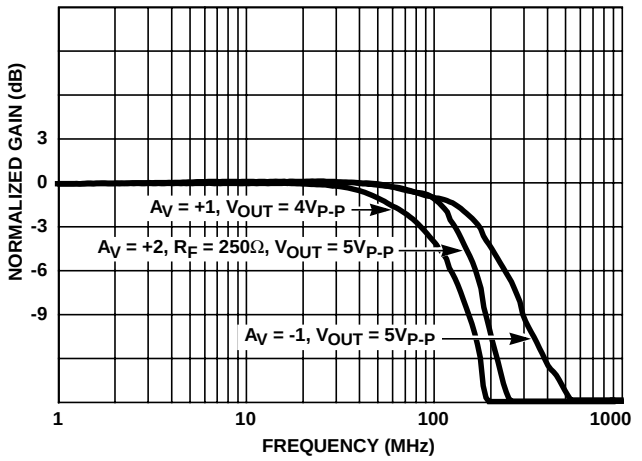


FIGURE 22. FULL POWER BANDWIDTH

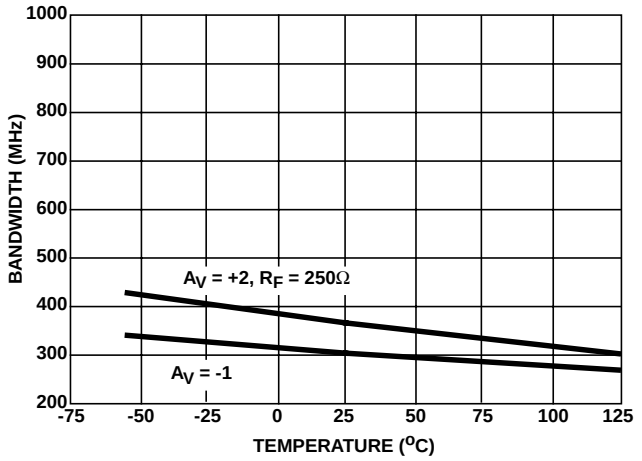


FIGURE 23. -3dB BANDWIDTH vs TEMPERATURE

Typical Performance Curves $V_{SUPPLY} = \pm5V$, $T_A = 25^oC$, R_F = Value From the Optimum Feedback Resistor Table, $R_L = 100\Omega$, Unless Otherwise Specified **(Continued)**

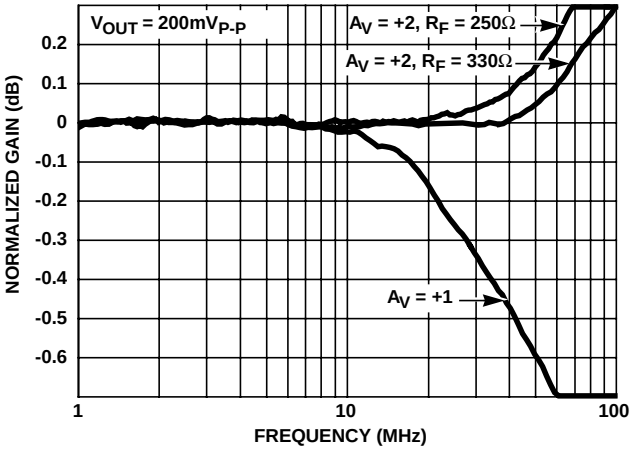


FIGURE 24. GAIN FLATNESS

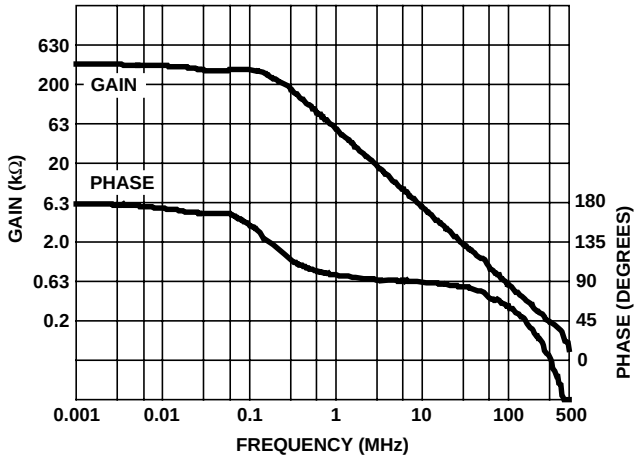


FIGURE 25. OPEN LOOP TRANSIMPEDANCE

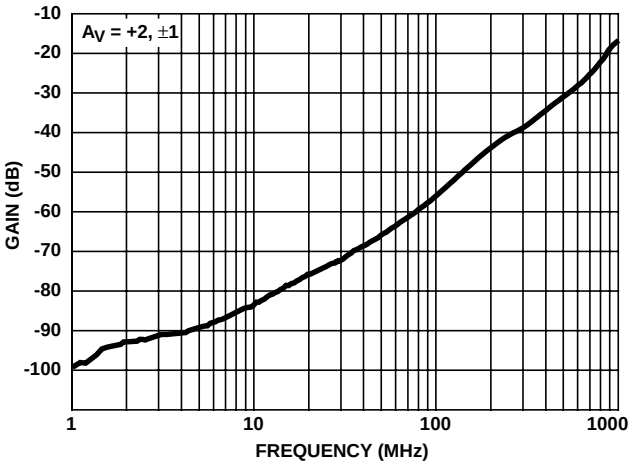


FIGURE 26. REVERSE ISOLATION

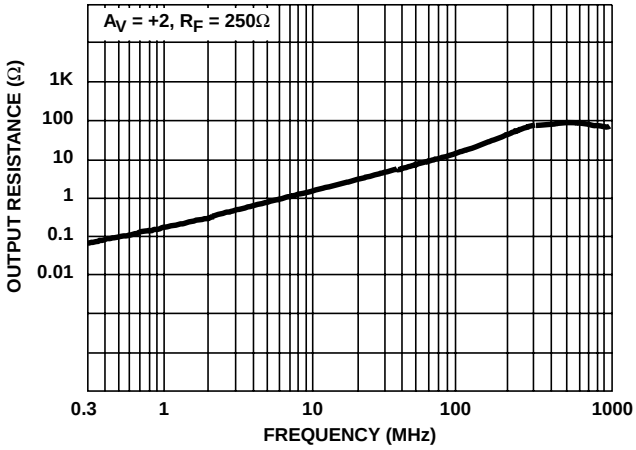


FIGURE 27. OUTPUT RESISTANCE

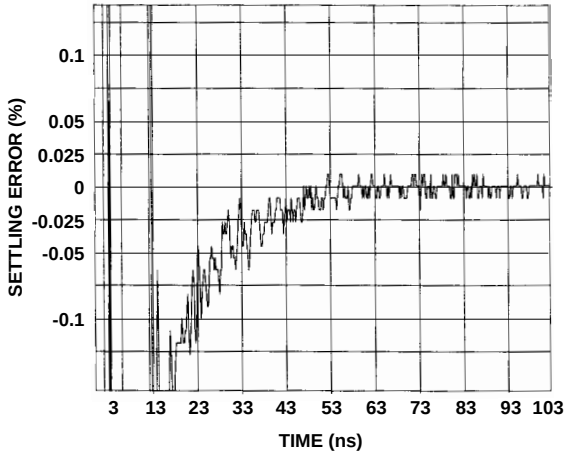


FIGURE 28. SETTLING TIME RESPONSE

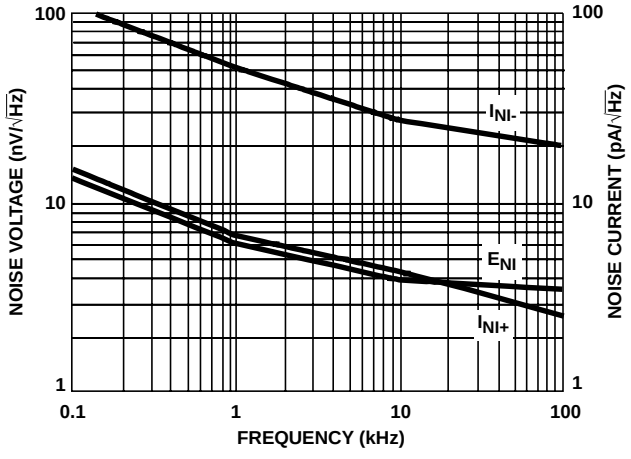


FIGURE 29. INPUT NOISE CHARACTERISTICS

Typical Performance Curves

V_{SUPPLY} = ±5V, T_A = 25°C, R_F = Value From the Optimum Feedback Resistor Table, R_L = 100Ω, Unless Otherwise Specified **(Continued)**

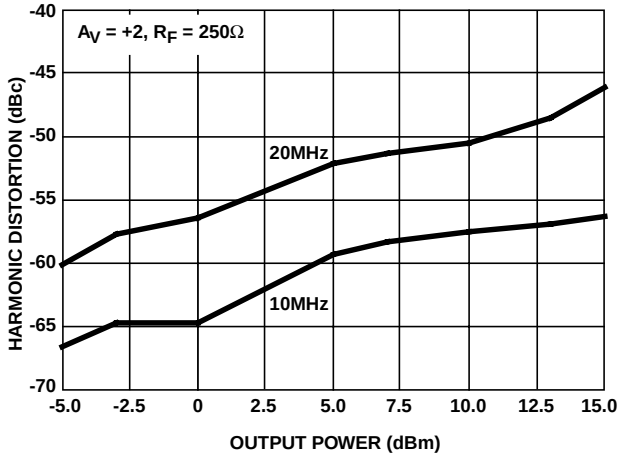


FIGURE 30. 2nd HARMONIC DISTORTION vs P_{OUT}

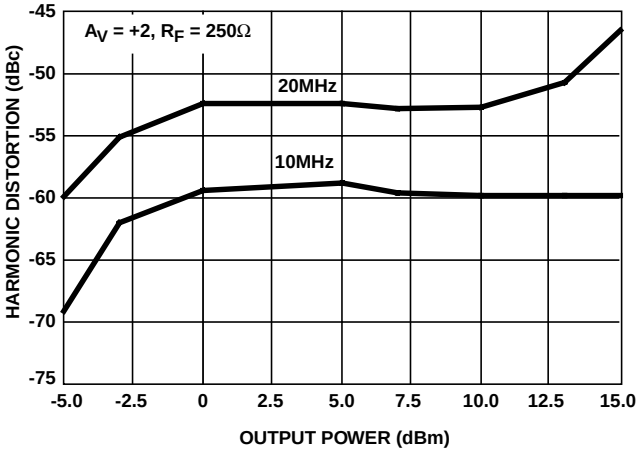


FIGURE 31. 3rd HARMONIC DISTORTION vs P_{OUT}

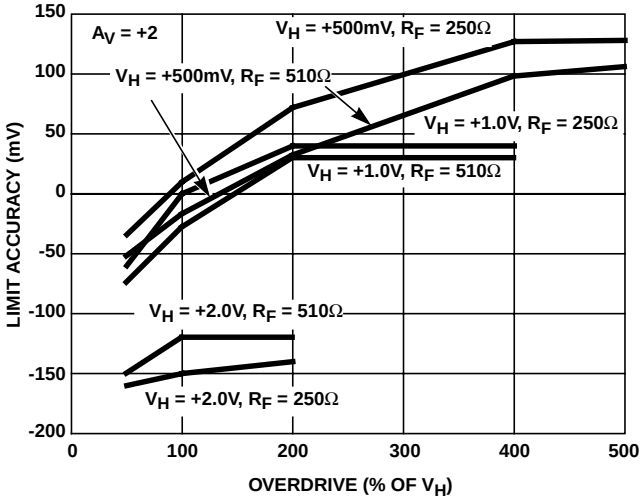


FIGURE 32. V_H LIMIT ACCURACY vs OVERDRIVE

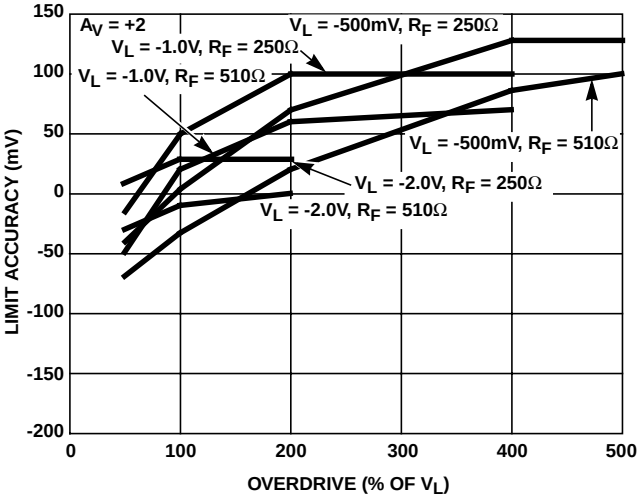


FIGURE 33. V_L LIMIT ACCURACY vs OVERDRIVE

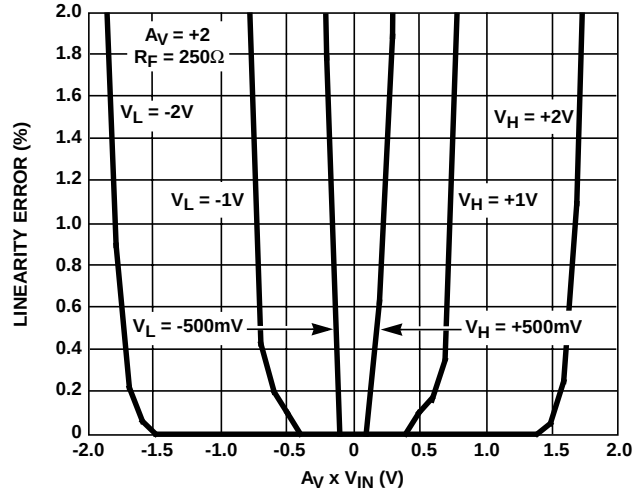


FIGURE 34. LINEARITY NEAR LIMIT VOLTAGE

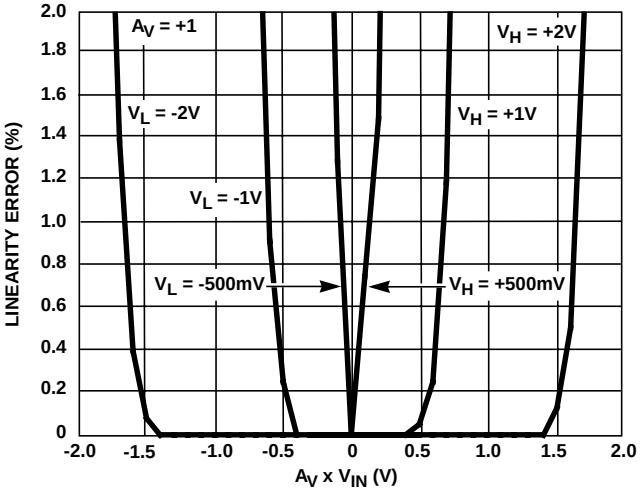


FIGURE 35. LINEARITY NEAR LIMIT VOLTAGE

Typical Performance Curves

$V_{SUPPLY} = \pm5V$, $T_A = 25^oC$, R_F = Value From the Optimum Feedback Resistor Table, $R_L = 100\Omega$, Unless Otherwise Specified **(Continued)**

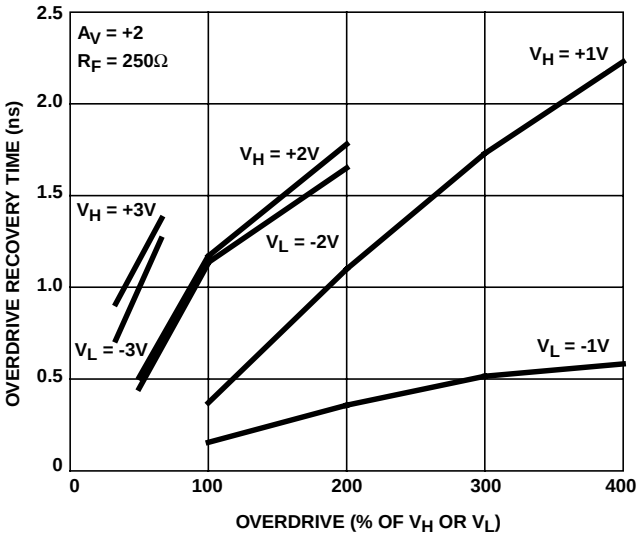


FIGURE 36. OVERDRIVE RECOVERY TIME vs OVERDRIVE

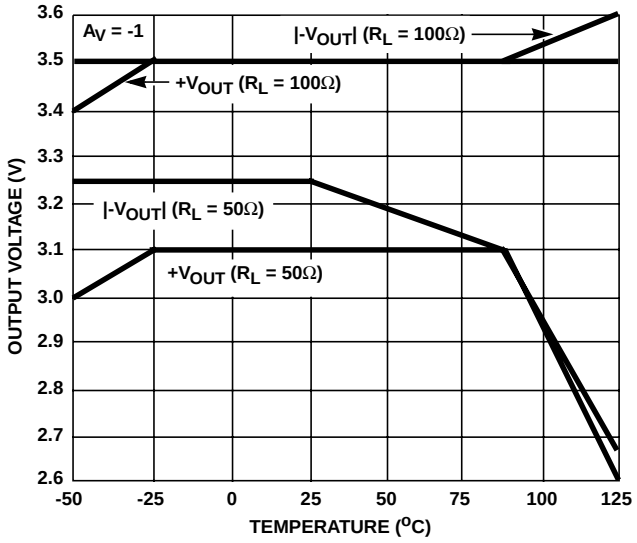


FIGURE 37. OUTPUT VOLTAGE vs TEMPERATURE

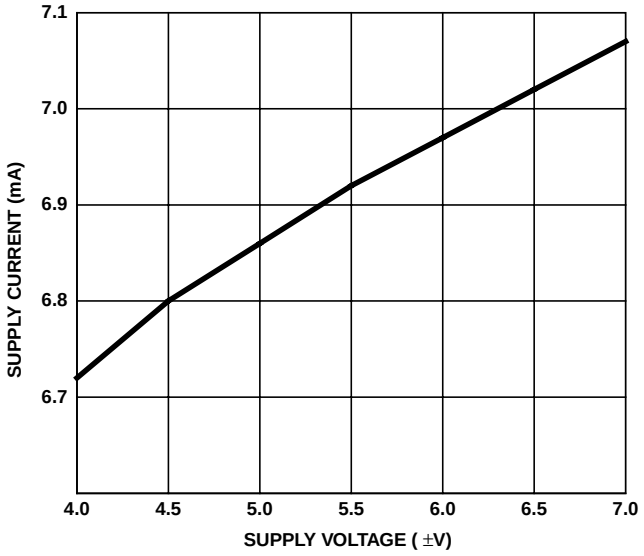


FIGURE 38. SUPPLY CURRENT vs SUPPLY VOLTAGE

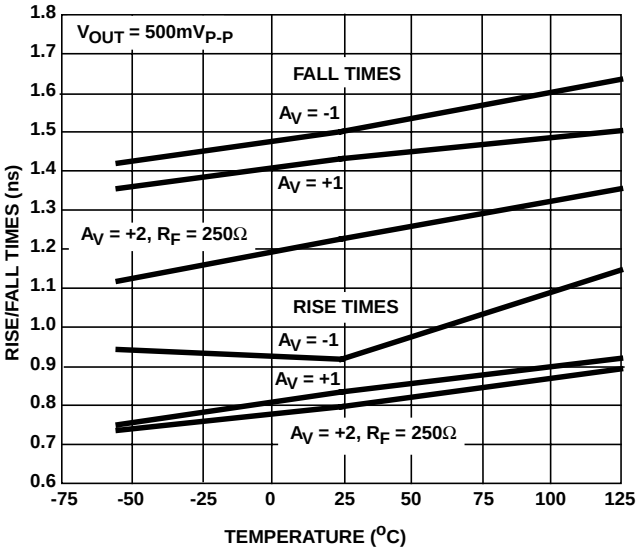


FIGURE 39. RISE AND FALL TIMES vs TEMPERATURE

Die Characteristics

DIE DIMENSIONS

59 mils x 58.2 mils x 19 mils
1500µm x 1480µm x 483µm

METALLIZATION

Type: Metal 1: AICu(2%)/TiW
Thickness: Metal 1: 8kÅ ±0.4kÅ
Type: Metal 2: AICu(2%)
Thickness: Metal 2: 16kÅ ±0.8kÅ

SUBSTRATE POTENTIAL (POWERED UP)

Floating (Recommend Connection to V-)

PASSIVATION

Type: Nitride
Thickness: 4kÅ ±0.5kÅ

TRANSISTOR COUNT

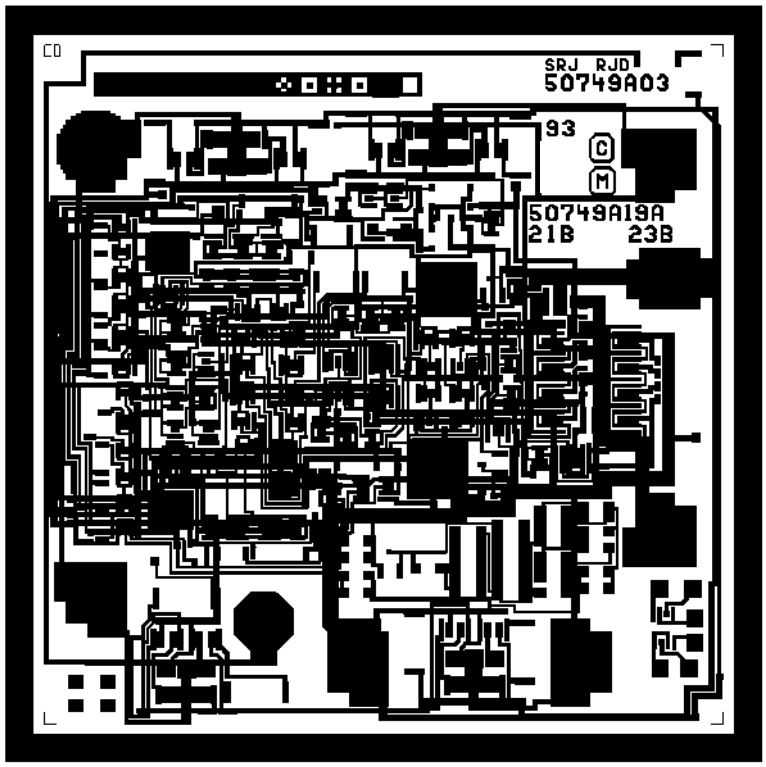
89

PROCESS

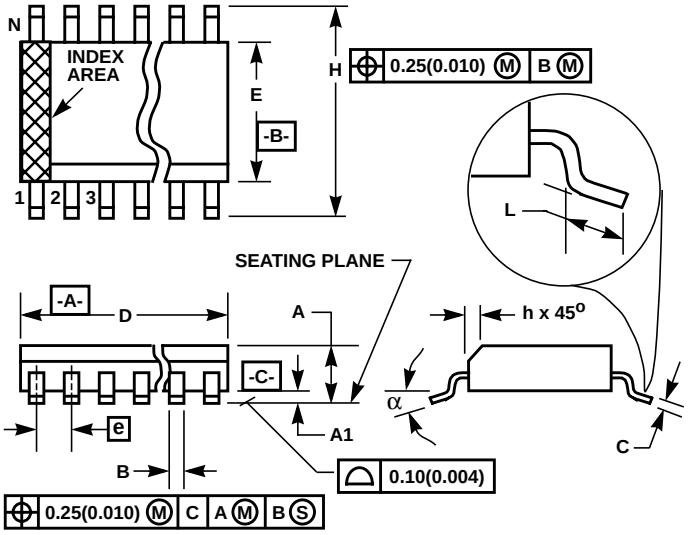
Bipolar Dielectric Isolation

Metallization Mask Layout

HFA1135



Small Outline Plastic Packages (SOIC)



NOTES:

1. Symbols are defined in the “MO Series Symbol List” in Section 2.2 of Publication Number 95.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Dimension “D” does not include mold flash, protrusions or gate burrs. Mold flash, protrusion and gate burrs shall not exceed 0.15mm (0.006 inch) per side.
4. Dimension “E” does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.25mm (0.010 inch) per side.
5. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
6. “L” is the length of terminal for soldering to a substrate.
7. “N” is the number of terminal positions.
8. Terminal numbers are shown for reference only.
9. The lead width “B”, as measured 0.36mm (0.014 inch) or greater above the seating plane, shall not exceed a maximum value of 0.61mm (0.024 inch).
10. Controlling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact.

M8.15 (JEDEC MS-012-AA ISSUE C)
8 LEAD NARROW BODY SMALL OUTLINE PLASTIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.0532	0.0688	1.35	1.75	-
A1	0.0040	0.0098	0.10	0.25	-
B	0.013	0.020	0.33	0.51	9
C	0.0075	0.0098	0.19	0.25	-
D	0.1890	0.1968	4.80	5.00	3
E	0.1497	0.1574	3.80	4.00	4
e	0.050 BSC		1.27 BSC		-
H	0.2284	0.2440	5.80	6.20	-
h	0.0099	0.0196	0.25	0.50	5
L	0.016	0.050	0.40	1.27	6
N	8		8		7
α	0^o	8^o	0^o	8^o	-

Rev. 0 12/93

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