

# OKI Semiconductor

## MSM7578H/7578V/7579

### Single Rail CODEC

#### GENERAL DESCRIPTION

The MSM7578 and MSM7579 are single-channel CODEC CMOS ICs for voice signals ranging from 300 to 3400 Hz. These devices contain filters for A/D and D/A conversion.

Designed especially for a single-power supply and low-power applications, these devices are particularly optimized for telephone terminals in digital wireless systems and ISDN systems. The devices use the same transmission clocks as those used in the MSM7508B and MSM7509B. The analog output signal can directly drive a piezoelectric type handset receiver.

#### FEATURES

- Single power supply:  $+5.0\text{ V} \pm 5\%$

- Low power consumption

Operating mode: 25 mW Typ. 47 mW Max.  $V_{DD} = 5\text{ V}$

Power down mode: 0.05 mW Typ. 0.3 mW Max.  $V_{DD} = 5\text{ V}$

- ITU-T Companding law

MSM7578H:  $\mu$ -law

MSM7579: A-law

MSM7578V:  $\mu$ /A-law pin-selectable

- Built-in PLL eliminates a master clock

- Serial data rate: 64/128/256/512/1024/2048 kHz  
96/192/384/768/1536/1544/200 kHz

- Adjustable transmit gain

- Built-in reference voltage supply

- Directly drive a line transformer of  $600\text{ }\Omega$

- The 16-pin DIP and 24-pin SOP package products provide pin compatibility with the MSM7508B/7509B

- The 20-pin SSOP package products have 1/3 the foot print of conventional products

- Package options:

16-pin plastic DIP (DIP16-P-300-2.54)

(Product name : MSM7578HRS)

(Product name : MSM7579RS)

(Product name : MSM7578VRS)

24-pin plastic SOP (SOP24-P-430-1.27-K)

(Product name : MSM7578HGS-K)

(Product name : MSM7578VGS-K)

(Product name : MSM7579GS-K)

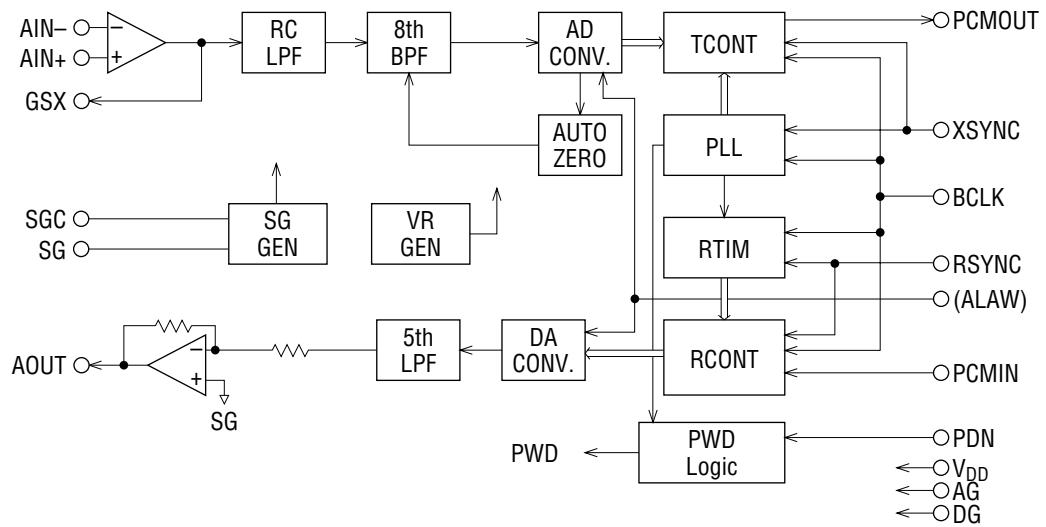
20-pin plastic SSOP (SSOP20-P-250-0.95-K)

(Product name : MSM7578HMS-K)

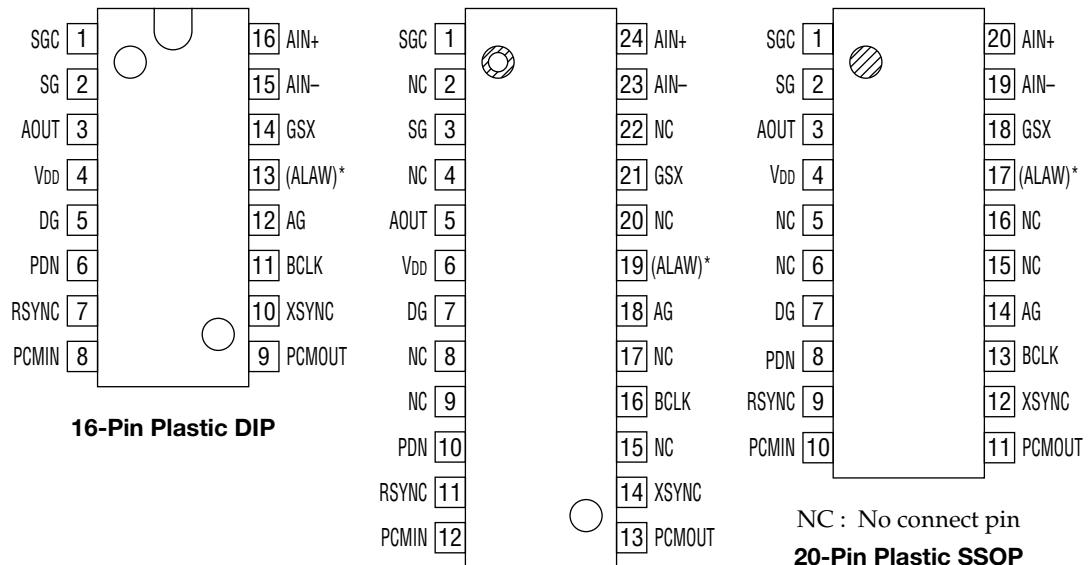
(Product name : MSM7579MS-K)

(Product name : MSM7578VMS-K)

## BLOCK DIAGRAM



## PIN CONFIGURATION (TOP VIEW)



NC : No connect pin

**24-Pin Plastic SOP**

\* The ALAW pin is only applied to the MSM7578VRS/MSM7578VGS-K/MSM7578VMS-K.

## PIN AND FUNCTIONAL DESCRIPTIONS

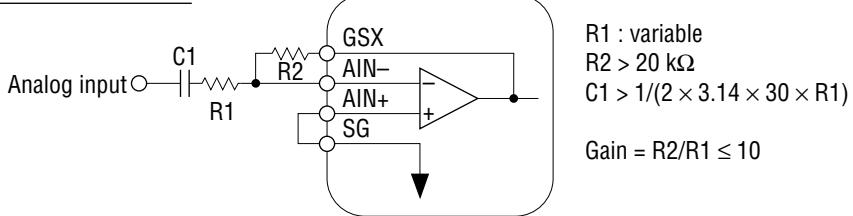
### AIN+, AIN-, GSX

Transmit analog input and transmit level adjustment.

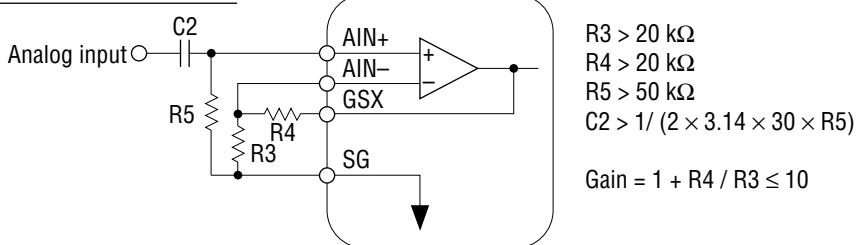
AIN+ is a non-inverting input to the op-amp; AIN- is an inverting input to the op-amp; GSX is connected to the output of the op-amp and is used to adjust the level, as shown below.

When not using AIN- and AIN+, connect AIN- to GSX and AIN+ to SG. During power saving and power down modes, the GSX output is at AG voltage.

#### 1) Inverting input type



#### 2) Non inverting input type



### AG

Analog signal ground.

### AOUT

Analog output.

The output signal has a maximum amplitude of 2.4 V<sub>PP</sub> above and below the signal ground voltage (V<sub>DD</sub>/2).

The output load resistance is a minimum of 600 Ω.

During power saving, or power down mode, the output of AOUT is at the voltage level of the signal ground.

**V<sub>DD</sub>**

Power supply for +5 V.

**PCM<sub>IN</sub>**

PCM signal input.

A serial PCM signal input to this pin is converted to an analog signal in synchronization with the RSYNC signal and BCLK signal.

The data rate of the PCM signal is equal to the frequency of the BCLK signal.

The PCM signal is shifted at a falling edge of the BCLK signal and latched into the internal register when shifted by eight bits.

The start of the PCM data (MSD) is identified at the rising edge of RSYNC.

**BCLK**

Shift clock signal input for the PCM<sub>IN</sub> and PCM<sub>OUT</sub> signal.

The frequency, equal to the data rate, is 64, 96, 128, 192, 256, 384, 512, 768, 1024, 1536, 1544, 2048, or 200 kHz. Setting this signal to logic "1" or "0" drives both transmit and receive circuits to the power saving state.

**RSYNC**

Receive synchronizing signal input.

Eight required bits are selected from serial PCM signals on the PCM<sub>IN</sub> pin by the receive synchronizing signal.

Signals in the receive section are synchronized by this synchronizing signal. This signal must be synchronized in phase with the BCLK. The frequency should be  $8\text{ kHz} \pm 50\text{ ppm}$  to guarantee the AC characteristics which are mainly the frequency characteristics of the receive section.

However, if the frequency characteristic of an applied system is not specified exactly, this device can operate in the range of  $8\text{ kHz} \pm 2\text{ kHz}$ , but the electrical characteristics in this specification are not guaranteed.

**XSYNC**

Transmit synchronizing signal input.

The PCM output signal from the PCM<sub>OUT</sub> pin is output in synchronization with this transmit synchronizing signal. This synchronizing signal triggers the PLL and synchronizes all timing signals of the transmit section.

This synchronizing signal must be synchronized in phase with BCLK.

The frequency should be  $8\text{ kHz} \pm 50\text{ ppm}$  to guarantee the AC characteristics which are mainly the frequency characteristics of the transmit section.

However, if the frequency characteristic of an applied system is not specified exactly, this device can operate in the range of  $8\text{ kHz} \pm 2\text{ kHz}$ , but the electrical characteristics in this specification are not guaranteed.

Setting this signal to logic "1" or "0" drives both transmit and receive circuits to the power saving state.

DG

Ground for the digital signal circuits.

This ground is separate from the analog signal ground. The DG pin must be connected to the AG pin on the printed circuit board to make a common analog ground.

PDN

Power down control signal.

A logic "0" level drives both transmit and receive circuits to a power down state.

## PCMOUT

PCM signal output.

The PCM output signal is output from MSD in a sequential order, synchronizing with the rising edge of the BCLK signal.

MSD may be output at the rising edge of the XSYNC signal, based on the timing between BCLK and XSYNC.

This pin is in a high impedance state except during 8-bit PCM output. It is also in a high impedance state during power saving or power down mode.

A pull-up resistor must be connected to this pin because its output is configured as an open drain. This device is compatible with the ITU-T recommendation on coding law and output coding format.

The MSM7579 (A-law) outputs the character signal, inverting the even bits

**SG**

Signal ground voltage output.

The output voltage is 1/2 of the power supply voltage.

The output drive current capability is  $\pm 300 \mu A$ .

This pin provides the SG level for CODEC peripherals.

This output voltage level is undefined during power saving or power down mode.

**SGC**

Used to generate the signal ground voltage level by connecting a bypass capacitor.

Connect a  $0.1 \mu F$  capacitor with excellent high frequency characteristics between the AG pin and the SGC pin.

**ALAW**

Control signal input of the companding law selection.

Provides only for the MSM7578VRS/7578VGS-K/7578VMS-K. The CODEC will operate in the  $\mu$ -law when this pin is at a logic "0" level and the CODEC will operate in the A-law when this pin is at a logic "1" level. The CODEC operates in the  $\mu$ -law if the pin is left open, since the pin is internally pulled down.

## ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Condition	Rating		Unit
Power Supply Voltage	$V_{DD}$	—	0 to 7		V
Analog Input Voltage	$V_{AIN}$	—	−0.3 to $V_{DD}$ + 0.3		V
Digital Input Voltage	$V_{DIN}$	—	−0.3 to $V_{DD}$ + 0.3		V
Storage Temperature	$T_{STG}$	—	−55 to +150		°C

## RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Power Supply Voltage	$V_{DD}$	Voltage must be fixed	4.75	5	5.25	V
Operating Temperature	$T_a$	—	−30	+25	+85	°C
Analog Input Voltage	$V_{AIN}$	Connect AIN− and GSX	—	—	2.4	$V_{PP}$
Input High Voltage	$V_{IH}$	XSYNC, RSYNC, BCLK, PCMIN, PDN, ALAW	2.2	—	$V_{DD}$	V
Input Low Voltage	$V_{IL}$		0	—	0.8	V
Clock Frequency	$f_C$	BCLK	64, 128, 256, 512, 1024, 2048, 96, 192, 384, 768, 1536, 1544, 200			kHz
Sync Pulse Frequency	$f_S$	XSYNC, RSYNC	6.0	8.0	9.0	kHz
Clock Duty Ratio	$D_C$	BCLK	40	50	60	%
Digital Input Rise Time	$t_{IR}$	XSYNC, RSYNC, BCLK, PCMIN, PDN, ALAW	—	—	50	ns
Digital Input Fall Time	$t_{IF}$		—	—	50	ns
Transmit Sync Pulse Setting Time	$t_{XS}$	BCLK→XSYNC, See Timing Diagram	100	—	—	ns
	$t_{SX}$	XSYNC→BCLK, See Timing Diagram	100	—	—	ns
Receive Sync Pulse Setting Time	$t_{RS}$	BCLK→RSYNC, See Timing Diagram	100	—	—	ns
	$t_{SR}$	RSYNC→BCLK, See Timing Diagram	100	—	—	ns
Sync Pulse Width	$t_{WS}$	XSYNC, RSYNC	1 BCLK	—	100	μs
PCMIN Set-up Time	$t_{DS}$	—	100	—	—	ns
PCMIN Hold Time	$t_{DH}$	—	100	—	—	ns
Digital Output Load	$R_{DL}$	Pull-up resistor	0.5	—	—	kΩ
	$C_{DL}$	—	—	—	100	pF
Analog Input Allowable DC Offset	$V_{off}$	Transmit gain stage, Gain = 1	−100	—	+100	mV
		Transmit gain stage, Gain = 10	−10	—	+10	mV
Allowable Jitter Width	—	XSYNC, RSYNC, BCLK	—	—	1	μs

## ELECTRICAL CHARACTERISTICS

### DC and Digital Interface Characteristics

( $V_{DD} = +5 \text{ V} \pm 5\%$ ,  $T_a = -30^\circ\text{C}$  to  $+85^\circ\text{C}$ )

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Power Supply Current	$I_{DD1}$	Operating mode, No signal	—	5	9	mA
	$I_{DD2}$	Power-down mode, PDN = 0	—	0.01	0.05	mA
	$I_{DD3}$	Power-save mode, PDN = 1, XSYNC → OFF	—	1.2	3.0	mA
Input High Voltage	$V_{IH}$	—	2.2	—	$V_{DD}$	V
Input Low Voltage	$V_{IL}$	—	0.0	—	0.8	V
High Level Input Leakage Current	$I_{IH}$	—	—	—	2.0	$\mu\text{A}$
Low Level Input Leakage Current	$I_{IL}$	—	—	—	0.5	$\mu\text{A}$
Digital Output Low Voltage	$V_{OL}$	Pull-up resistance > 500 $\Omega$	0.0	0.2	0.4	V
Digital Output Leakage Current	$I_O$	—	—	—	10	$\mu\text{A}$
Input Capacitance	$C_{IN}$	—	—	5	—	pF
Analog Input Resistance	$R_{IN}$	AIN+, AIN-	—	10	—	M $\Omega$

### Transmit Analog Interface Characteristics

( $V_{DD} = +5 \text{ V}$  to  $\pm 5\%$ ,  $T_a = -30^\circ\text{C}$  to  $+85^\circ\text{C}$ )

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Input Resistance	$R_{INX}$	AIN+, AIN-	10	—	—	M $\Omega$
Output Load Resistance	$R_{LGX}$	GSX with respect to SG	20	—	—	k $\Omega$
Output Load Capacitance	$C_{LGX}$		—	—	30	pF
Output Amplitude	$V_{OGX}$		-1.2	—	+1.2	V
Offset Voltage	$V_{OSGX}$	Gain = 1	-20	—	+20	mV

### Receive Analog Interface Characteristics

( $V_{DD} = +5 \text{ V}$  to  $\pm 5\%$ ,  $T_a = -30^\circ\text{C}$  to  $+85^\circ\text{C}$ )

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Output Load Resistance	$R_{LAO}$	AOUT with respect to SG	0.6	—	—	k $\Omega$
Output Load Capacitance	$C_{LAO}$	AOUT with respect to SG	—	—	50	pF
Output Amplitude	$V_{OAO}$	AOUT with respect to SG	-1.2	—	+1.2	V
Offset Voltage	$V_{OSAO}$	AOUT with respect to SG	-100	—	+100	mV

## AC Characteristics

(V<sub>DD</sub> = +5 V ±5%, Ta = -30°C to +85°C)

Parameter	Symbol	Freq. (Hz)	Level (dBm0)	Condition	Min.	Typ.	Max.	Unit	
Transmit Frequency Response	Loss T1	60	0		20	26	—	dB	
	Loss T2	300			-0.15	+0.07	+0.20	dB	
	Loss T3	1020			Reference		dB		
	Loss T4	2020			-0.15	-0.04	+0.20	dB	
	Loss T5	3000			-0.15	+0.06	+0.20	dB	
	Loss T6	3400			0	0.4	0.80	dB	
Receive Frequency Response	Loss R1	300	0		-0.15	-0.03	+0.20	dB	
	Loss R2	1020			Reference		dB		
	Loss R3	2020			-0.15	-0.02	+0.20	dB	
	Loss R4	3000			-0.15	+0.15	+0.20	dB	
	Loss R5	3400			0.0	0.4	0.80	dB	
Transmit Signal to Distortion Ratio	SD T1	1020	3	*1	35	43	—	dB	
	SD T2		0		35	41	—		
	SD T3		-30		35	38	—		
	SD T4		-40		29	31	—		
	SD T5		-45			30	—		
	SD R1		3		24	27	—		
Receive Signal to Distortion Ratio	SD R2		0			26	—		
	SD R3		-30	*1	36	43	—	dB	
	SD R4		-40		30	33.5	—		
	SD R5		-45			29	32		
	SD R1		3		25	30	—		
	SD R2		0			24	27		
Transmit Gain Tracking	GT T1	1020	3		-0.3	+0.01	+0.3	dB	
	GT T2		-10		Reference				
	GT T3		-40		-0.3	0	+0.3		
	GT T4		-50		-0.6	-0.13	+0.6		
	GT T5		-55		-1.2	-0.15	+1.2		
Receive Gain Tracking	GT R1	1020	3		-0.3	0	+0.3	dB	
	GT R2		-10		Reference				
	GT R3		-40		-0.3	+0.10	+0.3		
	GT R4		-50		-0.6	+0.20	+0.6		
	GT R5		-55		-1.2	+0.25	+1.2		

\*1 Psophometric filter is used

\*2 Upper is specified for the MSM7578H, lower for the MSM7579

## AC Characteristics (Continued)

(V<sub>DD</sub> = +5 V ±5%, Ta = -30°C to +85°C)

Parameter	Symbol	Freq. (Hz)	Level (dBm0)	Condition	Min.	Typ.	Max.	Unit
Idle Channel Noise	Nidle T	—	—	AIN = SG *1 *2	—	-72.5	-70	dBmOp
	Nidle R	—	—	*1 *3	—	-70.5	-68	
Absolute Level (Initial Difference)	AV T	1020	0	V <sub>DD</sub> = 5.0 V Ta = 25°C	0.5803	0.6007	0.6218	Vrms
	AV R				0.5803	0.6007	0.6218	
Absolute Level (Deviation of Temperature and Power)	AV Tt	1020	0	V <sub>DD</sub> = +5 V ±5% Ta = -30 to 85°C	-0.2	—	+0.2	dB
	AV Rt				-0.2	—	+0.2	
Absolute Delay	Td	1020	0	A to A BCLK = 64 kHz	—	—	0.60	ms
Transmit Group Delay	tgd T1	500	0	*4	—	0.19	0.75	ms
	tgd T2	600			—	0.11	0.35	
	tgd T3	1000			—	0.02	0.125	
	tgd T4	2600			—	0.05	0.125	
	tgd T5	2800			—	0.07	0.75	
Receive Group Delay	tgd R1	500	0	*4	—	0.00	0.75	ms
	tgd R2	600			—	0.00	0.35	
	tgd R3	1000			—	0.00	0.125	
	tgd R4	2600			—	0.09	0.125	
	tgd R5	2800			—	0.12	0.75	
Crosstalk Attenuation	CR T	1020	0	TRANS → RECV	75	85	—	dB
	CR R			RECV → TRANS	70	80	—	

\*1 Psophometric filter is used

\*2 Upper is specified for the MSM7578H, lower for the MSM7579

\*3 MSM7578H: All "1", MSM7579: "11010101"

\*4 Minimum value of the group delay distortion

## AC Characteristics (Continued)

(V<sub>DD</sub> = +5 V ±5%, Ta = -30°C to +85°C)

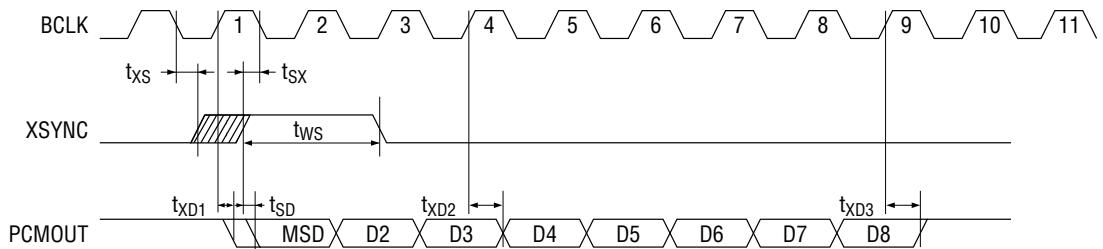
Parameter	Symbol	Freq. (Hz)	Level (dBm0)	Condition	Min.	Typ.	Max.	Unit
Discrimination	DIS	4.6 kHz to 72 kHz	0	0 to 4000 Hz	30	32	—	dB
Out-of-band Spurious	S	300 to 3400	0	4.6 kHz to 100 kHz	—	-37.5	-35	dBm0
Intermodulation Distortion	IMD	f <sub>a</sub> = 470 f <sub>b</sub> = 320	-4	2f <sub>a</sub> - f <sub>b</sub>	—	-52	-35	dBm0
Power Supply Noise Rejection Ratio	PSR T PSR R	0 to 50 kHz	50 mV <sub>PP</sub>	*5	—	30	—	dB
Digital Output Delay Time	t <sub>SD</sub>	C <sub>L</sub> = 100 pF			20	—	200	ns
	t <sub>XD1</sub>				20	—	200	
	t <sub>XD2</sub>				20	—	200	
	t <sub>XD3</sub>				20	—	200	

\*5 The measurement under idle channel noise

## TIMING DIAGRAM

### PCM Data Input/Output Timing

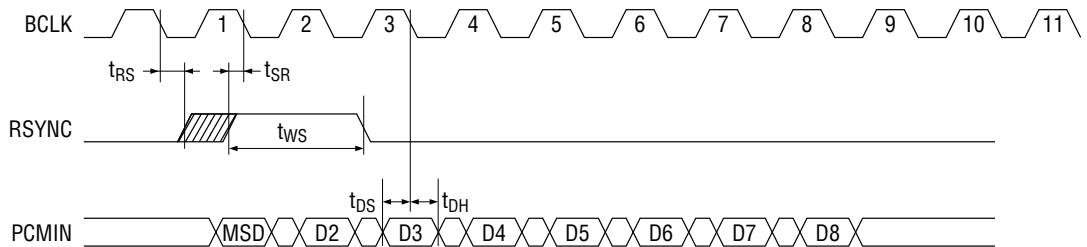
#### Transmit Timing



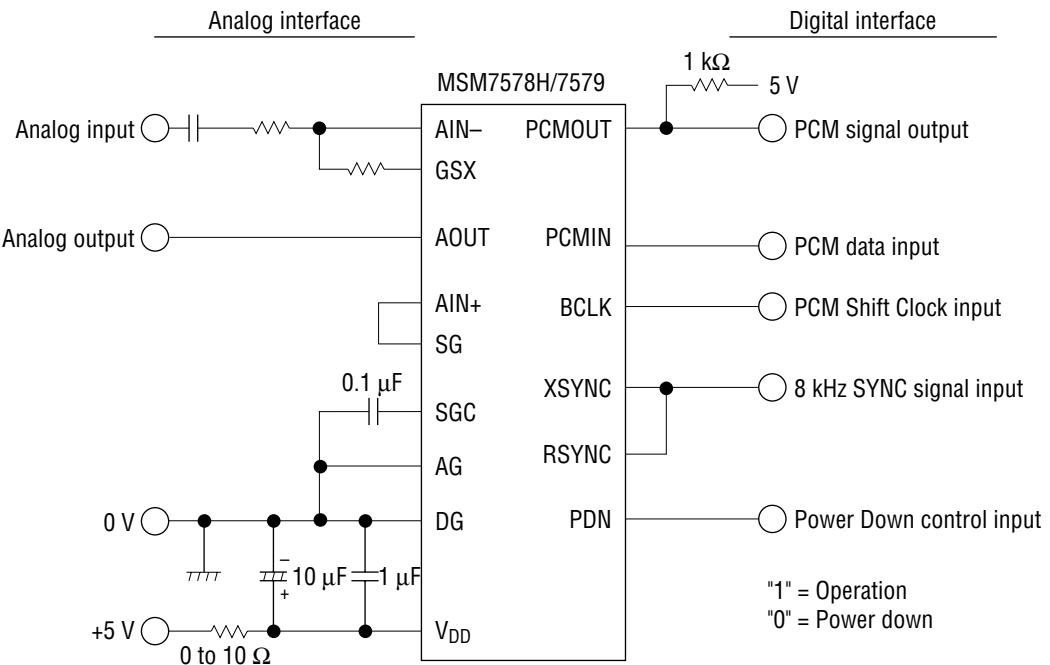
When  $t_{XS} \leq 1/2 \cdot F_c$ , the Delay of the MSD bit is defined as  $t_{XD1}$ .

When  $t_{SX} \leq 1/2 \cdot F_c$ , the Delay of the MSD bit is defined as  $t_{SD}$ .

#### Receive Timing



## APPLICATION CIRCUIT



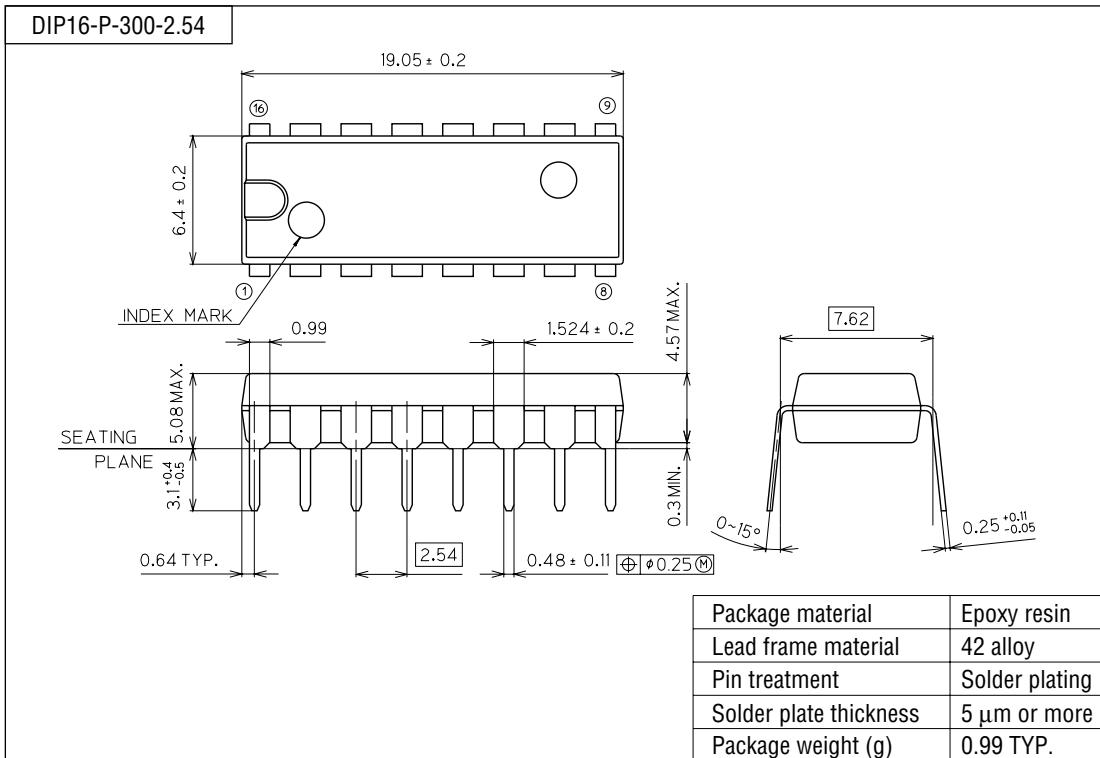
The analog output signal has an amplitude of  $\pm 1.2$  V above and below the offset voltage level of  $V_{DD}/2$ .

## RECOMMENDATIONS FOR ACTUAL DESIGN

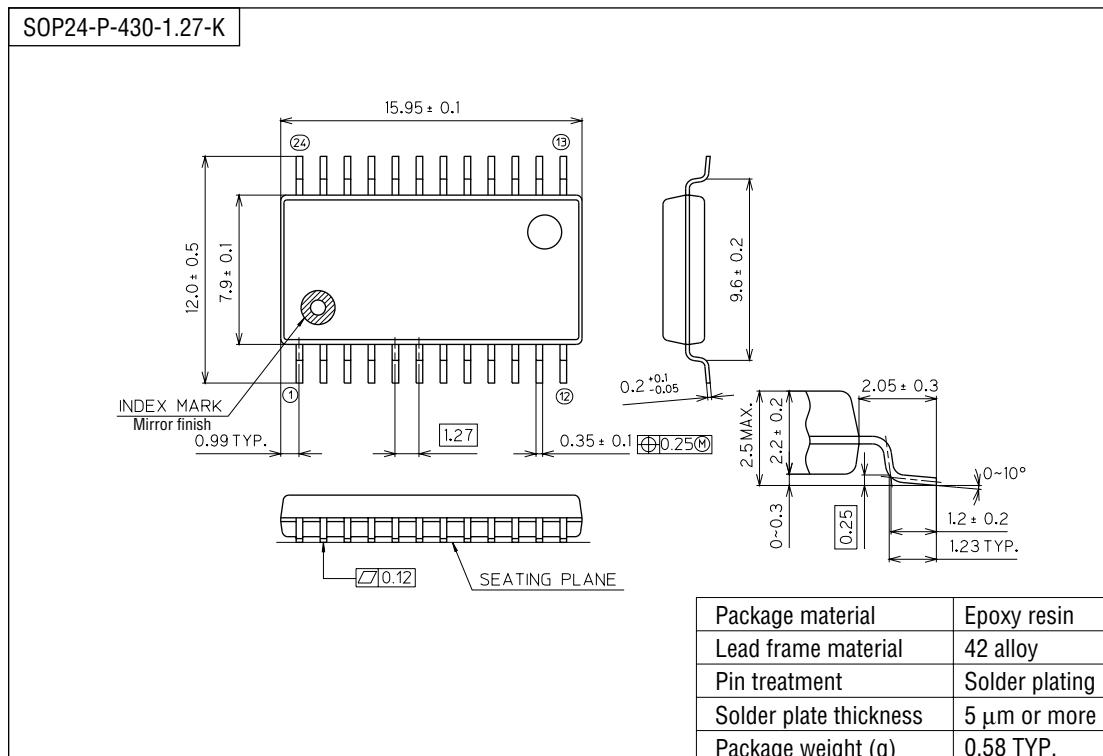
- To assure proper electrical characteristics, use bypass capacitors with excellent high frequency characteristics for the power supply and keep them as close as possible to the device pins.
- Connect the AG pin and the DG pin each other as close as possible. Connect to the system ground with low impedance.
- Mount the device directly on the board when mounted on PCBs. Do not use IC sockets. If an IC socket is unavoidable, use the short lead type socket.
- When mounted on a frame, use electro-magnetic shielding, if any electro-magnetic wave source such as power supply transformers surround the device.
- Keep the voltage on the V<sub>DD</sub> pin not lower than -0.3 V even instantaneously to avoid latch-up phenomenon when turning the power on.
- Use a low noise (particularly, low level type of high frequency spike noise or pulse noise) power supply to avoid erroneous operation and the degradation of the characteristics of these devices.

## PACKAGE DIMENSIONS

(Unit : mm)



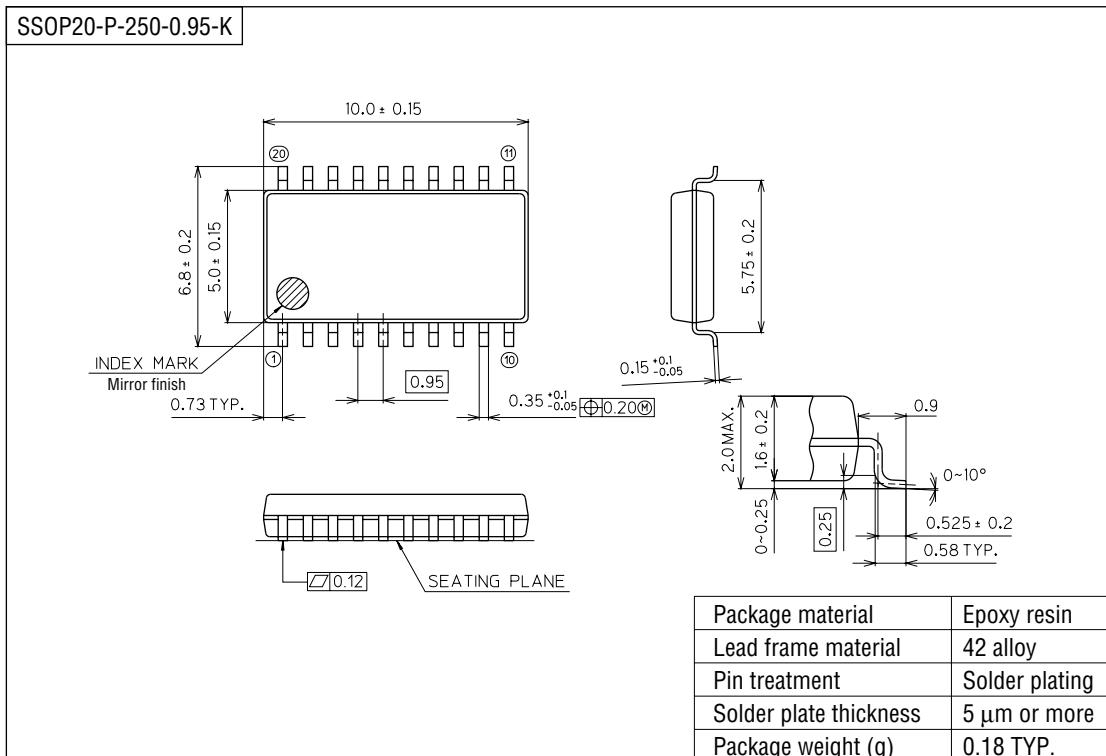
(Unit : mm)



#### Notes for Mounting the Surface Mount Type Package

The SOP, QFP, TSOP, SOJ, QFJ (PLCC), SHP and BGA are surface mount type packages, which are very susceptible to heat in reflow mounting and humidity absorbed in storage. Therefore, before you perform reflow mounting, contact Oki's responsible sales person for the product name, package name, pin number, package code and desired mounting conditions (reflow method, temperature and times).

(Unit : mm)



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