intersil

HGTP12N60A4, HGTG12N60A4, HGT1S12N60A4S

Data Sheet *May 1999* *File Number* 4656.2

600V, SMPS Series N-Channel IGBT

The HGTP12N60A4, HGTG12N60A4 and HGT1S12N60A4S are MOS gated high voltage switching devices combining the best features of MOSFETs and bipolar transistors. These devices have the high input impedance of a MOSFET and the low on-state conduction loss of a bipolar transistor. The much lower on-state voltage drop varies only moderately between 25°C and 150°C.

This IGBT is ideal for many high voltage switching applications operating at high frequencies where low conduction losses are essential. This device has been optimized for high frequency switch mode power supplies.

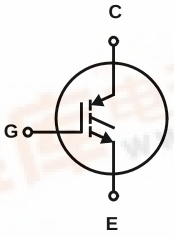
Formerly Developmental Type TA49335.

Ordering Information

PART NUMBER	PACKAGE	BRAND
HGTP12N60A4	TO-220AB	12N60A4
HGTG12N60A4	TO-247	12N60A4
HGT1S12N60A4S	TO-263AB	12N60A4

NOTE: When ordering, use the entire part number. Add the suffix 9A to obtain the TO-263AB variant in tape and reel, e.g. HGT1S12N60A4S9A

Symbol

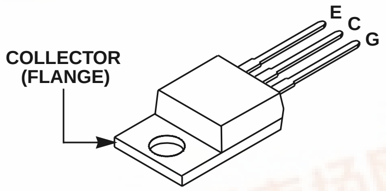


Features

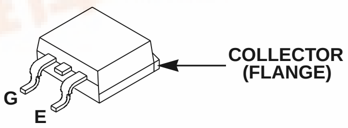
- >100kHz Operation at 390V, 12A
- 200kHz Operation at 390V, 9A
- 600V Switching SOA Capability
- Typical Fall Time. . . . . 70ns at T_J = 125°C
- Low Conduction Loss
- *Temperature Compensating* SABER Model http://www.intersil.com
- Related Literature
  - TB334 “Guidelines for Soldering Surface Mount Components to PC Boards

Packaging

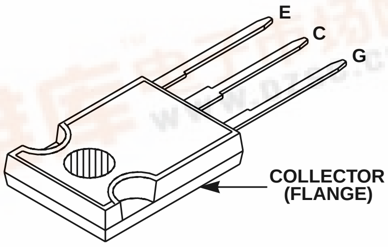
JEDEC TO-220AB ALTERNATE VERSION



JEDEC TO-263AB



JEDEC STYLE TO-247



INTERSIL CORPORATION IGBT PRODUCT IS COVERED BY ONE OR MORE OF THE FOLLOWING U.S. PATENTS

4,364,073	4,417,385	4,430,792	4,443,931	4,466,176	4,516,143	4,532,534	4,567,641
4,587,713	4,598,461	4,605,948	4,618,872	4,620,211	4,631,564	4,639,754	4,639,762
4,641,162	4,644,637	4,682,195	4,684,413	4,694,313	4,717,679	4,743,952	4,783,690
4,794,432	4,801,986	4,803,533	4,809,045	4,809,047	4,810,665	4,823,176	4,837,606
4,860,080	4,883,767	4,888,627	4,890,143	4,901,127	4,904,609	4,933,740	4,963,951
4,969,027							

CAUTION: These devices are sensitive to electrostatic discharge; follow proper IC Handling Procedures

Absolute Maximum Ratings $T_C = 25^oC$, Unless Otherwise Specified

		HGTG12N60A4, HGTP12N60A4, HGT1S12N60A4S	UNITS
Collector to Emitter Voltage	BV_{CES}	600	V
Collector Current Continuous			
At $T_C = 25^oC$	I_{C25}	54	A
At $T_C = 110^oC$	C110	23	A
Collector Current Pulsed (Note 1)	I_{CM}	96	A
Gate to Emitter Voltage Continuous	V_{GES}	±20	V
Gate to Emitter Voltage Pulsed	V_{GEM}	±30	V
Switching Safe Operating Area at $T_J = 150^oC$, Figure 2	SSOA	60A at 600V	
Power Dissipation Total at $T_C = 25^oC$	P_D	167	W
Power Dissipation Derating $T_C > 25^oC$		1.33	$W/^oC$
Operating and Storage Junction Temperature Range	T_J, T_{STG}	-55 to 150	^oC
Maximum Lead Temperature for Soldering			
Leads at 0.063in (1.6mm) from Case for 10s	T_L	300	^oC
Package Body for 10s, See Techbrief 334	T_{PKG}	260	^oC

CAUTION: Stresses above those listed in “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

1. Pulse width limited by maximum junction temperature.

Electrical Specifications $T_J = 25^oC$, Unless Otherwise Specified

PARAMETER	SYMBOL	TEST CONDITIONS		MIN	TYP	MAX	UNITS
Collector to Emitter Breakdown Voltage	BV_{CES}	$I_C = 250\mu A$, $V_{GE} = 0V$		600	-	-	V
Emitter to Collector Breakdown Voltage	BV_{ECS}	$I_C = 10mA$, $V_{GE} = 0V$		10	-	-	V
Collector to Emitter Leakage Current	I_{CES}	$V_{CE} = 600V$	$T_J = 25^oC$	-	-	250	µA
			$T_J = 125^oC$	-	-	2.0	mA
Collector to Emitter Saturation Voltage	$V_{CE(SAT)}$	$I_C = 12A$, $V_{GE} = 15V$	$T_J = 25^oC$	-	2.0	2.7	V
			$T_J = 125^oC$	-	1.6	2.0	V
Gate to Emitter Threshold Voltage	$V_{GE(TH)}$	$I_C = 250\mu A$, $V_{CE} = 600V$		-	5.6	-	V
Gate to Emitter Leakage Current	I_{GES}	$V_{GE} = \pm 20V$		-	-	±250	nA
Switching SOA	SSOA	$T_J = 150^oC$, $R_G = 10\Omega$, $V_{GE} = 15V$ $L = 100\mu H$, $V_{CE} = 600V$		60	-	-	A
Gate to Emitter Plateau Voltage	V_{GEP}	$I_C = 12A$, $V_{CE} = 300V$		-	8	-	V
On-State Gate Charge	$Q_{g(ON)}$	$I_C = 12A$, $V_{CE} = 300V$	$V_{GE} = 15V$	-	78	96	nC
			$V_{GE} = 20V$	-	97	120	nC
Current Turn-On Delay Time	$t_{d(ON)I}$	IGBT and Diode at $T_J = 25^oC$ $I_{CE} = 12A$ $V_{CE} = 390V$ $V_{GE} = 15V$ $R_G = 10\Omega$ $L = 500\mu H$ Test Circuit - (Figure 20)		-	17	-	ns
Current Rise Time	t_{rI}			-	8	-	ns
Current Turn-Off Delay Time	$t_{d(OFF)I}$			-	96	-	ns
Current Fall Time	t_{fI}			-	18	-	ns
Turn-On Energy (Note 3)	E_{ON1}			-	55	-	µJ
Turn-On Energy (Note 3)	E_{ON2}			-	160	-	µJ
Turn-Off Energy (Note 2)	E_{OFF}			-	50	-	µJ

Electrical Specifications $T_J = 25^oC$, Unless Otherwise Specified **(Continued)**

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Current Turn-On Delay Time	$t_{d(ON)I}$	IGBT and Diode at $T_J = 125^oC$ $I_{CE} = 12A$ $V_{CE} = 390V$ $V_{GE} = 15V$ $R_G = 10\Omega$ $L = 500\mu H$ Test Circuit - (Figure 20)	-	17	-	ns
Current Rise Time	t_{rI}		-	16	-	ns
Current Turn-Off Delay Time	$t_{d(OFF)I}$		-	110	170	ns
Current Fall Time	t_{fI}		-	70	95	ns
Turn-On Energy (Note 3)	E_{ON1}		-	55	-	µJ
Turn-On Energy (Note 3)	E_{ON2}		-	250	350	µJ
Turn-Off Energy (Note 2)	E_{OFF}		-	175	285	µJ
Thermal Resistance Junction To Case	$R_{\theta JC}$		-	-	0.75	$^oC/W$

NOTES:

2. Turn-Off Energy Loss (E_{OFF}) is defined as the integral of the instantaneous power loss starting at the trailing edge of the input pulse and ending at the point where the collector current equals zero ($I_{CE} = 0A$). All devices were tested per JEDEC Standard No. 24-1 Method for Measurement of Power Device Turn-Off Switching Loss. This test method produces the true total Turn-Off Energy Loss.
3. Values for two Turn-On loss conditions are shown for the convenience of the circuit designer. E_{ON1} is the turn-on loss of the IGBT only. E_{ON2} is the turn-on loss when a typical diode is used in the test circuit and the diode is at the same T_J as the IGBT. The diode type is specified in Figure 20.

Typical Performance Curves Unless Otherwise Specified

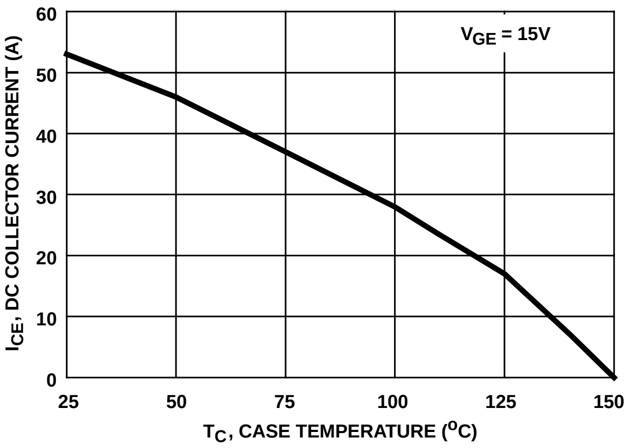


FIGURE 1. DC COLLECTOR CURRENT vs CASE TEMPERATURE

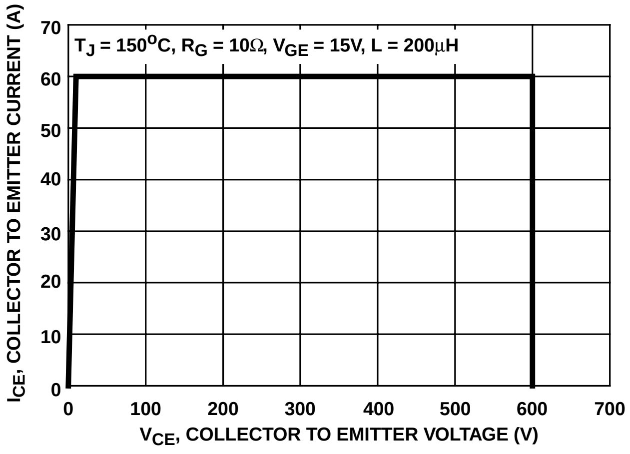


FIGURE 2. MINIMUM SWITCHING SAFE OPERATING AREA

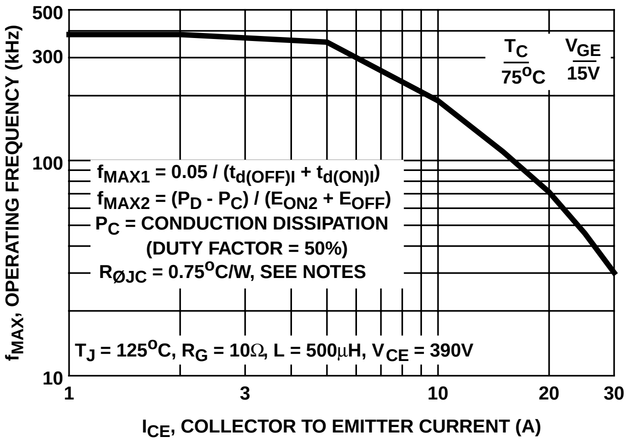


FIGURE 3. OPERATING FREQUENCY vs COLLECTOR TO EMITTER CURRENT

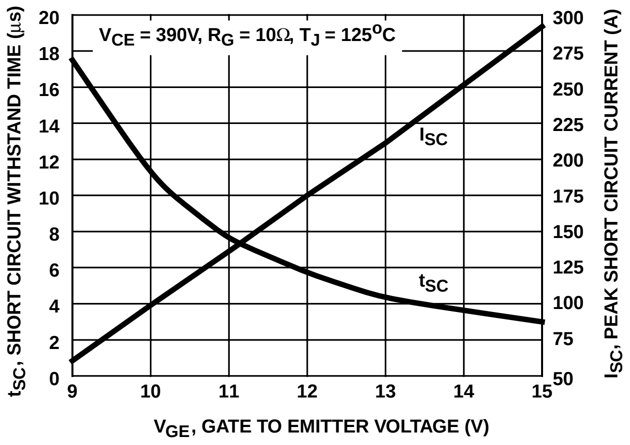


FIGURE 4. SHORT CIRCUIT WITHSTAND TIME

Typical Performance Curves Unless Otherwise Specified **(Continued)**

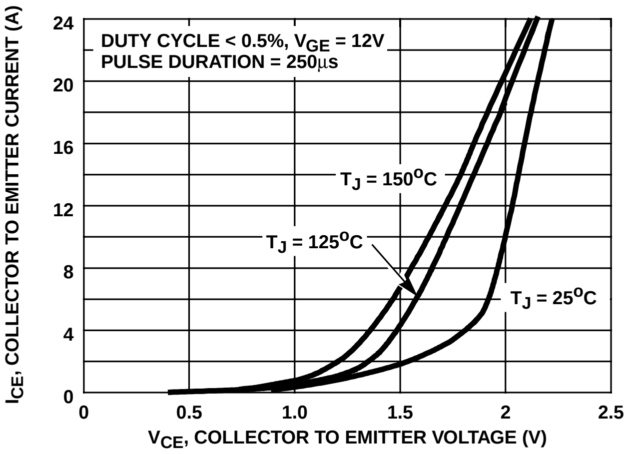


FIGURE 5. COLLECTOR TO EMITTER ON-STATE VOLTAGE

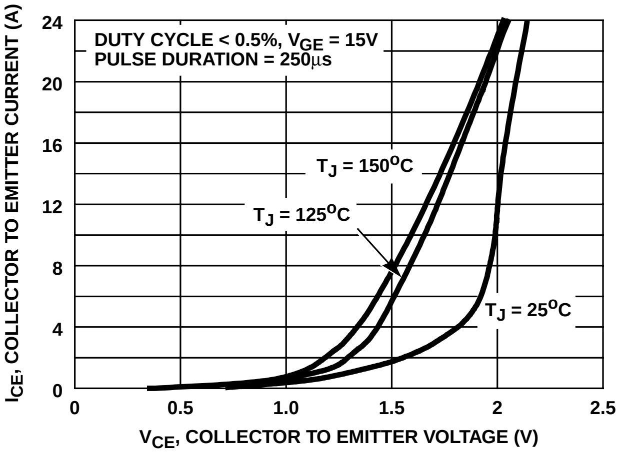


FIGURE 6. COLLECTOR TO EMITTER ON-STATE VOLTAGE

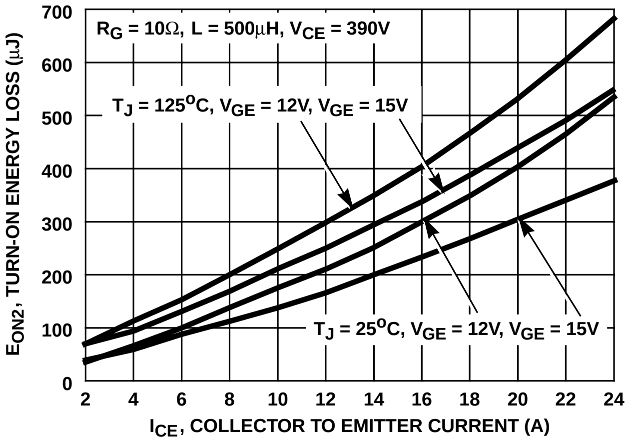


FIGURE 7. TURN-ON ENERGY LOSS vs COLLECTOR TO EMITTER CURRENT

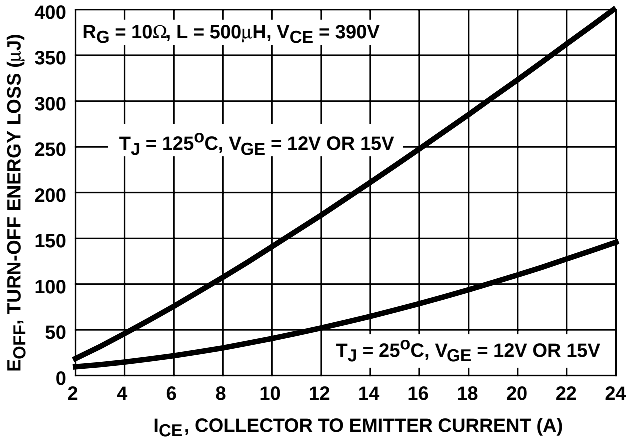


FIGURE 8. TURN-OFF ENERGY LOSS vs COLLECTOR TO EMITTER CURRENT

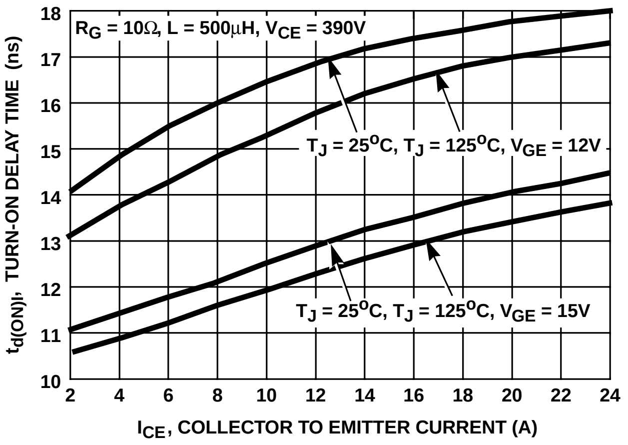


FIGURE 9. TURN-ON DELAY TIME vs COLLECTOR TO EMITTER CURRENT

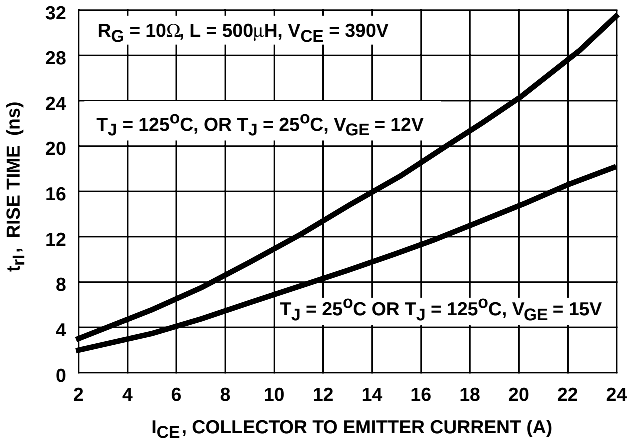


FIGURE 10. TURN-ON RISE TIME vs COLLECTOR TO EMITTER CURRENT

Typical Performance Curves Unless Otherwise Specified **(Continued)**

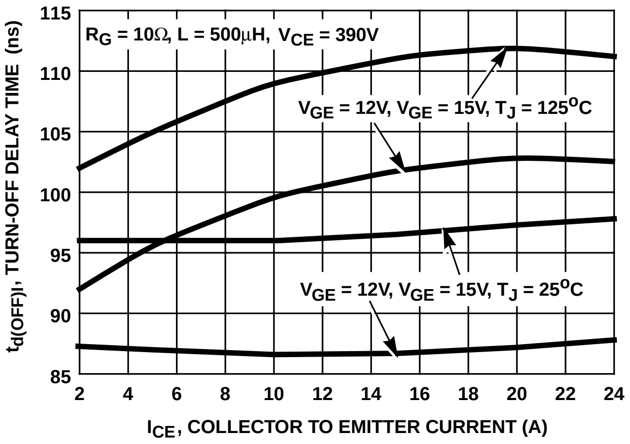


FIGURE 11. TURN-OFF DELAY TIME vs COLLECTOR TO EMITTER CURRENT

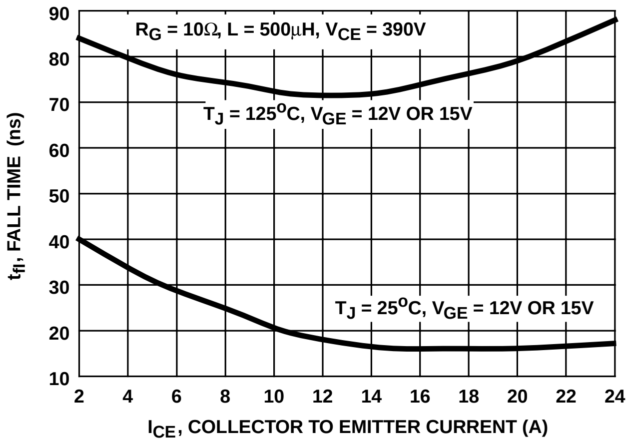


FIGURE 12. FALL TIME vs COLLECTOR TO EMITTER CURRENT

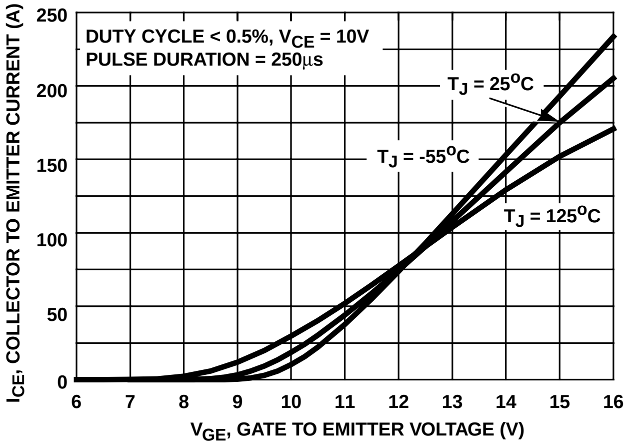


FIGURE 13. TRANSFER CHARACTERISTIC

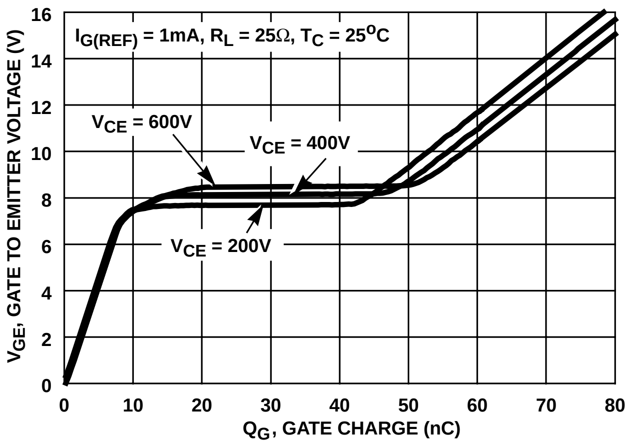


FIGURE 14. GATE CHARGE WAVEFORMS

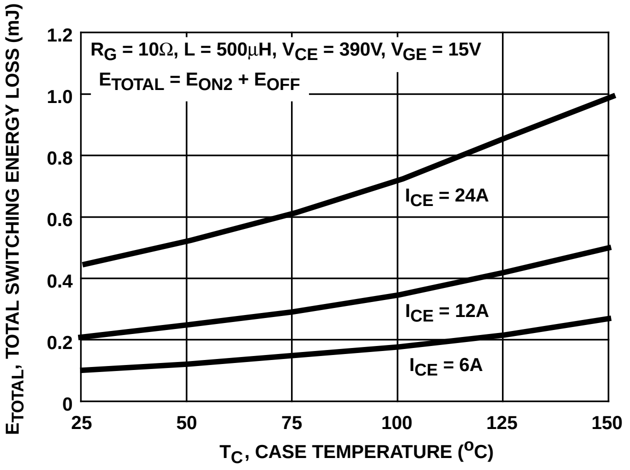


FIGURE 15. TOTAL SWITCHING LOSS vs CASE TEMPERATURE

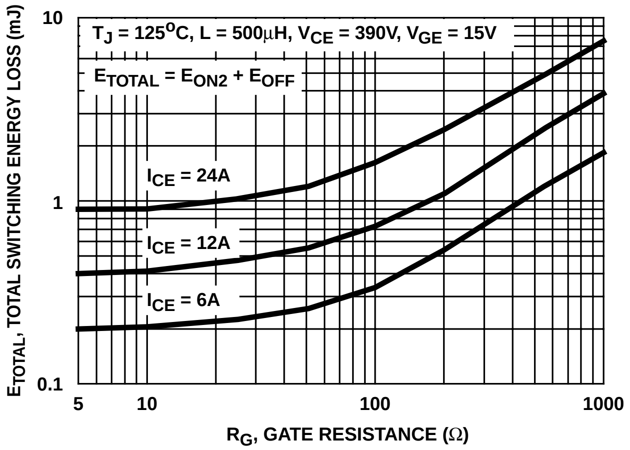


FIGURE 16. TOTAL SWITCHING LOSS vs GATE RESISTANCE

Typical Performance Curves Unless Otherwise Specified **(Continued)**

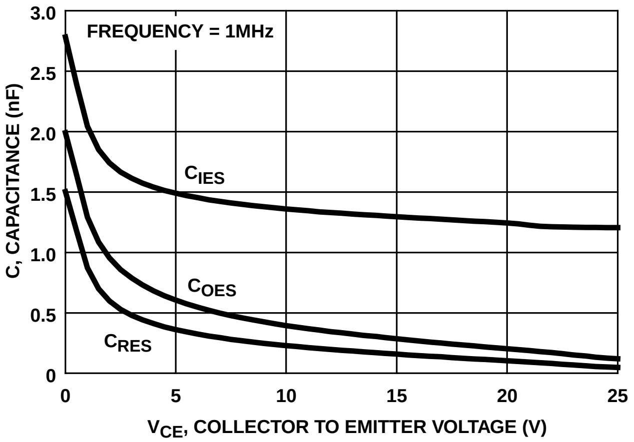


FIGURE 17. CAPACITANCE vs COLLECTOR TO EMITTER VOLTAGE

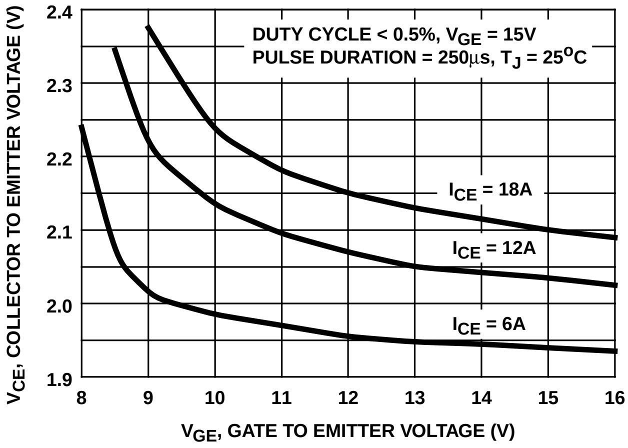


FIGURE 18. COLLECTOR TO EMITTER ON-STATE VOLTAGE vs GATE TO EMITTER VOLTAGE

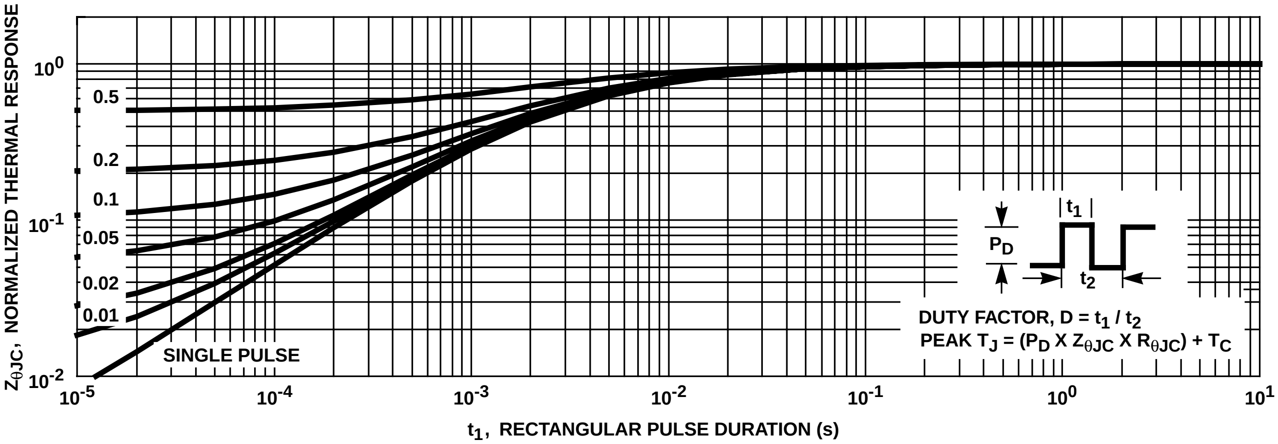


FIGURE 19. IGBT NORMALIZED TRANSIENT THERMAL RESPONSE, JUNCTION TO CASE

Test Circuit and Waveforms

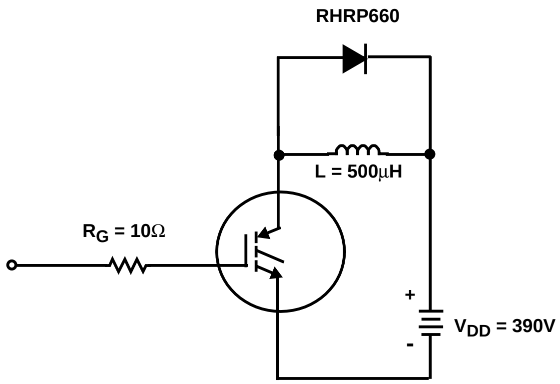


FIGURE 20. INDUCTIVE SWITCHING TEST CIRCUIT

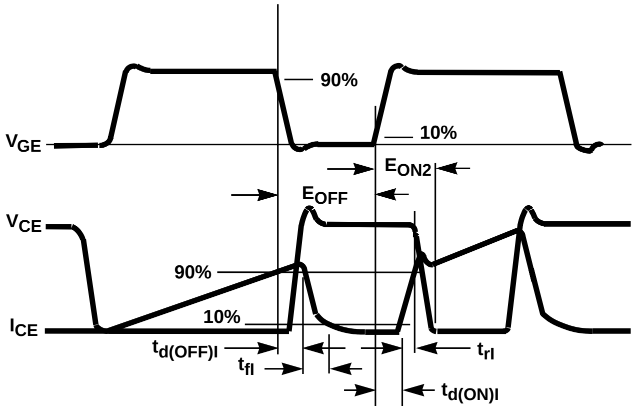


FIGURE 21. SWITCHING TEST WAVEFORMS

Handling Precautions for IGBTs

Insulated Gate Bipolar Transistors are susceptible to gate-insulation damage by the electrostatic discharge of energy through the devices. When handling these devices, care should be exercised to assure that the static charge built in the handler's body capacitance is not discharged through the device. With proper handling and application procedures, however, IGBTs are currently being extensively used in production by numerous equipment manufacturers in military, industrial and consumer applications, with virtually no damage problems due to electrostatic discharge. IGBTs can be handled safely if the following basic precautions are taken:

1. Prior to assembly into a circuit, all leads should be kept shorted together either by the use of metal shorting springs or by the insertion into conductive material such as "ECCOSORBD™ LD26" or equivalent.
2. When devices are removed by hand from their carriers, the hand being used should be grounded by any suitable means - for example, with a metallic wristband.
3. Tips of soldering irons should be grounded.
4. Devices should never be inserted into or removed from circuits with power on.
5. **Gate Voltage Rating** - Never exceed the gate-voltage rating of V_{GEM}. Exceeding the rated V_{GE} can result in permanent damage to the oxide layer in the gate region.
6. **Gate Termination** - The gates of these devices are essentially capacitors. Circuits that leave the gate open-circuited or floating should be avoided. These conditions can result in turn-on of the device due to voltage buildup on the input capacitor due to leakage currents or pickup.
7. **Gate Protection** - These devices do not have an internal monolithic Zener diode from gate to emitter. If gate protection is required an external Zener is recommended.

Operating Frequency Information

Operating frequency information for a typical device (Figure 3) is presented as a guide for estimating device performance for a specific application. Other typical frequency vs collector current (I_{CE}) plots are possible using the information shown for a typical unit in Figures 5, 6, 7, 8, 9 and 11. The operating frequency plot (Figure 3) of a typical device shows f_{MAX1} or f_{MAX2}; whichever is smaller at each point. The information is based on measurements of a typical device and is bounded by the maximum rated junction temperature.

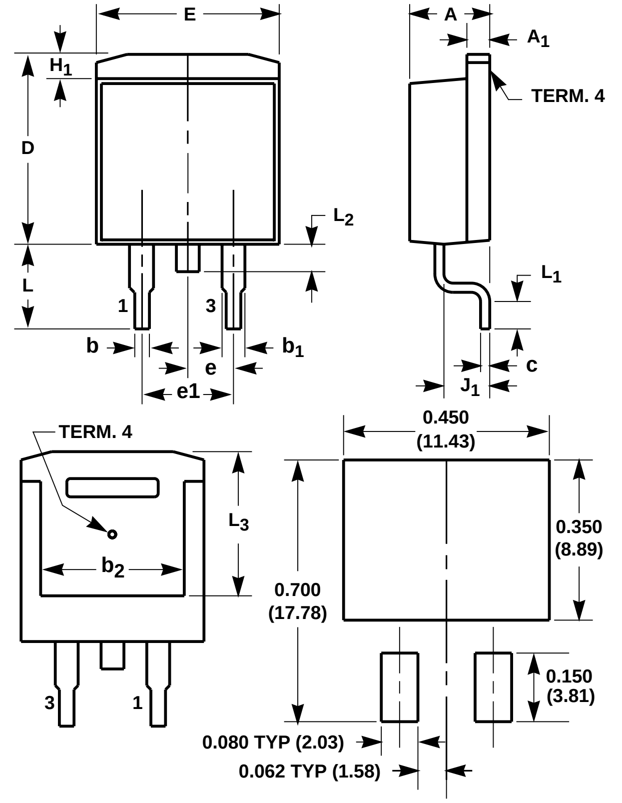
f_{MAX1} is defined by $f_{MAX1} = 0.05/(t_{d(OFF)I} + t_{d(ON)I})$. Deadtime (the denominator) has been arbitrarily held to 10% of the on-state time for a 50% duty factor. Other definitions are possible. $t_{d(OFF)I}$ and $t_{d(ON)I}$ are defined in Figure 21. Device turn-off delay can establish an additional frequency limiting condition for an application other than T_{JM}.

f_{MAX2} is defined by $f_{MAX2} = (P_D - P_C)/(E_{OFF} + E_{ON2})$. The allowable dissipation (P_D) is defined by $P_D = (T_{JM} - T_C)/R_{\theta JC}$. The sum of device switching and conduction losses must not exceed P_D. A 50% duty factor was used (Figure 3) and the conduction losses (P_C) are approximated by $P_C = (V_{CE} \times I_{CE})/2$.

E_{ON2} and E_{OFF} are defined in the switching waveforms shown in Figure 21. E_{ON2} is the integral of the instantaneous power loss ($I_{CE} \times V_{CE}$) during turn-on and E_{OFF} is the integral of the instantaneous power loss ($I_{CE} \times V_{CE}$) during turn-off. All tail losses are included in the calculation for E_{OFF}; i.e., the collector current equals zero ($I_{CE} = 0$).

ECCOSORBD™ is a trademark of Emerson and Cumming, Inc.

TO-263AB SURFACE MOUNT JEDEC TO-263AB PLASTIC PACKAGE



MINIMUM PAD SIZE RECOMMENDED FOR SURFACE-MOUNTED APPLICATIONS

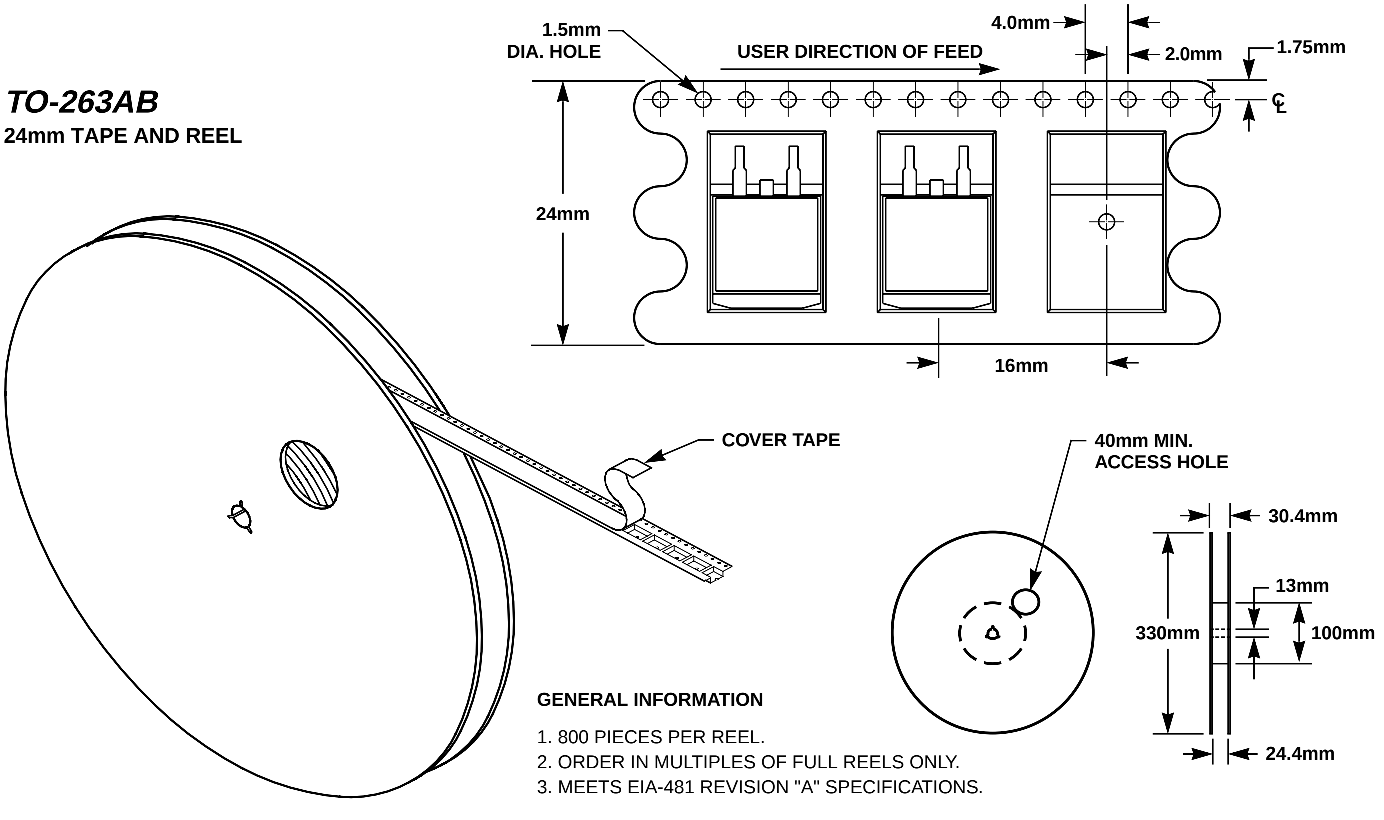
SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.170	0.180	4.32	4.57	-
A_1	0.048	0.052	1.22	1.32	4, 5
b	0.030	0.034	0.77	0.86	4, 5
b_1	0.045	0.055	1.15	1.39	4, 5
b_2	0.310	-	7.88	-	2
c	0.018	0.022	0.46	0.55	4, 5
D	0.405	0.425	10.29	10.79	-
E	0.395	0.405	10.04	10.28	-
e	0.100 TYP		2.54 TYP		7
e_1	0.200 BSC		5.08 BSC		7
H_1	0.045	0.055	1.15	1.39	-
J_1	0.095	0.105	2.42	2.66	-
L	0.175	0.195	4.45	4.95	-
L_1	0.090	0.110	2.29	2.79	4, 6
L_2	0.050	0.070	1.27	1.77	3
L_3	0.315	-	8.01	-	2

NOTES:

1. These dimensions are within allowable dimensions of Rev. C of JEDEC TO-263AB outline dated 2-92.
2. L_3 and b_2 dimensions established a minimum mounting surface for terminal 4.
3. Solder finish uncontrolled in this area.
4. Dimension (without solder).
5. Add typically 0.002 inches (0.05mm) for solder plating.
6. L_1 is the terminal length for soldering.
7. Position of lead to be measured 0.120 inches (3.05mm) from bottom of dimension D.
8. Controlling dimension: Inch.
9. Revision 11 dated 5-99.

TO-263AB

24mm TAPE AND REEL

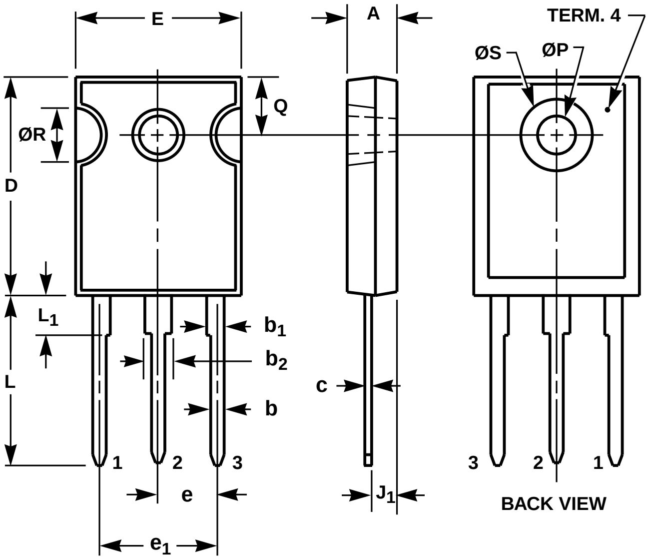


GENERAL INFORMATION

1. 800 PIECES PER REEL.
2. ORDER IN MULTIPLES OF FULL REELS ONLY.
3. MEETS EIA-481 REVISION "A" SPECIFICATIONS.

TO-247

3 LEAD JEDEC STYLE TO-247 PLASTIC PACKAGE



LEAD 1 - **GATE**
LEAD 2 - **COLLECTOR**
LEAD 3 - **EMITTER**
TERM. 4 - **COLLECTOR**

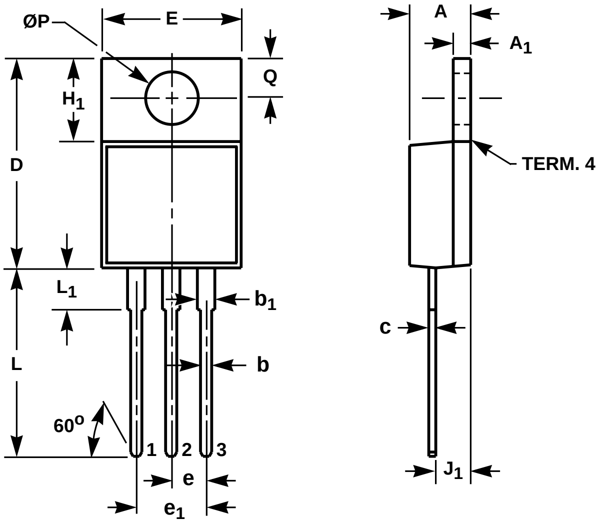
SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.180	0.190	4.58	4.82	-
b	0.046	0.051	1.17	1.29	2, 3
b_1	0.060	0.070	1.53	1.77	1, 2
b_2	0.095	0.105	2.42	2.66	1, 2
c	0.020	0.026	0.51	0.66	1, 2, 3
D	0.800	0.820	20.32	20.82	-
E	0.605	0.625	15.37	15.87	-
e	0.219 TYP		5.56 TYP		4
e_1	0.438 BSC		11.12 BSC		4
J_1	0.090	0.105	2.29	2.66	5
L	0.620	0.640	15.75	16.25	-
L_1	0.145	0.155	3.69	3.93	1
ØP	0.138	0.144	3.51	3.65	-
Q	0.210	0.220	5.34	5.58	-
ØR	0.195	0.205	4.96	5.20	-
ØS	0.260	0.270	6.61	6.85	-

NOTES:

1. Lead dimension and finish uncontrolled in L_1.
2. Lead dimension (without solder).
3. Add typically 0.002 inches (0.05mm) for solder coating.
4. Position of lead to be measured 0.250 inches (6.35mm) from bottom of dimension D.
5. Position of lead to be measured 0.100 inches (2.54mm) from bottom of dimension D.
6. Controlling dimension: Inch.
7. Revision 1 dated 1-93.

TO-220AB (Alternate Version)

3 LEAD JEDEC TO-220AB PLASTIC PACKAGE



SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.170	0.180	4.32	4.57	-
A_1	0.048	0.052	1.22	1.32	2, 4
b	0.030	0.034	0.77	0.86	2, 4
b_1	0.045	0.055	1.15	1.39	2, 4
c	0.018	0.022	0.46	0.55	2, 4
D	0.590	0.610	14.99	15.49	-
E	0.395	0.405	10.04	10.28	-
e	0.100 TYP		2.54 TYP		5
e_1	0.200 BSC		5.08 BSC		5
H_1	0.235	0.255	5.97	6.47	-
J_1	0.095	0.105	2.42	2.66	6
L	0.530	0.550	13.47	13.97	-
L_1	0.110	0.130	2.80	3.30	3
ØP	0.149	0.153	3.79	3.88	-
Q	0.105	0.115	2.66	2.92	-

NOTES:

1. These dimensions are within allowable dimensions of Rev. J of JEDEC TO-220AB outline dated 3-24-87.
2. Dimension (without solder).
3. Solder finish uncontrolled in this area.
4. Add typically 0.002 inches (0.05mm) for solder plating.
5. Position of lead to be measured 0.250 inches (6.35mm) from bottom of dimension D.
6. Position of lead to be measured 0.100 inches (2.54mm) from bottom of dimension D.
7. Controlling dimension: Inch.
8. Revision 3 dated 7-97.

All Intersil semiconductor products are manufactured, assembled and tested under **ISO9000** quality systems certification.

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