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### Dual SPST CMOS Analog Switch

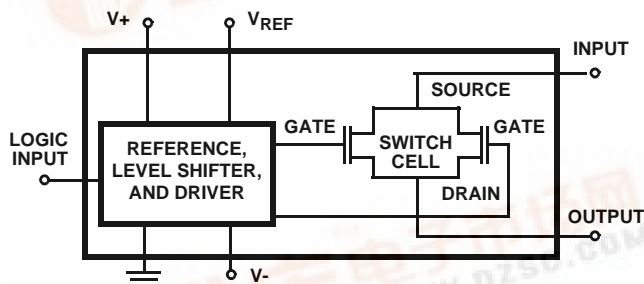
The HI-200/883 is a monolithic device comprising two independently selectable SPST switchers which feature fast switching speeds (240ns typical) combined with low power dissipation (15mW typical @ +25°C)

Each switch provides low "ON" resistance operation for input signal voltages up to the supply rails and for signal currents up to 25mA continuous. Rugged DI construction eliminates latch-up and substrate SCR failure modes.

All devices provide break-before-make switching and are TTL and CMOS compatible for maximum application versatility. HI-200/883 is an ideal component for use in high frequency analog switching. Typical applications include signal path switching, sample and hold circuits, digital filters, and op amp gain switching networks.

HI-200/883 is available in a 14 pin Ceramic DIP package and a 10 pin Metal Can (TO-100) package.

### Functional Diagram



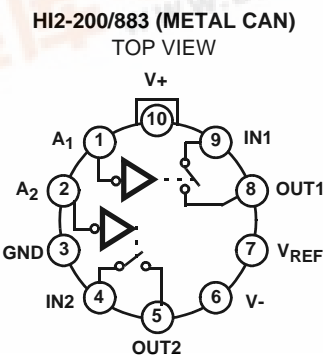
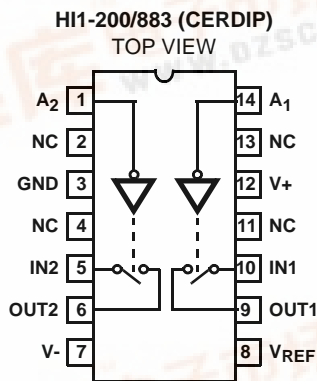
### Features

- This Circuit is Processed in Accordance to MIL-STD-883 and is Fully Conformant Under the Provisions of Paragraph 1.2.1.
- Low "On" Release .....100Ω Max
- Wide Analog Signal Range .....±15V
- TTL/CMOS Compatible ..... 2.4V (Logic "1")
- Turn-On Time..... 500ns
- Analog Current Range (Continuous) ..... 25mA
- No Latch-Up
- Replaces DG200

### Applications

- High Frequency Analog Switching
- Sample and Hold Circuits
- Digital Filters
- Op Amp Gain Switching Networks

### Pinouts



# HI-200/883

## Absolute Maximum Ratings

Voltage Between V+ and V- Terminals	.....40V
$\pm V_{SUPPLY}$ to Ground (V+, V-)	..... $\pm 20V$
Analog Input Voltage, (+V <sub>S</sub> )	..... +V <sub>SUPPLY</sub> +2V
(-V <sub>S</sub> )	..... -V <sub>SUPPLY</sub> -2V
Digital Input Voltage, (+V <sub>A</sub> )	..... +V <sub>SUPPLY</sub> +4V
(-V <sub>A</sub> )	..... -V <sub>SUPPLY</sub> -4V
Peak Current (S or D)	
(Pulse at 1ms, 10% Duty Cycle Max)	..... 40mA
Continuous Current	..... 25mA
Junction Temperature	..... +175°C
Storage Temperature Range	..... -65°C to +150°C
Lead Temperature (Soldering 10 sec)	..... $\leq 275^\circ C$

## Thermal Information

Thermal Resistance	$\theta_{JA}$ (°C/W)	$\theta_{JC}$ (°C/W)
CERDIP Package	80	24
Metal Can Package	160	75
Package Power Dissipation at +75°C		
Ceramic DIP Package	0.76W/°C	
Metal Can Package	0.62W/°C	
Package Power Dissipation Derating Factor above +75°C		
Ceramic DIP Package	10.08mW/°C	
Metal Can Package	8.24mW/°C	

## Recommended Operating Conditions

Operating Temperature Range	..... -55°C to +125°C
Operating Supply Voltage Range ( $\pm V_{SUPPLY}$ )	..... $\pm 15V$
Analog Input Voltage (V <sub>S</sub> )	..... $\pm V_{SUPPLY}$
Logic Low Level (V <sub>AL</sub> )	..... 0V to 0.8V
Logic High Level (V <sub>AH</sub> )	..... 2.4V to +V <sub>SUPPLY</sub>

*CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.*

**TABLE 1. D.C. ELECTRICAL PERFORMANCE SPECIFICATIONS**

Device Tested at: +V<sub>SUPPLY</sub> = +15V, -V<sub>SUPPLY</sub> = -15V, V<sub>REF</sub> = OPEN, GND = 0V, Unless Otherwise Specified.

D.C. PARAMETERS	SYMBOL	CONDITIONS	GROUP A SUBGROUPS	TEMPERATURE (°C)	MIN	MAX	UNITS
Switch "ON" Resistance	$I_{DS}$	$V_A = 0.8V, V_S = 10V, I_D = -1mA,$ All Unused Channels $V_A = 0.8V$	1	25	-	70	$\Omega$
			2, 3	-55 to 125	-	100	$\Omega$
		$V_A = 0.8V, V_S = -10V, I_D = 1mA,$ All Unused Channels $V_A = 0.8V$	1	25	-	70	$\Omega$
			2, 3	-55 to 125	-	100	$\Omega$
Source "OFF" Leakage Current	$I_{S(OFF)}$	$V_S = +14V, V_D = -14V, V_A = 2.4V,$ All Unused Channels $V_A = 2.4V,$ $V_D = +14V, V_S = -14V$	1	25	-5	5	nA
			2, 3	-55 to 125	-500	500	nA
		$V_S = -14V, V_D = +14V, V_A = 2.4V,$ All Unused Channels $V_A = 2.4V,$ $V_D = -14V, V_S = +14V$	1	25	-5	5	nA
			2, 3	-55 to 125	-500	500	nA
Drain "OFF" Leakage Current	$I_{D(OFF)}$	$V_D = -14V, V_S = +14V, V_A = 2.4V,$ All Unused Channels $V_A = 2.4V,$ $V_D = +14V, V_S = -14V$	1	25	-5	5	nA
			2, 3	-55 to 125	-500	500	nA
		$V_D = +14V, V_S = -14V, V_A = 2.4V,$ All Unused Channels $V_A = 2.4V,$ $V_D = -14V, V_S = +14V$	1	25	-5	5	nA
			2, 3	-55 to 125	-500	500	nA
Channel "ON" Leakage Current	$I_{D(ON)}$	$V_D = V_S = +14V, V_A = 0.8V,$ All Unused Channels $V_A = 0.8V,$ $V_D = V_S = -14V$	1	25	-5	5	nA
			2, 3	-55 to 125	-500	500	nA
		$V_D = V_S = -14V, V_A = 0.8V,$ All Unused Channels $V_A = 0.8V,$ $V_D = V_S = +14V$	1	25	-5	5	nA
			2, 3	-55 to 125	-500	500	nA
Low Level Input Current	$I_{AL}$	$V_{AL} = 0.8V$ All Channels $V_A = 2.4V$	1	25	-1.0	1.0	$\mu A$
			2, 3	-55 to 125	-1.0	1.0	$\mu A$
High Level Input Current	$I_{AH}$	$V_{AH} = 2.4V$ All Channels $V_{AH} = 4.0V$	1	25	-1.0	1.0	$\mu A$
			2, 3	-55 to 125	-1.0	1.0	$\mu A$
Supply Current	$+I_{CC}$	All Channels $V_A = 0V$	1	25	-	2.0	$\mu A$
			2, 3	-55 to 125	-	2.0	$\mu A$
		All Channels $V_A = 3V$	1	25	-	2.0	mA
			2, 3	-55 to 125	-	2.0	mA

## HI-200/883

**TABLE 1. D.C. ELECTRICAL PERFORMANCE SPECIFICATIONS (Continued)**

Device Tested at: +V<sub>SUPPLY</sub> = +15V, -V<sub>SUPPLY</sub> = -15V, V<sub>REF</sub> = OPEN, GND = 0V, Unless Otherwise Specified.

D.C. PARAMETERS	SYMBOL	CONDITIONS	GROUP A SUBGROUPS	TEMPERATURE (°C)	MIN	MAX	UNITS
Supply Current	-I <sub>CC</sub>	All Channels V <sub>A</sub> = 0V	1	25	-2.0	-	μA
			2, 3	-55 to 125	-2.0	-	μA
		All Channels V <sub>A</sub> = 3V	1	25	-2.0	-	μA
			2, 3	-55 to 125	-2.0	-	μA

**TABLE 2. A.C. ELECTRICAL PERFORMANCE SPECIFICATIONS**

Device Tested at: +V<sub>SUPPLY</sub> = +15V, -V<sub>SUPPLY</sub> = -15V, V<sub>REF</sub> = OPEN, GND = 0V, Unless Otherwise Specified.

PARAMETERS	SYMBOL	CONDITIONS	GROUP A SUB-GROUPS	TEMPERATURE (°C)	MIN	MAX	UNITS
Turn "ON" Time	t <sub>ON</sub>	C <sub>L</sub> = 35pF, R <sub>L</sub> = 1kΩ	9	25	-	500	ns
			10, 11	55 to 125	-	800	ns
Turn "OFF" Time	t <sub>OFF</sub>	C <sub>L</sub> = 33pF, R <sub>L</sub> = 1kΩ	9	25	-	500	ns
			10, 11	55 to 125	-	650	ns

**TABLE 3. ELECTRICAL PERFORMANCE SPECIFICATIONS (NOTE 1)**

Device Tested at: +V<sub>SUPPLY</sub> = +15V, -V<sub>SUPPLY</sub> = -15V, V<sub>REF</sub> = OPEN, GND = 0V

PARAMETERS	SYMBOL	CONDITIONS	NOTE	TEMPERATURE (°C)	MIN	MAX	UNITS
Address Capacitance	C <sub>A</sub>	f = 1MHz, V <sub>AL</sub> = 0V	1	25	-	20	pF
Switches Input Capacitance	C <sub>S</sub> (OFF)	f = 1MHz, V <sub>AH</sub> = 5V, Measured Source to GND	1	25	-	20	pF
Switch Output Capacitance	C <sub>D</sub> (OFF)	f = 1MHz, V <sub>AH</sub> = 5V, Measured Output to Ground	1	25	-	20	pF
	C <sub>D</sub> (ON)	f = 1MHz, V <sub>AL</sub> = 0V, Measured Output to Ground	1	25	-	30	pF
Drain to Source Capacitance	C <sub>DS</sub>	f = 1MHz, V <sub>AH</sub> = 5V	1	25	-	2.0	pF
Off Isolation	V <sub>ISO</sub>	f = 200kHz, V <sub>A</sub> = 2.4, R <sub>L</sub> = 1K, V <sub>GEN</sub> = 1V <sub>P-P</sub> , C <sub>L</sub> = 10pF	1	25	55	-	dB
Cross Talk	V <sub>CT</sub>	f = 200kHz, V <sub>A</sub> = 2.4, R <sub>L</sub> = 1K, V <sub>GEN</sub> = 1V <sub>P-P</sub> , C <sub>L</sub> = 10pF	1	25	60	-	dB
Charge Transfer Error	V <sub>CTE</sub>	f = 200kHz, V <sub>A</sub> = 0 to 4V, C <sub>L</sub> = 0.01μF	1	25	-10	10	mV

NOTE:

- Parameters listed in Table 2 are controlled via design or process parameters and are not directly tested at final production. These parameters are lab characterized upon initial design release, or upon design changes. These parameters are guaranteed by characterization based upon data from multiple production runs which reflect lot to lot and within lot variation.

**TABLE 4. ELECTRICAL TEST REQUIREMENTS**

MIL-STD-883 TEST REQUIREMENTS	SUBGROUPS (Tables 1 and 2)
Interim Electrical Parameters (Pre Burn-in)	1
Final Electrical Test Parameters	1 (Note 2), 2, 3, 9, 10, 11
Group A Test Requirements	1, 2, 3, 9, 10, 11
Groups C & D Endpoints	1

NOTE:

- PDA applies to Subgroup 1 only.

Test Circuits

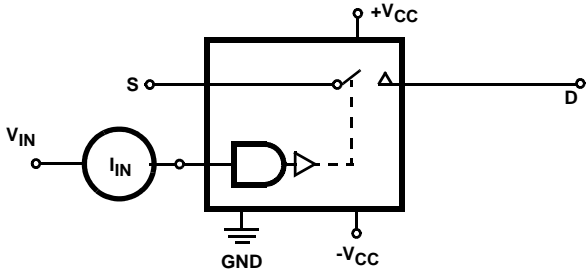


FIGURE 1. INPUT LEAKAGE CURRENT

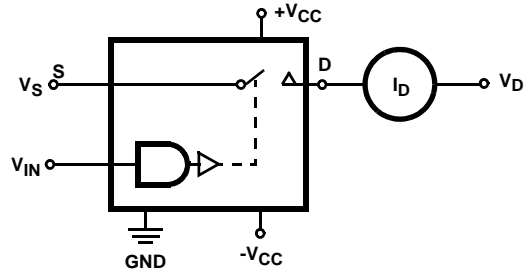


FIGURE 2.  $I_D$  (OFF)

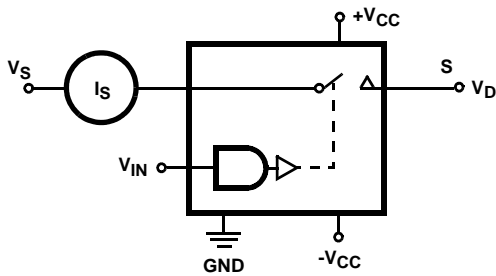


FIGURE 3.  $I_S$  (OFF)

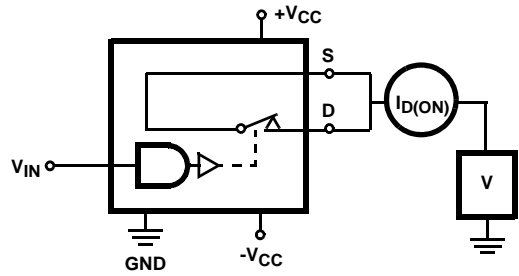


FIGURE 4.  $I_D$  (ON)

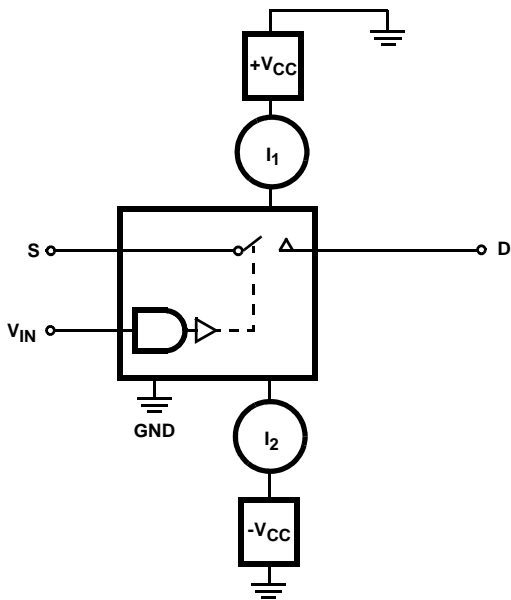


FIGURE 5. SUPPLY CURRENTS

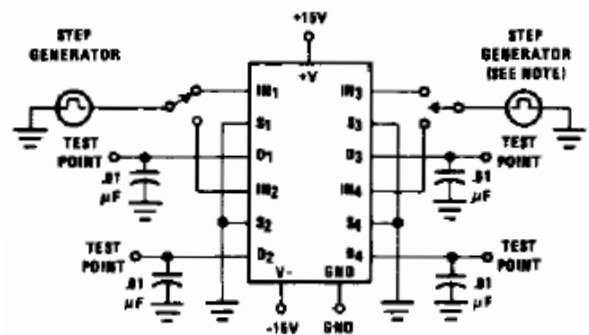


FIGURE 6. CHARGE TRANSFER ERROR

Test Circuits (Continued)

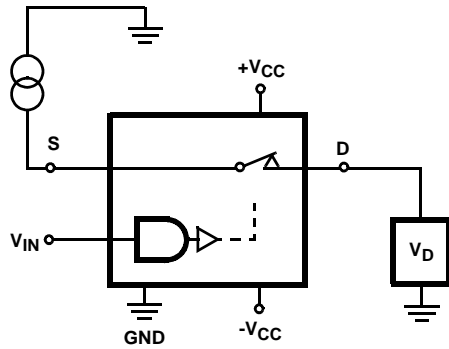


FIGURE 7. R<sub>DS</sub>

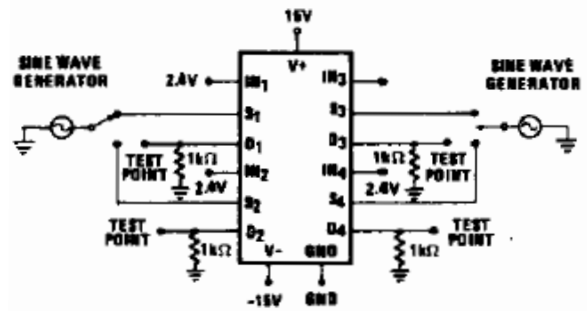


FIGURE 8. OFF CHANNEL ISOLATION

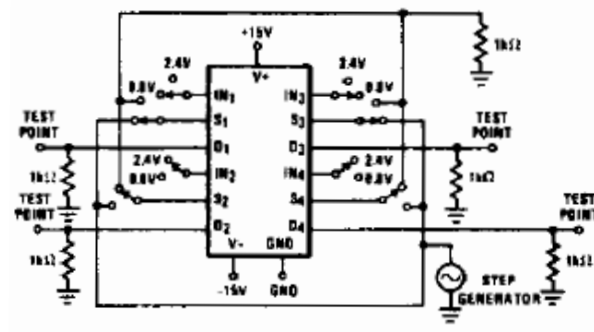


FIGURE 9. CROSSTALK BETWEEN CHANNELS

Switching Waveforms

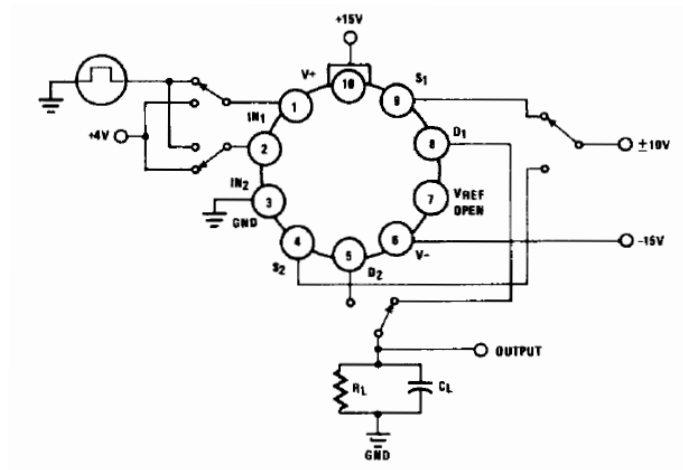


FIGURE 10.

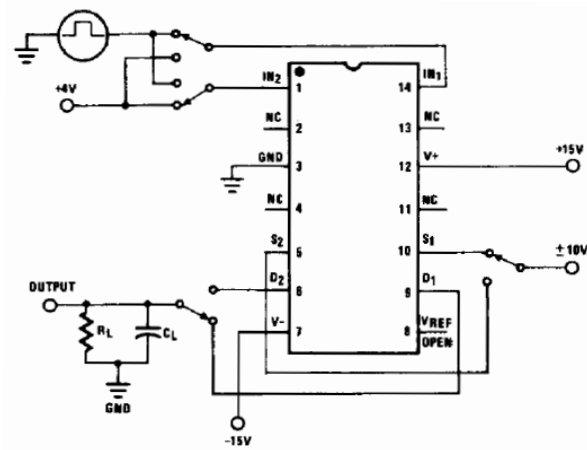


FIGURE 11.

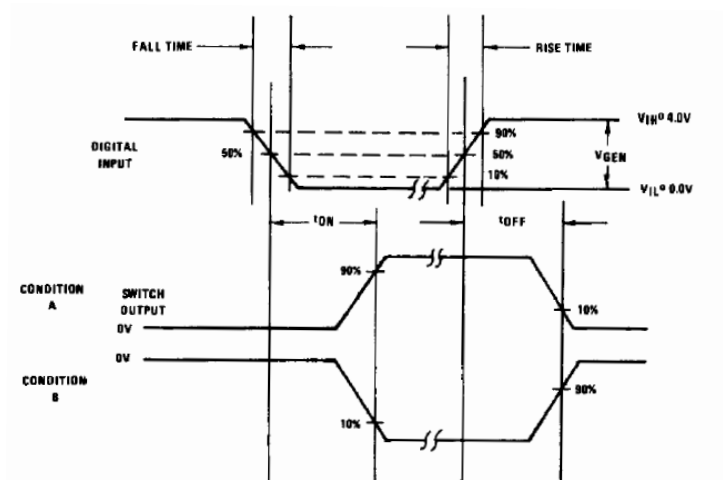


FIGURE 12.

Burn-In Circuits

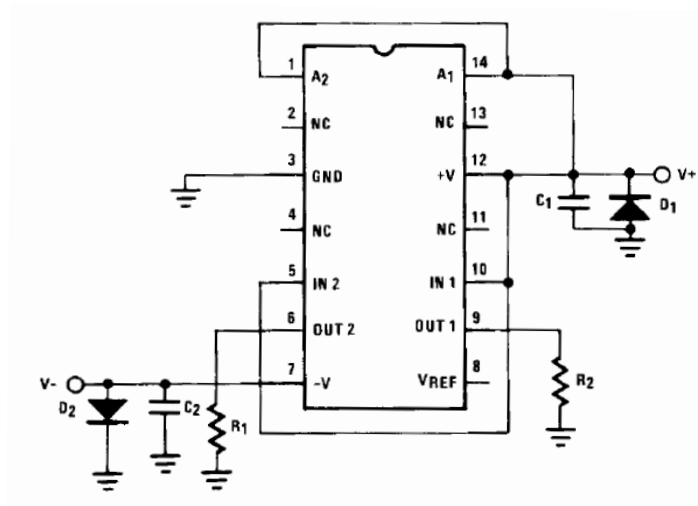


FIGURE 13. HI-200/883 CERAMIC DIP

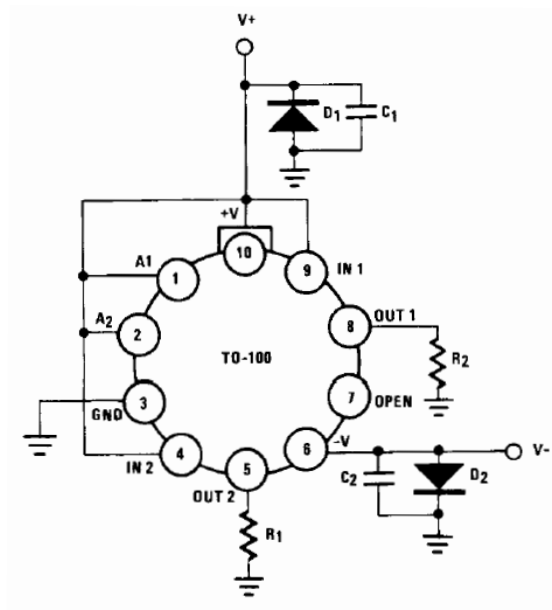


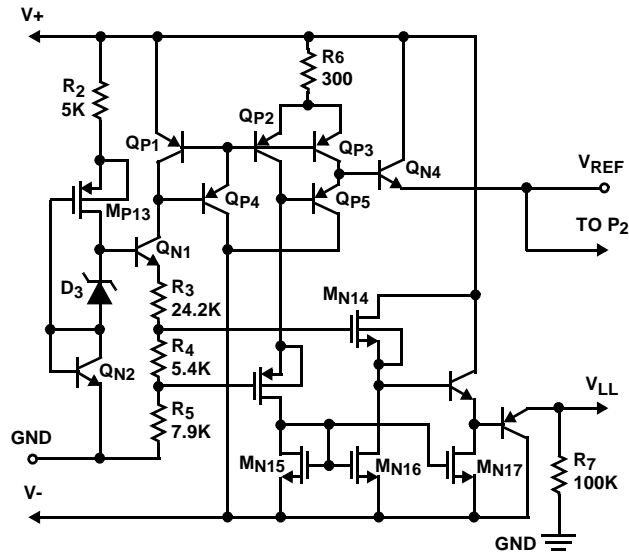
FIGURE 14. HI-200/883 METAL CAN (TO-99)

NOTES:

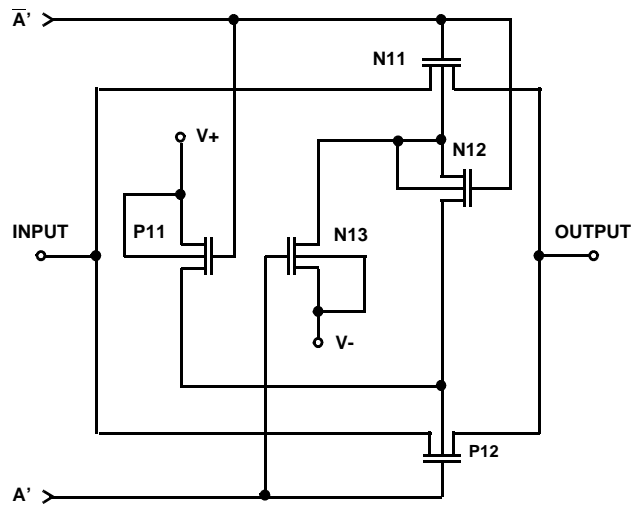
3.  $R_1 = R_2 = 10k\Omega$
4.  $C_1 = C_2 = 0.01\mu F$  (per socket) or  $0.1\mu F$  (per row)
5.  $D_1 = D_2 = IN4002$  or equivalent
6.  $|(V+) - (V-)| = 30V$

Schematic Diagrams

TTL/CMOS REFERENCE CIRCUIT  $V_{REF}$  CELL



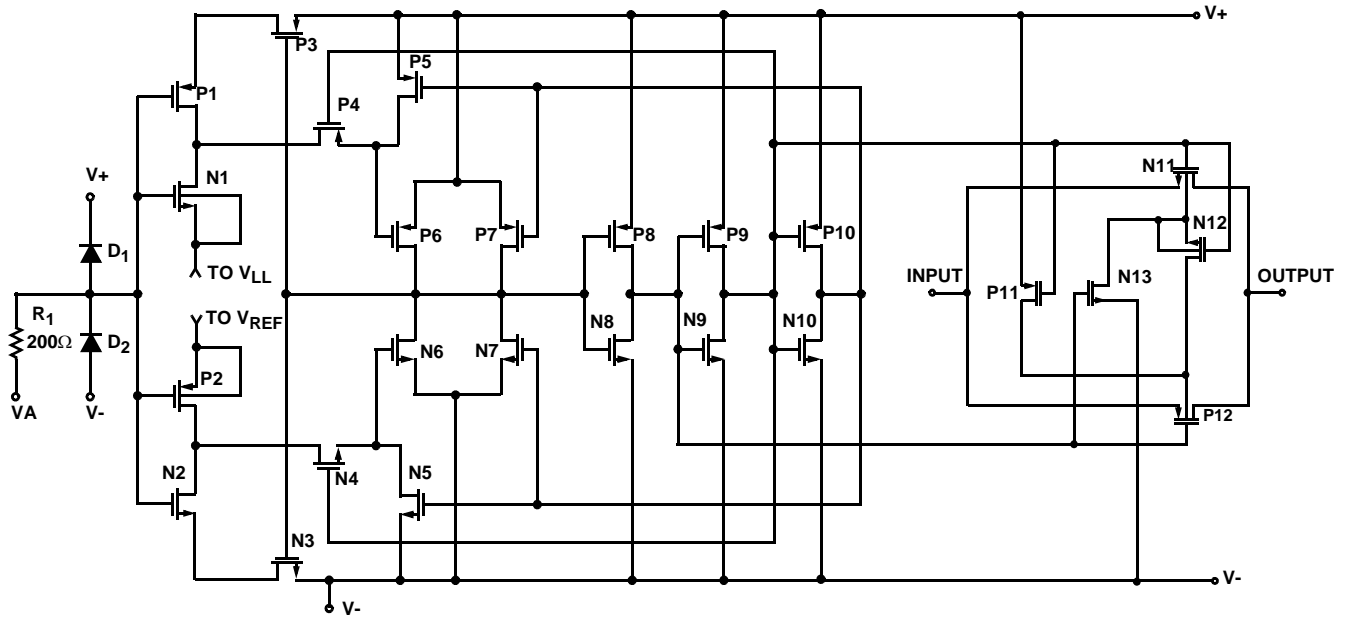
SWITCH CELL





Schematic Diagrams (Continued)

DIGITAL INPUT BUFFER AND LEVEL SHIFTER



Test Circuits and Waveforms  $T_A = 25^\circ\text{C}$ ,  $V_{\text{SUPPLY}} = \pm 15\text{V}$ ,  $V_{\text{AH}} = 2.4\text{V}$ ,  $V_{\text{AL}} = 0.8\text{V}$  and  $V_{\text{REF}} = \text{Open}$

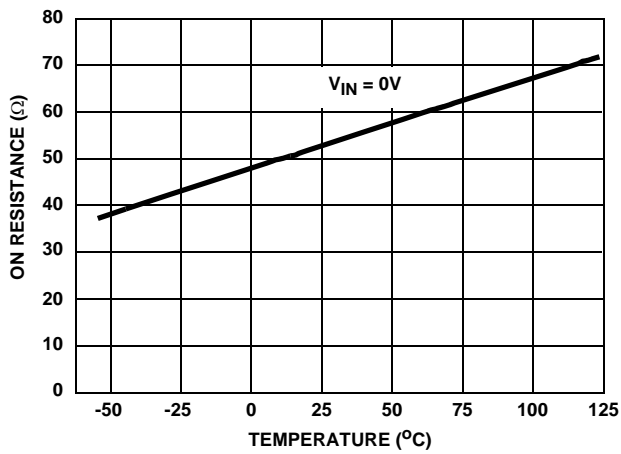


FIGURE 15. ON RESISTANCE vs TEMPERATURE

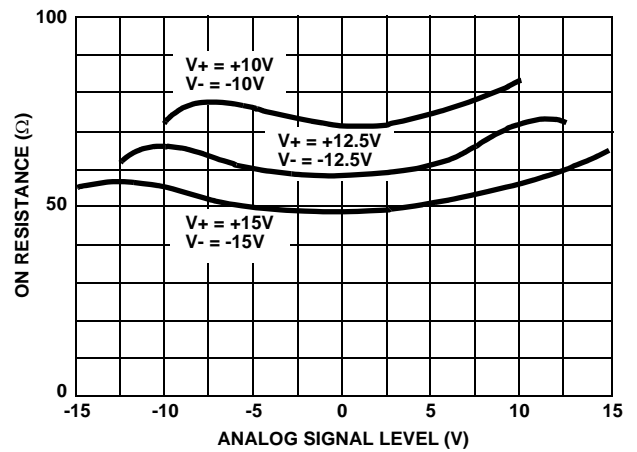


FIGURE 16. ON RESISTANCE vs ANALOG SIGNAL LEVEL AND POWER SUPPLY VOLTAGE

**Test Circuits and Waveforms**  $T_A = 25^{\circ}\text{C}$ ,  $V_{\text{SUPPLY}} = \pm 15\text{V}$ ,  $V_{\text{AH}} = 2.4\text{V}$ ,  $V_{\text{AL}} = 0.8\text{V}$  and  $V_{\text{REF}} = \text{Open}$  (Continued)

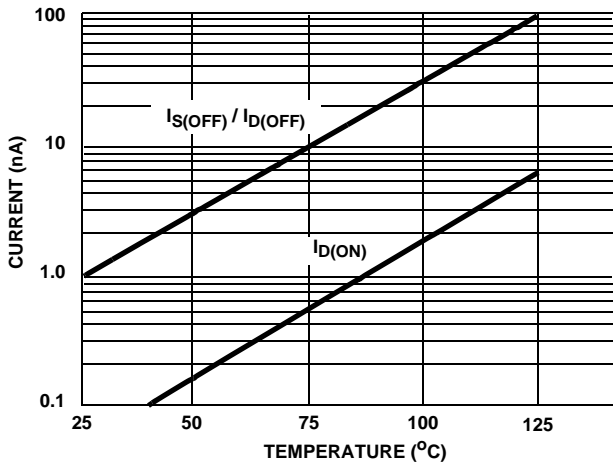


FIGURE 17. LEAKAGE CURRENT vs TEMPERATURE

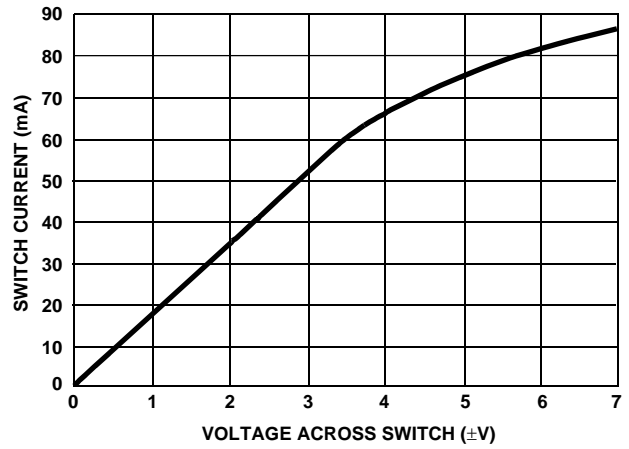


FIGURE 18. SWITCH CURRENT vs VOLTAGE

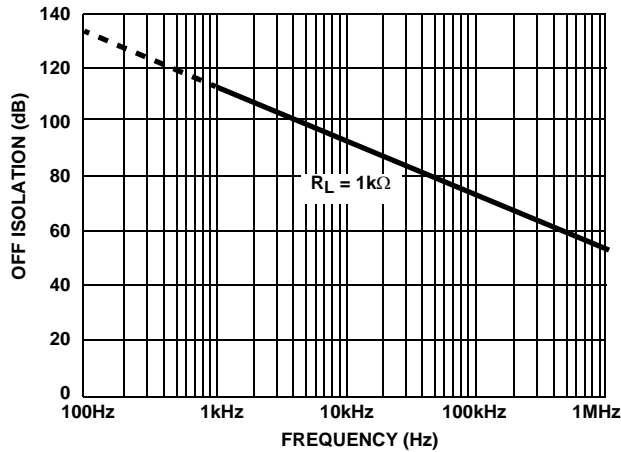


FIGURE 19. OFF ISOLATION vs FREQUENCY

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**Die Characteristics**

**DIE DIMENSIONS:**

54 mils x 79mils x 19 mils

**METALLIZATION:**

Type: Aluminum  
 Thickness:  $16k\text{\AA} \pm 2k\text{\AA}$

**GLASSIVATION:**

Type: Nitride over Silox  
 Silox Thickness:  $12k\text{\AA} \pm 2k\text{\AA}$   
 Nitride Thickness:  $3.5k\text{\AA} \pm 1k\text{\AA}$

**DIE ATTACH:**

Material: Gold/Silicon Eutectic Alloy  
 Temperature: Ceramic DIP - 460°C (Max)  
 Metal Can - 420°C (Max)

**WORST CASE CURRENT DENSITY:**

$2 \times 10^5 \text{ A/cm}^2$  at 25mA

**Metallization Mask Layout**

