HOLT INTEGRATED CIRCUITS INC

HI-8281

January 2001

ARINC 429 LINE DRIVER AND DUAL RECEIVER

GENERAL DESCRIPTION

The HI-8281 device from Holt Integrated Circuits is a silicon gate CMOS device for interfacing a 16-bit parallel data bus directly to the ARINC 429 serial bus. The device provides two receivers, an independent transmitter and line driver capability in a single package. The receiver input circuitry and logic are designed to meet the ARINC 429 specifications for loading, level detection, timing, and protocol. The transmitter section provides the ARINC 429 communication protocol and the line driver circuits provide the ARINC 429 output levels.

The 16-bit parallel data bus exchanges the 32-bit ARINC data word in two steps when either loading the transmitter or interrogating the receivers. The data bus interfaces with CMOS and TTL.

Timing of all the circuitry begins with the master clock input, CLK. For ARINC 429 applications, the master clock frequency is 1 MHz.

Each independent receiver monitors the data stream with a sampling rate 10 times the data rate. The sampling rate is software selectable at either 1MHz or 125KHz. The results of a parity check are available as the 32nd ARINC bit. The HI-8281 examines the null and data timings and will reject erroneous patterns. For example, with a 125 KHz clock selection, the data frequency must be between 10.4 KHz and 15.6 KHz.

The transmitter has a First In, First Out (FIFO) memory to store 8 ARINC words for transmission. The data rate of the transmitter is software selectable by dividing the master clock, CLK, by either 10 or 80. The master clock is used to set the timing of the ARINC transmission within the required resolution.

APPLICATIONS

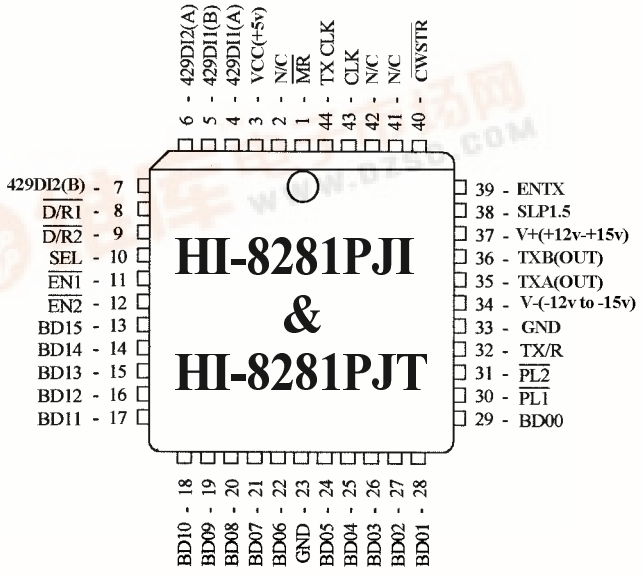
- Avionics data communication
- Serial to parallel conversion
- Parallel to serial conversion

FEATURES

- ARINC specification 429 compatible
- Direct receiver and transmitter interface to ARINC bus in a single device.
- 16-Bit parallel data bus.
- Timing control 10 times the data rate
- Selectable data clocks
- Receiver error rejection per ARINC specification 429
- Automatic transmitter data timing
- Self test mode
- Parity functions
- Low power
- Industrial & full military temperature ranges

PIN CONFIGURATION (Top View)

44 - PIN PLASTIC PLCC



(See page 4-27 for additional pin configuration)

PIN DESCRIPTION

SIGNAL	FUNCTION	DESCRIPTION
VCC	POWER	+5V ±5%
V+	POWER	+12V ± 5% or +15V ± 10%
V-	POWER	-12V ± 5% or -15V ± 10%
429DI1 (A)	INPUT	ARINC receiver 1 positive input
429DI1 (B)	INPUT	ARINC receiver 1 negative input
429DI2 (A)	INPUT	ARINC receiver 2 positive input
429DI2 (B)	INPUT	ARINC receiver 2 negative input
$\overline{D/R1}$	OUTPUT	Receiver 1 data ready flag
$\overline{D/R2}$	OUTPUT	Receiver 2 data ready flag
SEL	INPUT	Receiver data byte selection (0 = BYTE 1) (1 = BYTE 2)
$\overline{EN1}$	INPUT	Data Bus control, enables receiver 1 data to outputs
$\overline{EN2}$	INPUT	Data Bus control, enables receiver 2 data to outputs if $\overline{EN1}$ is high
BD15	I/O	Data Bus
BD14	I/O	Data Bus
BD13	I/O	Data Bus
BD12	I/O	Data Bus
BD11	I/O	Data Bus
BD10	I/O	Data Bus
BD09	I/O	Data Bus
BD08	I/O	Data Bus
BD07	I/O	Data Bus
BD06	I/O	Data Bus
GND	POWER	0 V - both pins must be connected
BD05	I/O	Data Bus
BD04	I/O	Data Bus
BD03	I/O	Data Bus
BD02	I/O	Data Bus
BD01	I/O	Data Bus
BD00	I/O	Data Bus
TX/R	OUTPUT	Transmitter ready flag. Goes low when ARINC word loaded into FIFO. Goes high After transmission and FIFO empty.
$\overline{PL1}$	INPUT	Latch enable for byte 1 entered from data bus to transmitter FIFO.
$\overline{PL2}$	INPUT	Latch enable for byte 2 entered from data bus to transmitter FIFO. Must follow $\overline{PL1}$.
TXA(OUT)	OUTPUT	Line driver output - A side
TXB(OUT)	OUTPUT	Line driver output - B side
ENTX	INPUT	Enable Transmission
$\overline{CWSTR}$	INPUT	Clock for control word register
CLK	INPUT	Master Clock input
TX CLK	OUTPUT	Transmitter Clock equal to Master Clock (CLK), divided by either 10 or 80.
$\overline{MR}$	INPUT	Master Reset, active low
SLP1.5	INPUT	Logic input to control the slope of the differential output signal. HIGH = 1.5 µs

FUNCTIONAL DESCRIPTION

CONTROL WORD REGISTER

The HI-8282 contains 10 data flip flops whose D inputs are connected to the data bus and clocks connected to $\overline{CWSTR}$. Each flip flop provides options to the user as follows:

DATA BUS PIN	FUNCTION	CONTROL	DESCRIPTION
BDO5	SELF TEST	0 = ENABLE	If enabled, an internal connection is made passing 429DO and $\overline{429DO}$ to the receiver logic inputs
BDO6	RECEIVER 1 DECODER	1 = ENABLE	If enabled, ARINC bits 9 and, 10 must match the next two control word bits
BDO7	-	-	If Receiver 1 Decoder is enabled, the ARINC bit 9 must match this bit
BDO8	-	-	If Receiver 1 Decoder is enabled, the ARINC bit 10 must match this bit
BDO9	RECEIVER 2 DECODER	1 = ENABLE	If enabled, ARINC bits 9 and 10 must match the next two control word bits
BD10	-	-	If Receiver 2 Decoder is enabled, then ARINC bit 9 must match this bit
BD11	-	-	If Receiver 2 Decoder is enabled, then ARINC bit 10 must match this bit
BD12	INVERT XMTR PARITY	1 = ENABLE	Logic 0 enables normal odd parity and Logic 1 enables even parity output in transmitter 32nd bit
BD13	XMTR DATA CLK SELECT	0 = ÷10 1 = ÷80	CLK is divided either by 10 or 80 to obtain XMTR data clock
BD14	RCVR DTA CLK SELECT	0 = ÷10 1 = ÷80	CLK is divided either by 10 or 80 to obtain RCVR data clock

ARINC 429 DATA FORMAT

The following table shows the bit positions in exchanging data with the receiver or the transmitter. ARINC bit 1 is the first bit transmitted or received.

BYTE 1																
DATA BUS	BD 15	BD 14	BD 13	BD 12	BD 11	BD 10	BD 09	BD 08	BD 07	BD 06	BD 05	BD 04	BD 03	BD 02	BD 01	BD 00
ARINC BIT	13	12	11	10	9	31	30	32	1	2	3	4	5	6	7	8

BYTE 2																
DATA BUS	BD 15	BD 14	BD 13	BD 12	BD 11	BD 10	BD 09	BD 08	BD 07	BD 06	BD 05	BD 04	BD 03	BD 02	BD 01	BD 00
ARINC BIT	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14

THE RECEIVERS

ARINC BUS INTERFACE

Figure 1 shows the input circuit for each receiver. The ARINC 429 specification requires the following detection levels:

STATE	DIFFERENTIAL VOLTAGE
ONE	+6.5 Volts to +13 Volts
NULL	+2.5 Volts to -2.5 Volts
ZERO	-6.5 Volts to -13 Volts

The HI-8282 guarantees recognition of these levels with a common mode Voltage with respect to GND less than ±4V for the worst case condition (4.75V supply and 13V signal level).

The tolerances in the design guarantee detection of the above levels, so the actual acceptance ranges are slightly larger. If the ARINC signal is out of the actual acceptance ranges, including the nulls, the chip rejects the data.

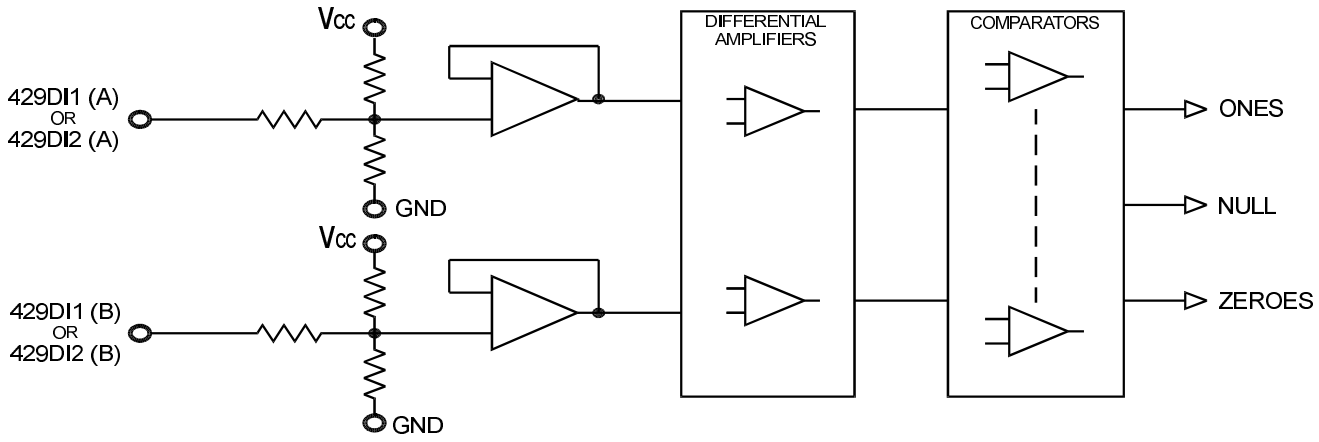


FIGURE 1. **ARINC RECEIVER INPUT**

FUNCTIONAL DESCRIPTION (con't)

RECEIVER LOGIC OPERATION

Figure 2 shows a block diagram of the logic section of each receiver.

BIT TIMING

The ARINC 429 specification contains the following timing specification for the received data:

	HIGH SPEED	LOW SPEED
BIT RATE	100K BPS ± 1%	12K -14.5K BPS
PULSE RISE TIME	1.5 ± 0.5 µsec	10 ± 5 µsec
PULSE FALL TIME	1.5 ± 0.5 µsec	10 ± 5 µsec
PULSEWIDTH	5 µsec ± 5%	34.5 to 41.7 µsec

Again the HI-8282 accepts signals that meet these specifications and rejects outside the tolerances. The way the logic operation achieves this is described below:

1. Key to the performance of the timing checking logic is an accurate 1MHz clock source. Less than 0.1% error is recommended.

2. The sampling shift registers are 10 bits long and must show three consecutive Ones, Zeros or Nulls to be considered valid data. Additionally, for data bits, the One or Zero in the upper bits of the sampling shift registers must be followed by a Null in the lower bits within the data bit time. For a Null in the word gap, three consecutive Nulls must be found in both the upper and lower bits of the sampling shift register. In this manner the minimum pulse width is guaranteed.

3. Each data bit must follow its predecessor by not less than 8 samples and no more than 12 samples. In this manner the bit rate is checked. With exactly 1MHz input clock frequency, the acceptable data bit rates are as follows:

	HIGH SPEED	LOW SPEED
DATA BIT RATE MIN	83K BPS	10.4K BPS
DATA BIT RATE MAX	125K BPS	15.6K BPS

4. TheWordGaptimersamplestheNullshiftregister every 10 input clocks (80 for low speed) after the last data bit of a Valid reception. If the Null is present, theWordGapcounter Is incremented. A count of 3 will enable the next reception.

RECEIVER PARITY

The receiver parity circuit counts Ones received, including the parity bit, ARINC bit 32. If the result is odd, then "0" will appear in the 32nd bit.

RETRIEVING DATA

Once 32 valid bits are recognized, the receiver logic generates an End of Sequence (EOS). If the receiver decoder is enabled and the 9th and 10th ARINC bits match the control word program bits or if the receiver decoder is disabled, then EOS clocks the data ready flag flip flop to a "1", $\overline{D/R1}$ or $\overline{D/R2}$ (or both) will go low. The data flag for a receiver will remain low until after both ARINC bytes from that receiver are retrieved. This is accomplished by activating $\overline{EN}$ with SEL, the byte selector, low to retrieve the first byte and activating $\overline{EN}$ with SEL high to retrieve the second byte. $\overline{EN1}$ retrieves data from receiver 1 and $\overline{EN2}$ retrieves data from receiver 2.

If another ARINC word is received, and a new EOS occurs before the two bytes are retrieved, the data is overwritten by the new word.

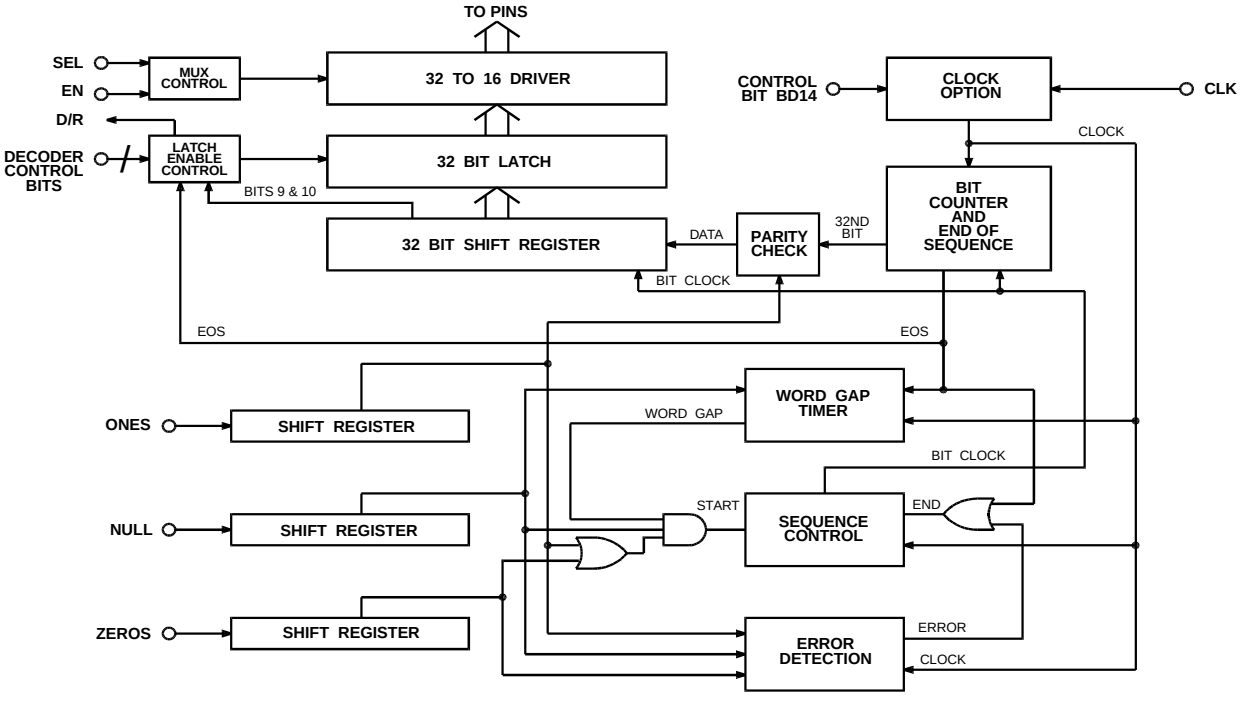


FIGURE 2. **RECEIVER BLOCK DIAGRAM**

FUNCTIONAL DESCRIPTION (con't)

TRANSMITTER

A block diagram of the transmitter section is shown in Figure 3.

FIFO OPERATION

The FIFO is loaded sequentially by first pulsing PL1 to load byte 1 and then $\overline{PL2}$ to load byte 2. The control logic automatically loads the 31 bit word in the next available position of the FIFO. If TX/R, the transmitter ready flag is high (FIFO empty), then 8 words, each 31 bits long, may be loaded. If TX/R is low, then only the available positions may be loaded. If all 8 positions are full, the FIFO ignores further attempts to load data.

DATA TRANSMISSION

When ENTX goes high, enabling transmission, the FIFO positions are incremented with the top register loading into the data transmission shift register. Within 2.5 data clocks the first data bit appears at either 429DO or $\overline{429DO}$. The 31 bits in the data transmission shift register are presented sequentially to the outputs in the ARINC 429 format with the following timing:

	HIGH SPEED	LOW SPEED
ARINC DATA BIT TIME	10 Clocks	80 Clocks
DATA BIT TIME	5 Clocks	40 Clocks
NULL BIT TIME	5 Clocks	40 Clocks
WORD GAP TIME	40 Clocks	320 Clocks

The word counter detects when all loaded positions are transmitted and sets the transmitter ready flag, TX/R, high.

TRANSMITTER PARITY

The parity generator counts the ONES in the 31-bit word. If the BD12 control word bit is set low, the 32nd bit transmitted will make parity odd. If the control bit is high the parity is even.

SELF TEST

If the BD05 control word bit is set low, 429DO or $\overline{429DO}$ become inputs to the receiver bypassing the interface circuitry.

SYSTEMOPERATION

The two receivers are independent of the transmitter. Therefore, control of data exchanges are strictly at the option of the user. The only restrictions are:

1. The received data may be overwritten if not retrieved within one ARINC word cycle.

2. The FIFO can store 8 words maximum and ignores attempts to load addition data if full.

3. Byte 1 of the transmitter data must be loaded first.

4. Either byte of the received data may be retrieved first. Both bytes must be retrieved to clear the data ready flag.

5. After ENTX, transmission enable ,goes high it cannot go low until TX/R, transmitter readyflag, goes high. Otherwise, one ARINC word is lost during transmission.

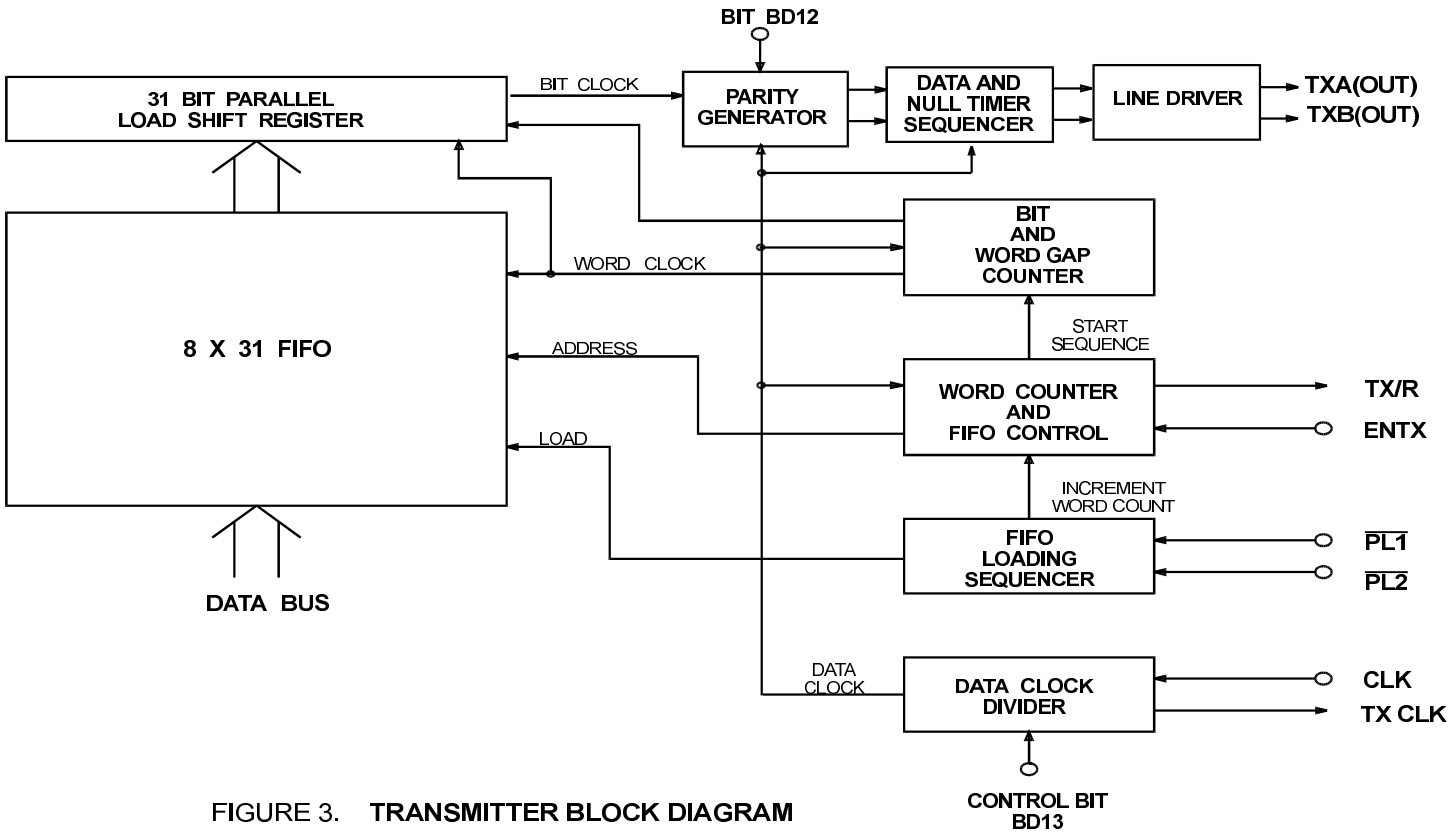


FIGURE 3. **TRANSMITTER BLOCK DIAGRAM**

FUNCTIONAL DESCRIPTION (con't)

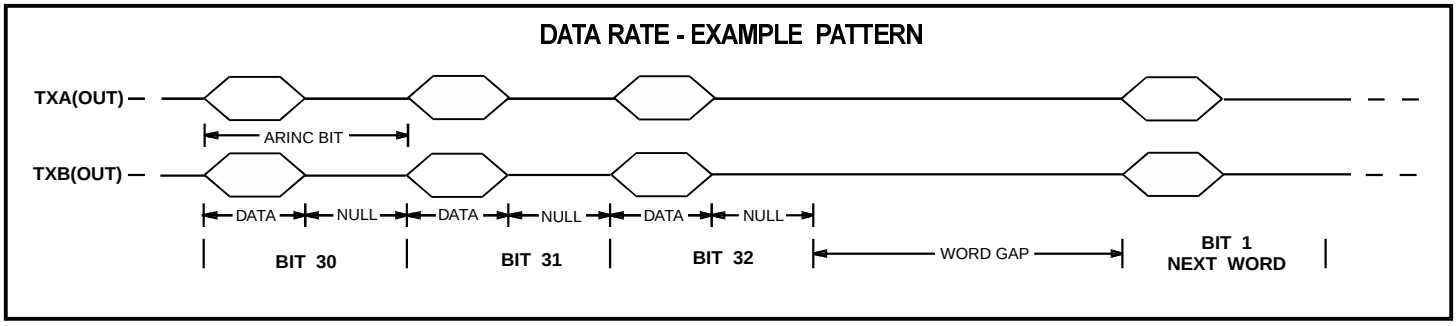
LINE DRIVER OPERATION

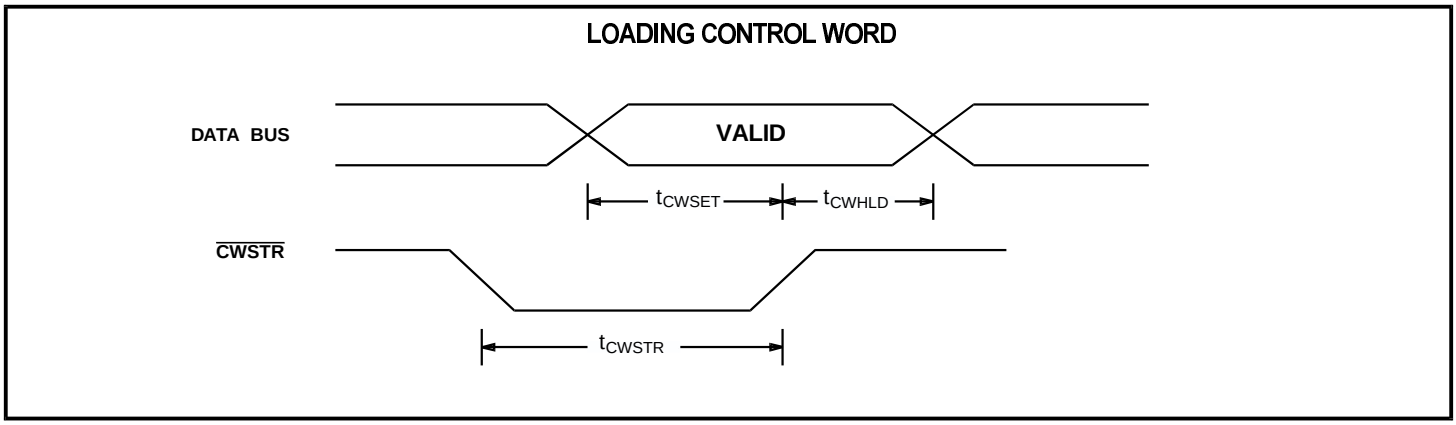
The line driver in the HI-8281 is designed to directly drive the ARINC 429 bus. The two ARINC outputs (TXA(OUT) and TXB(OUT)) provide a differential voltage to produce a +10 volt One, a -10 volt Zero, and a 0 volt Null. The device incorporates on board zeners to translate internal CMOS levels to ARINC specified amplitudes. A logic input (SLP1.5) is provided to control the slope of the differential output signal. No additional hardware is required to control the slope. A HIGH on SLP1.5 causes a slope of 1.5 µs on the ARINC outputs; a LOW on SLP1.5 causes a slope of 10 µs. Timing is set by on-chip resistor and capacitor and tested to be within ARINC requirements. The HI-8281 has 37.5 ohms in series with each line driver output.

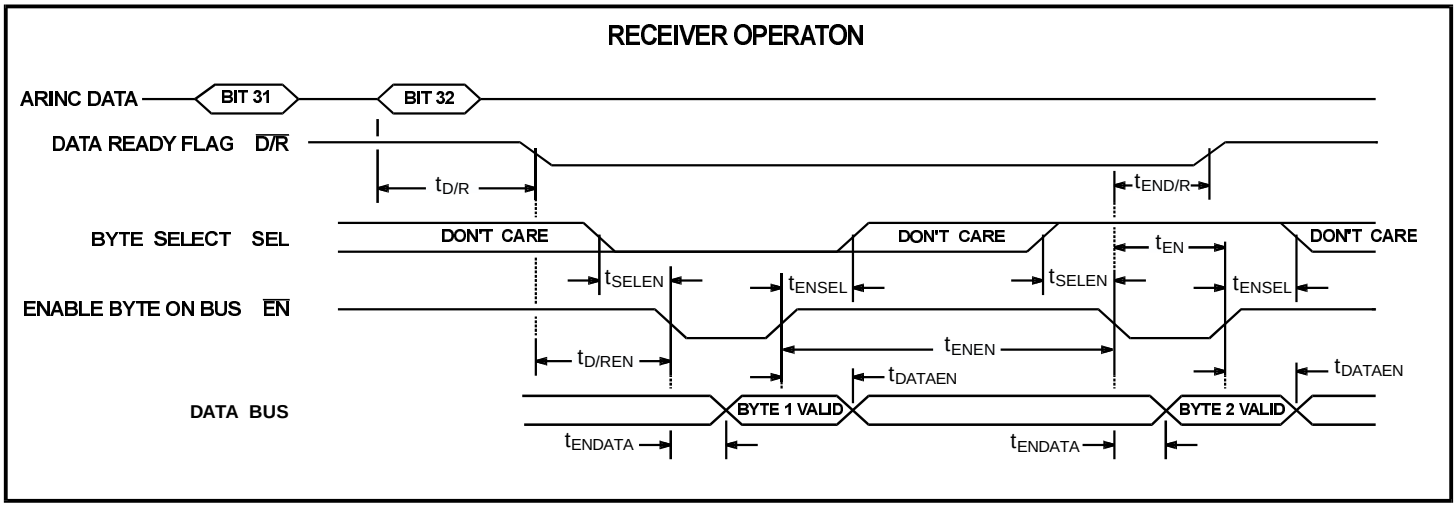
REPEATER OPERATION

Repeater mode of operation allows a data word that has been received by the HI-8281 to be placed directly into its FIFO for transmission. Repeater operation is similar to normal receiver operation. In normal operation, either byte of a received data word may be read from the receiver latches first by use of SEL input. During repeater operation however, the lower byte of the data word must be read first. This is necessary because, as the data is being read, it is also being loaded into the FIFO and the transmitter FIFO is always loaded with the lower byte of the data word first. Signal flow for repeater operation is shown in the Timing Diagrams section.

TIMING DIAGRAMS

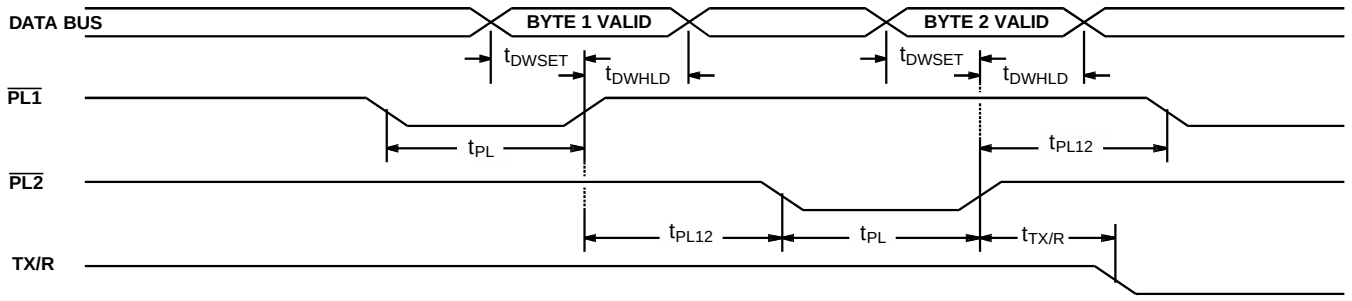




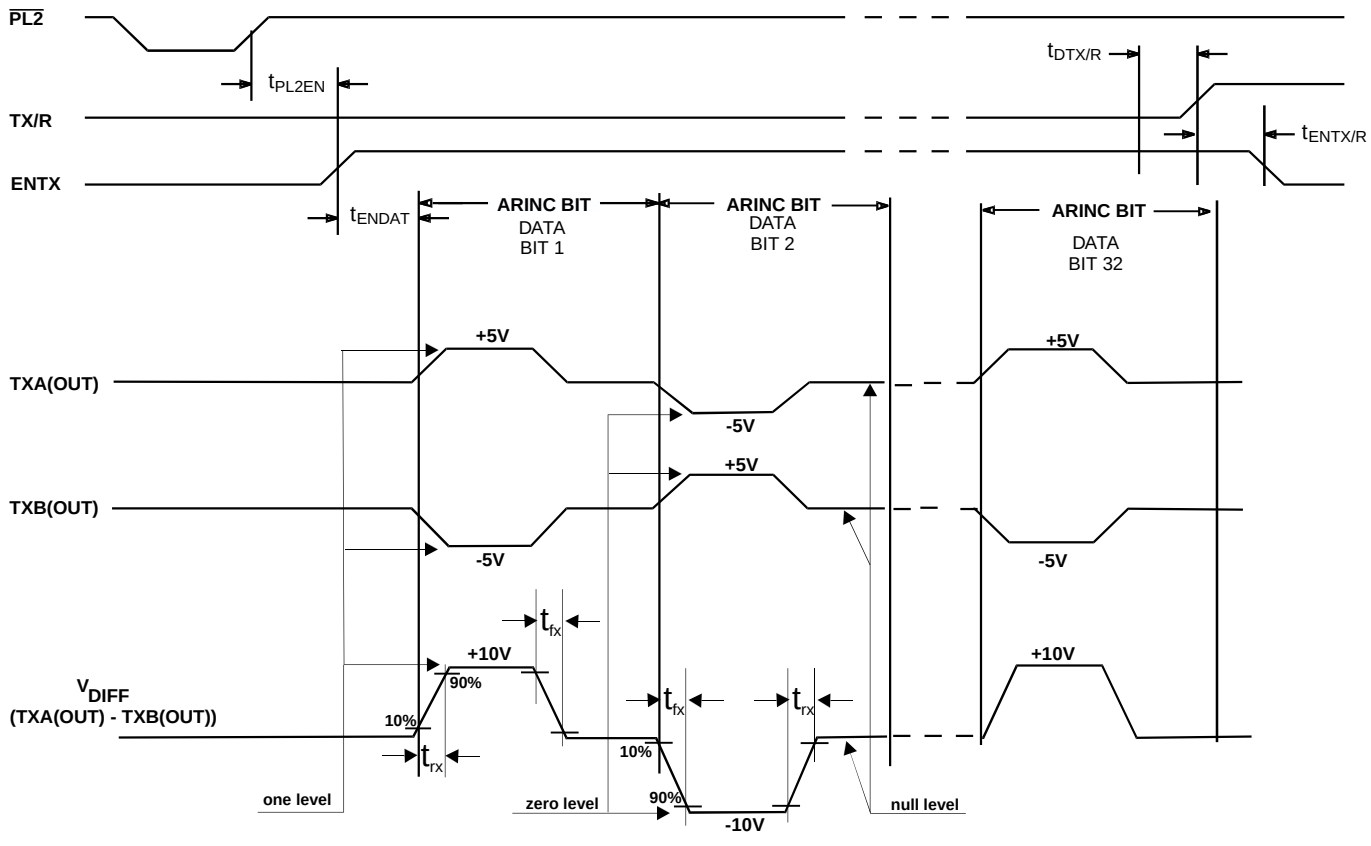


TIMING DIAGRAMS (con't)

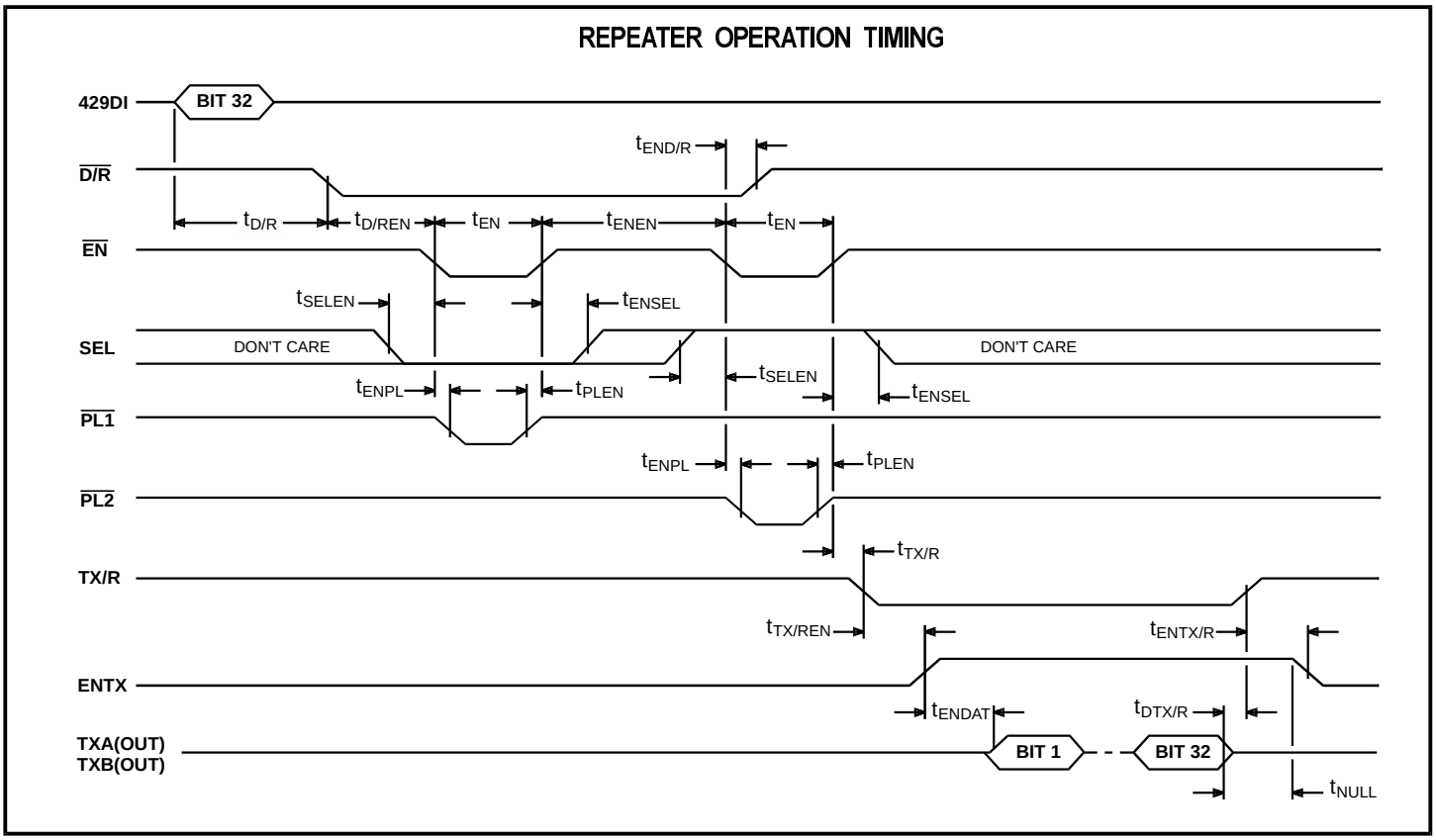
TRANSMITTER OPERATION



TRANSMITTING DATA



TIMING DIAGRAMS (con't)



ABSOLUTE MAXIMUM RATINGS

Supply Voltages Vcc ..... -0.3V to +7V V+ ..... 20V V- ..... -20V	Power Dissipation at 25C Plastic PLCC ..... 1.5 W, derate 10mW/°C Ceramic J-LEAD CERQUAD ..... 1.0 W, derate 7mW/°C
Voltage at pins 4, 5, 6 and 7 ..... -29V to +29V	DC Current Drain per pin ..... ±10mA
Voltage at pin 38 ..... -0.3 to V+ +0.3V	Storage Temperature Range: ..... -65°C to +150°C
Voltage at any other pin ..... -0.3V to Vcc +0.3V	Operating Temperature Range: (Industrial) ..... -40°C to +85°C (Military) ..... -55°C to +125°C

NOTE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC ELECTRICAL CHARACTERISTICS

Vcc = 5V ±5%, V+ = 12V to 15V, V- = -12V to -15V, GND = 0V, TA = Operating Temperature Range (unless otherwise specified).

PARAMETER		SYMBOL	CONDITIONS	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT
ARINC INPUTS - Pins 4, 5, 6 & 7							
Differential Input Voltage:	ONE	V_{IH}	Pins 4 to 5, 6 to 7: Common mode voltage less than ±4V with respect to GND	6.5	10.0	13.0	V
	ZERO	V_{IL}		-13.0	-10.0	-6.5	V
	NULL	V_{NUL}		-2.5	0	2.5	V
Input Resistance:	Differential	R_I		12			KΩ
	To GND	R_G		12	27		KΩ
	To Vcc	R_H		12	27		KΩ
Input Current:	Input Sink	I_{IH}				200	µA
	Input Source	I_{IL}		-450			µA
Input Capacitance: (Guaranteed but not tested)	Differential	C_I	Pins 4 to 5, 6 to 7			20	pF
	To GND	C_G				20	pF
	To Vcc	C_H				20	pF
BI-DIRECTIONAL INPUTS - Pins 13 - 22, 24 - 29							
Input Voltage:	Input Voltage HI	V_{IH}		2.1			V
	Input Voltage LO	V_{IL}				0.7	V
Input Current:	Input Sink	I_{IH}				1.5	µA
	Input Source	I_{IL}		-1.5			µA
OTHER INPUTS - Pins 1, 8 - 12, 30, 31, 39, 40 & 43							
Input Voltage:	Input Voltage HI	V_{IH}		3.5			V
	Input Voltage LO	V_{IL}				0.7	V
Input Current:	Input Sink	I_{IH}				10	µA
	Input Source	I_{IL}		-20			
INPUT - SLP1.5, PIN 38							
Input Voltage	Input Voltage HI	V_{IH}		2.1	-	V+	V
	Input Voltage LO	V_{IL}		-	-	0.5	V
Input Current	Input Sink	I_{IH}	V_{IN} = 0V			0.1	µA
	Input Source	I_{IL}	V_{IN} = 5V			0.1	µA

DC ELECTRICAL CHARACTERISTICS (con't)

Vcc = 5V ±5%, V+ = 12V to 15V, V- = -12V to -15V, GND = 0V, TA = Operating Temperature Range (unless otherwise specified).

PARAMETER	SYMBOL	CONDITIONS	LIMITS			UNIT
			MIN	TYP	MAX	
ARINC OUTPUTS - Pins 35 & 36						
ARINC output voltage One or zero Null	 V_{DOUt} V_{NOUT}	 no load and magnitude at pin " " " " " "	 4.50 -0.25	 5.00	 5.50 0.25	 V V
ARINC output current	I_{OUT}		80			mA
OTHER OUTPUTS - Pins 13-22, 24-29, 32 & 34						
Output Voltage: Logic "1" Output Voltage Logic "0" Output Voltage	V_{OH} V_{OL}	I_{OH} = -1.5mA I_{OL} = 1.8mA	2.7		 0.4	V V
Output Current: Output Sink (Bi-directional Pins) Output Source	I_{OL} I_{OH}	V_{OUT} = 0.4V V_{OUT} = V_{CC} - 0.4V	3.0 1.5			mA mA
Output Current: Output Sink (All Other Outputs) Output Source	I_{OL} I_{OH}	V_{OUT} = 0.4V V_{OUT} = V_{CC} - 0.4V	3.6 1.5			mA mA
Output Capacitance:	C_O			15		pF
Operating Supply Current						
VCC, Pin 3:	I_{CC1}				20	mA
V+, Pin 37:	I_{DD1}				16	mA
V-, Pin 34:	I_{EE1}				16	mA

AC ELECTRICAL CHARACTERISTICS

Vcc = 5V, V+=12V to 15V, V- = -12V to -15V,GND = 0V, TA = Oper. Temp. Range and fclk = 1MHz ±0.1% with 60/40 duty cycle

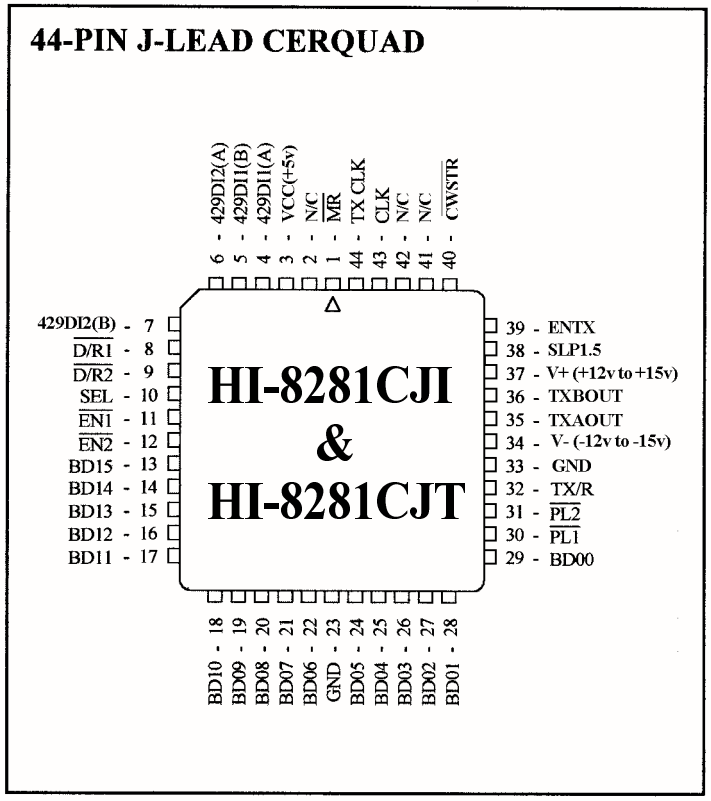
PARAMETER	SYMBOL	LIMITS			UNITS
		MIN	TYP	MAX	
CONTROL WORD TIMING					
Pulse Width - $\overline{CWSTR}$	t_{CWSTR}	130			ns
Setup - DATA BUS Valid to $\overline{CWSTR}$ HIGH	t_{CWSET}	140			ns
Hold - $\overline{CWSTR}$ HIGH to DATA BUS Hi-Z	t_{CWHLD}	0			ns
RECEIVER TIMING					
Delay - Start ARINC 32nd Bit to $\overline{D/R}$ LOW: High Speed	$t_{D/R}$			16	µs
Low Speed	$t_{D/R}$			128	µs
Delay - $\overline{D/R}$ LOW to $\overline{EN}$ L0W	$t_{D/REN}$	0			ns
Delay - $\overline{EN}$ LOW to $\overline{D/R}$ HIGH	$t_{END/R}$			200	ns
Setup - SEL to $\overline{EN}$ L0W	t_{SELEN}	20			ns
Hold - SEL to $\overline{EN}$ HIGH	t_{ENSEL}	50			ns
Delay - $\overline{EN}$ L0W to DATA BUS Valid	t_{ENDATA}			200	ns
Delay - $\overline{EN}$ HIGH to DATA BUS Hi-Z	t_{DATAEN}			30	ns
Pulse Width - $\overline{EN1}$ or $\overline{EN2}$	t_{EN}	240			ns
Spacing - $\overline{EN}$ HIGH to next $\overline{EN}$ L0W	t_{ENEN}	50			ns
FIFO TIMING					
Pulse Width - $\overline{PL1}$ or $\overline{PL2}$	t_{PL}	200			ns
Setup - DATA BUS Valid to $\overline{PL}$ HIGH	t_{DWSET}	110			ns
Hold - $\overline{PL}$ HIGH to DATA BUS Hi-Z	t_{DWHLD}	20			ns
Spacing - $\overline{PL1}$ or $\overline{PL2}$	t_{PL12}	0			ns
Delay - $\overline{PL2}$ HIGH to TX/R LOW	$t_{TX/R}$			840	ns
TRANSMISSION TIMING					
Spacing - $\overline{PL2}$ HIGH to ENTX HIGH	t_{PL2EN}	0			µs
Delay - 32nd ARINC Bit to TX/R HIGH	$t_{DTX/R}$			400	ns
Spacing - TX/R HIGH to ENTX L0W	$t_{ENTX/R}$	0			ns
LINE DRIVER OUTPUT TIMING					
Delay - ENTX HIGH to TXA(OUT) or TXB(OUT): High Speed	t_{ENDAT}			27	µs
Delay - ENTX HIGH to TXA(OUT) or TXB(OUT): Low Speed	t_{ENDAT}			216	µs
Line driver transition differential times:					
(High Speed, Pin 38 - Logic 1) high to low	t_{fx}	1.0	1.5	2.0	µs
low to high	t_{rx}	1.0	1.5	2.0	µs
(Low Speed, Pin 38 = Logic 0) high to low	t_{fx}	5.0	10	15	µs
low to high	t_{rx}	5.0	10	15	µs

AC ELECTRICAL CHARACTERISTICS (con't)

Vcc = 5V, V+ = 12V to 15V, V- = -12V to -15V,GND = 0V, TA= Oper. Temp. Range and fclk = 1MHz ±0.1% with 60/40 duty cycle

PARAMETER	SYMBOL	LIMITS			UNITS
		MIN	TYP	MAX	
REPEATER OPERATION TIMING					
Delay - $\overline{EN}$ LOW to $\overline{PL}$ LOW	t_{ENPL}	0			ns
Hold - $\overline{PL}$ HIGH to $\overline{EN}$ HIGH	t_{PLEN}	0			ns
Delay - TX/R LOW to ENTX HIGH	$t_{TX/REN}$	0			ns
Master Reset Pulse Width	t_{MR}	400			ns
ARINC Data Rate and Bit Timing				± 1%	

ADDITIONAL HI-8281 PIN CONFIGURATION



(See page 4-23 for additional pin configuration)

ORDERING INFORMATION

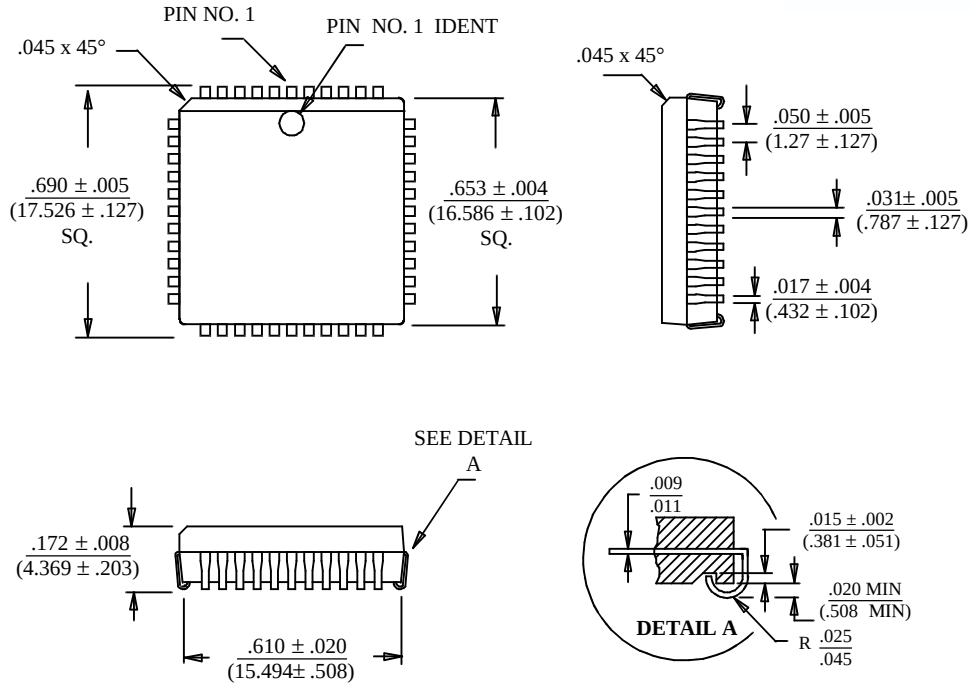
PART NUMBER	PACKAGE DESCRIPTION	TEMPERATURE RANGE	FLOW	BURN IN	LEAD FINISH
HI-8281PJI	44 PIN PLASTIC J LEAD	-40°C TO +85°C	I	NO	SOLDER
HI-8281PJT	44 PIN PLASTIC J LEAD	-55°C TO +125°C	T	NO	SOLDER
HI-8281CJI	44 PIN CERQUAD J LEAD	-40°C TO +85°C	I	NO	SOLDER
HI-8281CJT	44 PIN CERQUAD J LEAD	-55°C TO +125°C	T	NO	SOLDER

HOLT INC.
INTEGRATED CIRCUITS

HI-8281 PACKAGE DIMENSIONS

inches (millimeters)

44-PIN PLASTIC J-LEAD PLCC



44-PIN CERQUAD J-LEAD