

0.25A/50V Octal Low Side Power Driver with Serial Bus Control

June 1996

Features

- Eight Open Drain - NDMOS Low Side Drivers Each Capable of 250mA
- High Voltage Power BiMOS with Low Idle and Standby Current
- Over-Voltage Clamp Protection
 - Each Output 50V Typical
- Serial Data Input, Parallel Output Power Drive
- Common Enable for Output Drivers and Data Storage Register
- -40°C to 85°C Operating Range

Applications

- Automotive and Industrial Systems
- Solenoids, Relays and Lamp Drivers
- Logic and μ P Controlled Drivers
- Robotic Controls

Description

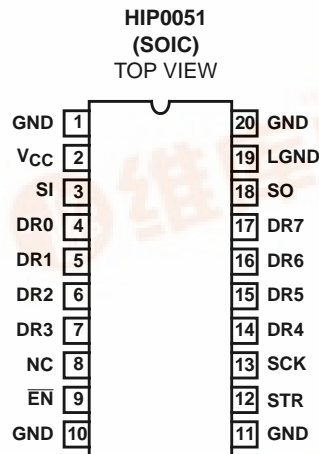
The HIP0051 is a logic controlled, eight channel Octal Low Side Power Driver. As shown in the Block Diagram, the outputs are controlled via the serial data interface which allows the data to be shifted out, allowing control of other cascaded serial devices.

The HIP0051 is fabricated in a Power BiMOS IC process, and is intended for use in automotive and other applications having a wide range of temperature and electrical stress conditions. It is particularly suited for driving lamps, displays, relays, and solenoids in applications where low operating power, high breakdown voltage, and high output current at high temperature is required.

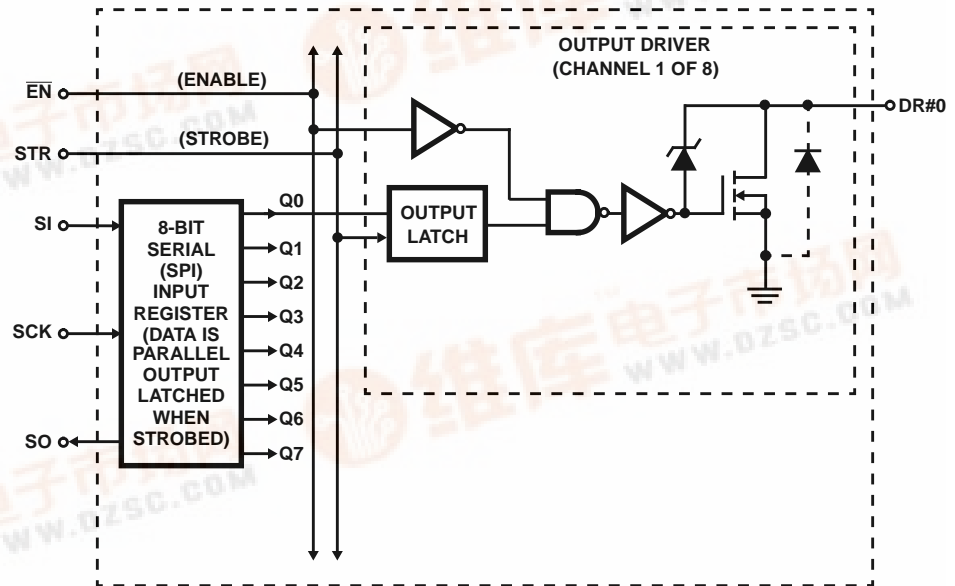
Ordering Information

PART NUMBER	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
HIP0051IB	-40 to 85	20 Ld SOIC	M20.3

Pinout



Block Diagram



Specifications HIP0051

Absolute Maximum Ratings

Output Voltage, V_{OUT} (Note 1)	-0.3V to 40V
Input Voltage, V_{IN}	-0.3V to $V_{CC} + 0.3V$
Logic Supply Voltage, V_{CC}	-0.3V to +7V
Output Clamp Energy, 25°C (5ms Pulse)	75mJ
Continuous Output Load Current, I_{LOAD} (Each Output)	0.25A
Continuous Output Current, I_{LOAD} (All Outputs ON, Note 2)	1.69A
Peak Output Current	
Each Output, Other Outputs OFF	±2A
Peak Avalanche Current (3ms duration)	1A

Thermal Information

Thermal Resistance (Typical, Note 3)	θ_{JA} (°C/W)
SOIC Package	100
Maximum Junction Temperature	150°C
Maximum Storage Temperature Range, T_{STG}	-55°C to 150°C
Maximum Lead Temperature (Soldering 10s)	300°C
(SOIC Lead Tips Only)	

Operating Conditions

Operating Ambient Temperature Range, T_A	-40°C to 85°C
Operating Logic Supply Voltage Range, V_{CC}	+4.5V to +5.5V
Power Output Driver Voltage Range	0 to V_{OC}
Max. Supply Current, with 100mA each Output	100µA
Max. Supply Current, with No Load, Outputs OFF	100µA
Logic Input High Voltage	0.7 $\times V_{CC}$
Logic Input Low Voltage	0.2 $\times V_{CC}$
Typical Output $R_{DS(ON)}$ Channel Resistance	2Ω
Typical Output Rise Time	.4µs
Typical Output Fall Time	10µs

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTES:

- The MOSFET Output Drain is internally clamped with a Drain-to-Gate zener diode that turns-on the MOSFET; holding the Drain at the Output Clamp voltage V_{OC} .
- The maximum continuous current with all outputs on is limited by package dissipation. At 25°C ambient temperature, the maximum equal current with all outputs ON is 211mA in each output for a total of 1.69A. At a maximum ambient temperature of $T_A = 85°C$ and $r_{DS(ON)(Max)} = 3.5\Omega$, each output is limited to 152mA and the total current for all 8 outputs ON is $8 \times 152mA = 1.22A$.
- θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Electrical Specifications $V_{CC} = 4.5V$ to $5.5V$, $V_{BATT} = 8V$ to $16V$, $T_A = -40°C$ to $85°C$, Unless Otherwise Specified.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
OUTPUTS DRIVERS (DR0 TO DR7)						
Output Channel Resistance	$r_{DS(ON)}$	Output Current = 200mA, $T_A = 85°C$		2	3.5	Ω
Output Clamping Voltage	V_{OC}	Outputs OFF	42	50	58	V
Output Clamping Energy	E_{OC}	5ms Pulse, $T_A = 25°C$	75	190		mJ
Peak Output Load Currents, Short Duration	I_{PEAK}	100µs Duration, Each Output, all Outputs ON, Duty Cycle ≤ 2%	0.85	-	-	A
Cold Start-up Lamp Currents	I_{LAMP}	5ms Duration, Each Output, all Outputs ON, Duty Cycle ≤ 17%	0.3	-	-	A
Output OFF Leakage Current	I_{OFF}	Output Voltage = 40V, $T_A = 85°C$	-	-0.2	10	µA
Output Rise Time	t_{rise}	Load = 75Ω, 0.01µF (RC in Parallel), $V_{BATT} = 18V$	0.5	4	30	µs
Output Fall Time	t_{fall}		0.5	10	30	µs
Output Delay from Strobe, High to Low Output Transition	t_{DHL}		1	4	10	µs
Output Delay from Strobe, Low to High Output Transition	t_{DLH}		0.2	2.6	10	µs
LOGIC SUPPLY						
Logic Supply Current, Loaded	I_{CC}	All Outputs ON, 200mA Load at each Output	-	-	100	µA
Logic Supply Current, No Load	I_{CC}	All Outputs OFF	-	-	100	µA

Specifications HIP0051

Electrical Specifications $V_{CC} = 4.5V$ to $5.5V$, $V_{BATT} = 8V$ to $16V$, $T_A = -40^{\circ}C$ to $85^{\circ}C$, Unless Otherwise Specified. **(Continued)**

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
LOGIC INPUTS (\overline{EN}, SI, SCK, STR)						
Threshold Voltage at Falling Edge	V_{T-}	$V_{CC} = 5V \pm 10\%$	$0.2V_{CC}$	$0.3V_{CC}$	-	V
Threshold Voltage at Rising Edge	V_{T+}	$V_{CC} = 5V \pm 10\%$	-	$0.6V_{CC}$	$0.7V_{CC}$	V
Hysteresis Voltage	V_H	$V_{T+} - V_{T-}$	0.85	1.4	2.25	V
Leakage Current	I_{LIN}	$V_{CC} = 5V$	-10	-0.2	10	μA
Leakage Current	I_{LIN}	$V_{CC} = 0V$	-10	-0.1	10	μA
SERIAL DATA CLOCK (SCK)						
Frequency	f_{SCK}		-	-	1.6	MHz
Pulse Width High	$t_{W(CKH)}$		175	27	-	ns
Pulse Width Low	$t_{W(CKL)}$		175	27	-	ns
SERIAL DATA IN (SI)						
Input Setup Time	t_{SUI}		-	1.1	75	ns
Input Hold Time	T_{HI}		-	1.5	75	ns
STROBE (STR)						
Strobe Pulse Width	$t_{W(S)}$		150	12	-	ns
Min. Clock to Strobe Delay	$t_{D(CS)}$		75	5	-	ns
SERIAL DATA OUT (SO)						
Low Level Output Voltage	V_{OL}	Sink Current = 1.6mA	-	0.2	0.4	V
High Level Output Voltage	V_{OH}	Source Current = -1.6mA	3.7	4.4	-	V
Propagation Delay	$t_{P(CD)}$		75	260	-	ns

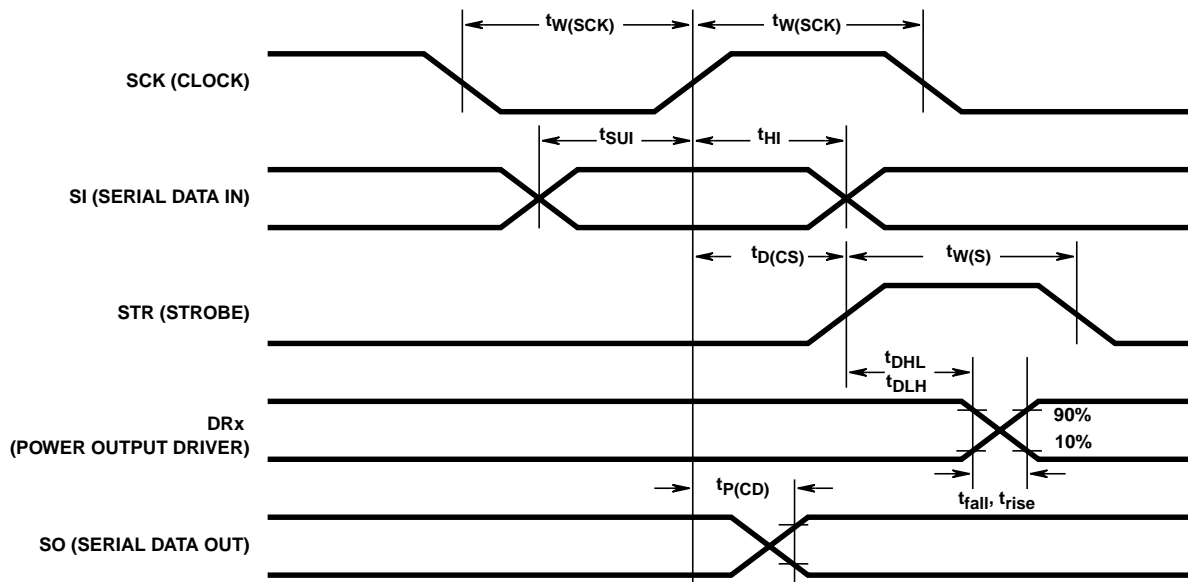
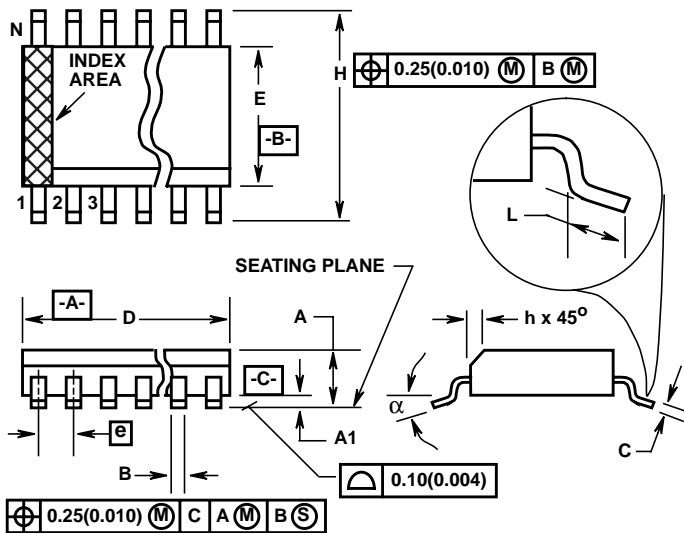


FIGURE 1. LOGIC TIMING CONTROL SPECIFICATIONS

HIP0051

Small Outline Plastic Packages (SOIC)



M20.3 (JEDEC MS-013-AC ISSUE C) 20 LEAD WIDE BODY SMALL OUTLINE PLASTIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.0926	0.1043	2.35	2.65	-
A1	0.0040	0.0118	0.10	0.30	-
B	0.013	0.0200	0.33	0.51	9
C	0.0091	0.0125	0.23	0.32	-
D	0.4961	0.5118	12.60	13.00	3
E	0.2914	0.2992	7.40	7.60	4
e	0.050 BSC		1.27 BSC		-
H	0.394	0.419	10.00	10.65	-
h	0.010	0.029	0.25	0.75	5
L	0.016	0.050	0.40	1.27	6
N	20		20		7
alpha	0°	8°	0°	8°	-

NOTES:

1. Symbols are defined in the "MO Series Symbol List" in Section 2.2 of Publication Number 95.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Dimension "D" does not include mold flash, protrusions or gate burrs. Mold flash, protrusion and gate burrs shall not exceed 0.15mm (0.006 inch) per side.
4. Dimension "E" does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.25mm (0.010 inch) per side.
5. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
6. "L" is the length of terminal for soldering to a substrate.
7. "N" is the number of terminal positions.
8. Terminal numbers are shown for reference only.
9. The lead width "B", as measured 0.36mm (0.014 inch) or greater above the seating plane, shall not exceed a maximum value of 0.61mm (0.024 inch)
10. Controlling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact.

Rev. 0 12/93

All Intersil semiconductor products are manufactured, assembled and tested under **ISO9000** quality systems certification.

Intersil products are sold by description only. Intersil Corporation reserves the right to make changes in circuit design and/or specifications at any time without notice. Accordingly, the reader is cautioned to verify that data sheets are current before placing orders. Information furnished by Intersil is believed to be accurate and reliable. However, no responsibility is assumed by Intersil or its subsidiaries for its use; nor for any infringements of patents or other rights of third parties which may result from its use. No license is granted by implication or otherwise under any patent or patent rights of Intersil or its subsidiaries.

For information regarding Intersil Corporation and its products, see web site <http://www.intersil.com>