

Half Amp High Side Driver with Overload Protection

December 1997

Features

- Over Operating Range.....-40°C to 125°C
 - V_{SAT} at 0.6A 1.0V Max
 - Power Supply Range 4.5V to 25V
- Over-Voltage Shutdown Protected
- Negative Output Voltage Clamp
- Over-Current Limiting
- Thermal Limiting Protection
- Load Dump..... 60VPEAK
- Reverse Battery Protection.....To -16V
- CMOS/TTL Logic Level Control Input

Applications

- Motor Driver/Controller
- Driver for Solenoids, Relays & Lamps
- MOSFET and IGBT Driver
- Driver for Temperature Controller

Ordering Information

PART NUMBER	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
HIP1031AS	-40 to 125	5 Ld TS-001AA SIP	Z5.067C

Description

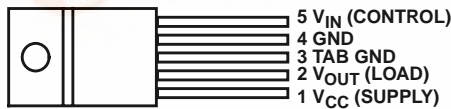
The HIP1031 is a High Side Driver Power Integrated Circuit designed to switch power supply voltage to an output load. It is the equivalent of a PNP pass transistor operated as a protected high side current switch in the saturated ON state with low forward voltage drop at the maximum rated current. It has low output leakage and low idle current in the OFF state.

The Functional Block Diagram for the HIP1031 shows the protection control circuit functions of over-current, overvoltage and over-temperature. A small metal resistor senses overcurrent in the power supply path of the pass transistor and load. Overvoltage detection and shutdown of the output driver occurs when a comparator determines that the supply voltage has exceeded a comparator reference level. Over-temperature is sensed from a V_{BE} differential sense element that is thermally close to the output drive transistor. In addition to the input detected overvoltage protection, negative peak voltage of an inductive load is clamped with an internal zener diode. An internal bandgap supply voltage source provides a stable voltage reference over the chip operating temperature range, providing bias and reference control for the protection circuits.

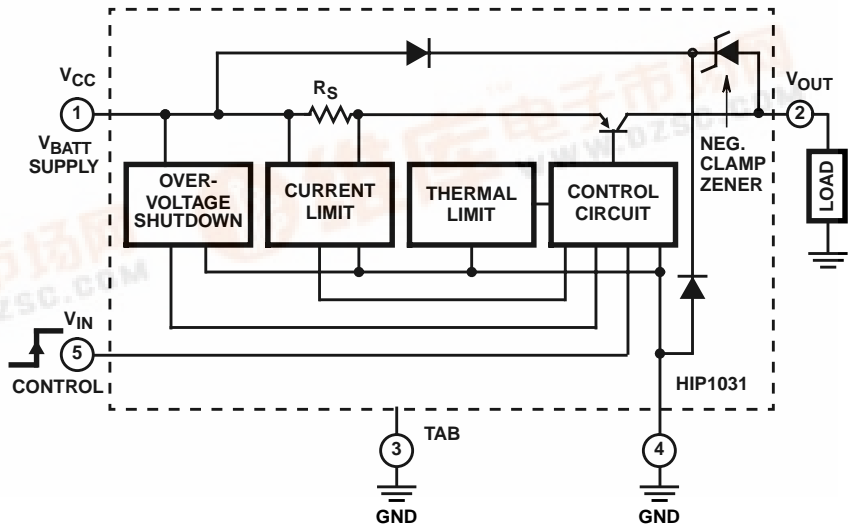
The HIP1031 is particularly well suited for driving lamps, relays, and solenoids in automotive and industrial control applications where voltage and current overload protection at high temperatures is required. The HIP1031 is supplied in a 5 lead TS-001AA Power SIP package.

Pinout

HIP1031 (SIP)
TOP VIEW



Functional Block Diagram



HIP1031

Absolute Maximum Ratings

Supply Voltage, V_{CC}	See O.V. Shutdown Limit, V_{OVSD}
Input Voltage, V_{IN} (Note 1)	-0.8V to +7V
Load Current, I_{OUT}	Internally Limiting
Load Dump (Survival)	$\pm 60V_{PEAK}$
Reverse Battery	-16V

Operating Conditions

Temperature Range	-40°C to 125°C
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CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTES:

- The Input Control Voltage, V_{IN} , may range from -0.85V to +7V for a V_{CC} supply voltage of 0V to +25V.
- θ_{JA} is measured with the component mounted on an evaluation PC board in free air.
- The worst case thermal resistance, θ_{JC} for the SIP TS-001AA 5 pin package is 4°C/W. The calculation for dissipation and junction temperature rise due to dissipation is:

$$P_D = (V_{CC} - V_{OUT})(I_{OUT}) + (V_{CC})(I_{CCMAX} - I_{OUT}) \text{ or } (V_{CC})(I_{CCMAX}) - (V_{OUT})(I_{OUT})$$

$$T_J = T_{AMBIENT} + (P_D)(\theta_{JC}) \text{ for an infinite Heat Sink.}$$

Refer to Figure 1 for Derating based on Dissipation and Thermal Resistance. Derating from 150°C is based on the reciprocal of thermal resistance, $\theta_{JC} + \theta_{HS}$. For example: Where $\theta_{JC} = 4^\circ\text{C/W}$ and given $\theta_{HS} = 6^\circ\text{C/W}$ as the thermal resistance of an external Heat Sink, the junction-to-air thermal resistance, $\theta_{JA} = 10^\circ\text{C/W}$. Therefore, for the maximum allowed dissipation, derate 0.1W/°C for each degree from T_{AMB} to the maximum rated junction temperature of 150°C. If $T_{AMB} = 100^\circ\text{C}$, the maximum P_D is $(150 - 100) \times 0.1\text{W/}^\circ\text{C} = 5\text{W}$.

Electrical Specifications $T_A = -40^\circ\text{C}$ to 125°C , $V_{IN} = 2\text{V}$, $V_{CC} = +12\text{V}$, Unless Otherwise Specified

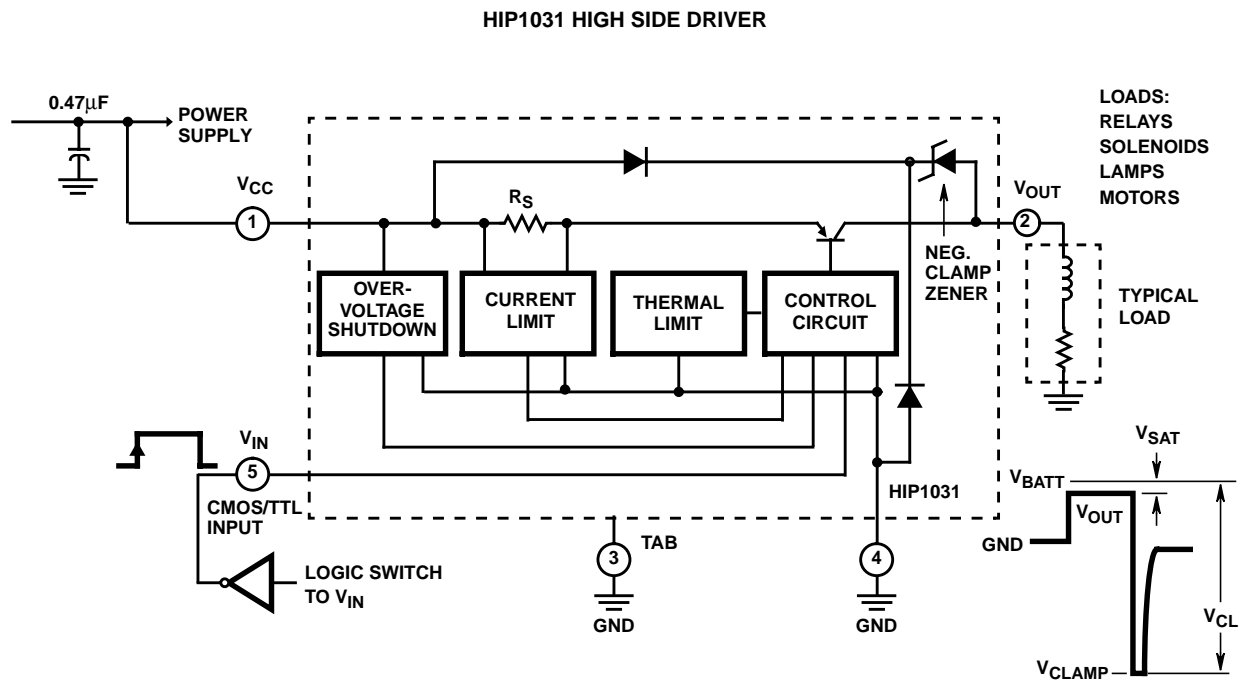
PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Operating Voltage Range	V_{CC}		4.5	-	25	V
Over-Voltage Shutdown	V_{OVSD}	$R_L = 1\text{k}\Omega$, $V_{IN} = 2\text{V}$	26	33	38	V
Over-Temperature Limiting	T_{SD}		-	150	-	°C
Negative Pulse Output Clamp Voltage	V_{CL}	$I_{CL} = -100\text{mA}$, $V_{CC} = 4.5\text{V}$ to 25V , $V_{IN} = 0.8\text{V}$	$(V_{CC} - 62)$	$(V_{CC} - 37)$	$(V_{CC} - 28)$	V
Short Circuit Current Limiting	I_{SC}	(Note 4)	0.7	1.1	1.7	A
Input Control ON	V_{IH}		2.0	-	-	V
Input Control OFF	V_{IL}		-	-	0.8	V
Input Current High	I_{IH}	$V_{IN} = 5.5\text{V}$, $V_{CC} = 6\text{V}$ to 24V	10	-	40	μA
Input Current Low	I_{IL}	$V_{IN} = 0.8\text{V}$, $V_{CC} = 6\text{V}$ to 24V	10	-	30	μA
Supply Current, Full Load, Input Control ON	I_{CCMAX}	$V_{IN} = 2\text{V}$; $I_{OUT} = 0.55\text{A}$	-	-	0.6	A
Supply Current, No Load, Input Control OFF	I_{CCMIN}	$V_{IN} = 0\text{V}$; $I_{OUT} = 0\text{A}$	-	55	150	μA
Input-Output Forward Voltage Drop ($V_{CC} - V_{OUT}$)	V_{SAT}	$I_{OUT} = 0.6\text{A}$, $V_{CC} = 4.5\text{V}$ to 25V	-	-	1.0	V
Output Leakage	I_{OUT_LK}	$V_{IN} = 0.8\text{V}$, $V_{CC} = 6\text{V}$ to 24V	-	-	50	μA
Turn-On Time	t_{ON}	$R_L = 80\Omega$, $T_A = 125^\circ\text{C}$	-	6	20	μs
Turn-OFF Time	t_{OFF}	$R_L = 80\Omega$, $T_A = 125^\circ\text{C}$	-	17	65	μs

NOTE:

- Short Circuit current will be reduced when Thermal Shutdown occurs. Testing of a short circuit current may require a short duration pulse.

HIP1031

Typical Application



Typical Performance Curves

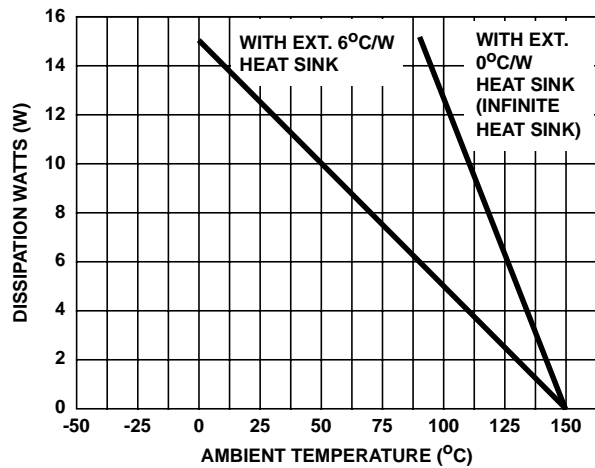


FIGURE 1. DISSIPATION DERATING CURVES

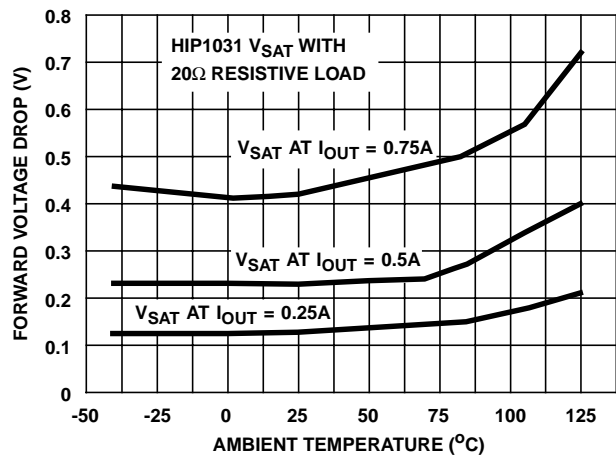
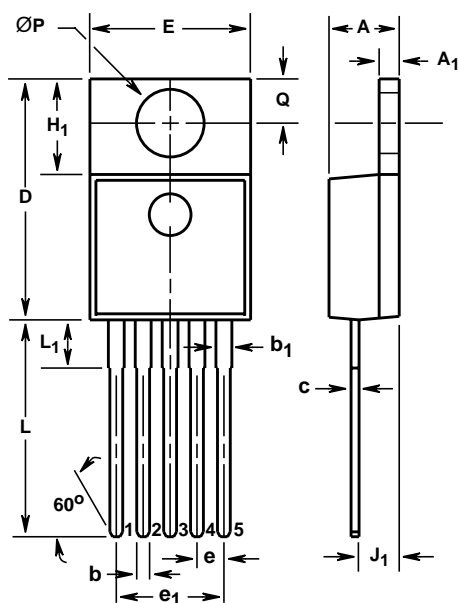


FIGURE 2. TYPICAL V_{SAT} CHARACTERISTIC vs TEMPERATURE

HIP1031

Single-In-Line Plastic Packages (SIP)



Z5.067C (ALTERNATE VERSION) 5 LEAD PLASTIC SINGLE-IN-LINE PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.170	0.180	4.32	4.57	-
A ₁	0.048	0.052	1.22	1.32	3, 4
b	0.030	0.034	0.77	0.86	3, 4
b ₁	0.031	0.041	0.79	1.04	3, 4
c	0.018	0.022	0.46	0.55	3, 4
D	0.590	0.610	14.99	15.49	-
E	0.395	0.405	10.04	10.28	-
e	0.067 TYP		1.70 TYP		5
e ₁	0.268 BSC		6.80 BSC		5
H ₁	0.235	0.255	5.97	6.47	-
J ₁	0.095	0.105	2.42	2.66	6
L	0.530	0.550	13.47	13.97	-
L ₁	0.110	0.130	2.80	3.30	2
ØP	0.149	0.153	3.79	3.88	-
Q	0.105	0.115	2.66	2.92	-

Rev. 1 4/96

NOTES:

1. These dimensions are within allowable dimensions of Rev. A of JEDEC TS-001AA outline dated 8-89.
2. Solder finish uncontrolled in this area.
3. Lead dimension (without solder).
4. Add typically 0.002 inches (0.05mm) for solder plating.
5. Position of lead to be measured 0.250 inches (6.35mm) from bottom of dimension D.
6. Position of lead to be measured 0.100 inches (2.54mm) from bottom of dimension D.
7. Controlling dimension: Inch.

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