intersil

HIP5061

7A, High Efficiency Current Mode Controlled PWM Regulator

April 1994

Features

- Single Chip Current Mode Control IC
- 60V, On-Chip DMOS Power Transistor
- Thermal Protection
- Over-Current Protection
- 250kHz Operation
- Output Rise and Fall Times - 10ns
- On-Chip Reference Voltage - 5.1V
- Slope Compensation
- V_{DD} Clamp Allows 10.8V to 60V Supply
- Supply Current Does Not Increase When Power Device is On

Applications

- Distributed / Board Mounted Power Supplies
- DC - DC Converter Modules
- Voltage Inverters
- Small Uninterruptable Power Supplies
- Cascode Switching for Off Line SMPS

Description

The HIP5061 is a complete power control IC, incorporating both the high power DMOS transistor, CMOS logic and low level analog circuitry on the same Intelligent Power IC. The standard “Boost”, “Buck-Boost”, “Cuk”, “Forward”, “Flyback” and the “SEPIC” (Single-Ended Primary Inductance Converter) power supply topologies may be implemented with this single control IC.

Over-temperature and rapid short-circuit recovery circuitry is incorporated within the IC. These protection circuits disable the drive to the power transistor to protect the transistor and insure rapid restarting of the supply after the short circuit is removed.

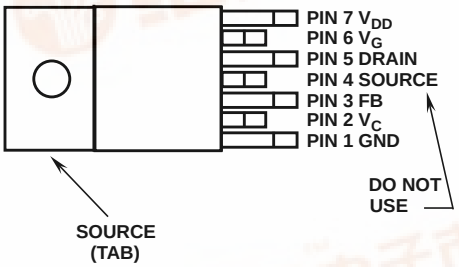
As a result of the power DMOS transistors current (7A at 30% duty cycle, 5A DC) and 60V capability, supplies with output power over 50W are possible.

Ordering Information

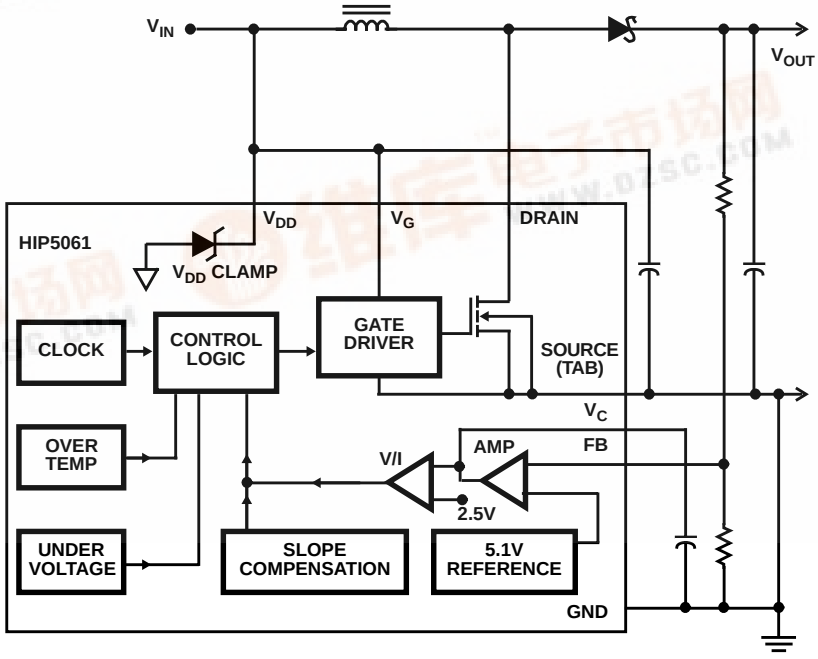
PART NUMBER	TEMPERATURE RANGE	PACKAGE
HIP5061DS	0^oC to $+85^oC$	7 Lead Staggered “Gullwing” SIP

Pinout

HIP5061 (SIP)
TOP VIEW



Simplified Functional Diagram



Absolute Maximum Ratings (Note 1)

DC Supply Voltage, V_{DD} . . . . . -0.3V to 16V
DC Supply Current, I_{DD} 105mA
DMOS Drain Voltage . . . . . -0.3V to 60V
Average DMOS Drain Current 5A
DMOS Source Voltage, V_{SOURCE}, TAB . . . . . -0.1V to 0.1V
DC Supply Voltage, V_G . . . . . -0.3V to V_{DD} + 0.3V
Compensation Pin Current, I_{VC} . . . . . -5mA to 35mA
Voltage at All Other Pins . . . . . -0.3V to V_{DD} + 0.3V
Operating Junction Temperature Range . . . . . 0^oC to $+105^oC$
Storage Temperature Range . . . . . -55^oC to $+150^oC$
ESD Classification . . . . . Class 2 - 2KV
Single Pulse Avalanche Energy Rating, µs (Note 2) . . . EAS 100mJ

Thermal Information

Thermal Resistance θ_{JC}
Plastic SIP Package . . . . . $2^oC/W$
Maximum Package Power Dissipation at $+85^oC$
(Depends Upon Mounting, Heat Sink and Application) 10W
Max. Junction Temperature . . . . . $+105^oC$
(Controlled By Thermal Shutdown Circuit)
Lead Temperature (Soldering 10s) . . . . . $+265^oC$

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Electrical Specifications

$V_{DD} = V_G$ =12V, V_C = 5V, V_{FB} = 5.1V, SOURCE = GND = DRAIN = 0V, $T_J = 0^oC$ to $+105^oC$, Unless Otherwise Specified

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
DEVICE PARAMETERS						
I_{DD}	Quiescent Supply Current	$V_{DD} = V_G$ = 13.2V, V_C = 0V, V_{FB} = 4V	6	12	18	mA
I_{DD}	Operating Supply Current	$V_{DD} = V_G$ = 13.2V, V_C = 8.5V, V_{FB} = 4V	-	24	31	mA
IV_G	Quiescent Current to Gate Driver	$V_{DD} = V_G$ = 13.2V, V_C = 0V	-	0	10	µA
IV_G	Operating Current to Gate Driver	V_C = 3V	-	1	2	mA
V_{DDC}	Clamp Voltage	I_{DD} = 100mA	13.3	14	15	V
V_{REF}	Reference Voltage	I_{VC} = 0µA, $V_C = V_{FB}$	5.0	5.1	5.2	V
AMPLIFIERS						
$\|I_{FB}\|$	Input Current	$V_{FB} = V_{REF}$	-	-0.85	0.5	µA
$g_m (V_{FB})$	V_{FB} Transconductance $I_{VC}/(V_{FB} - V_{REF})$	$/I_{VC}/$ = 500µA, Note 3	20	30	43	mS
IV_{CMAX}	Maximum Source Current	V_{FB} = 4.6V	-4	-1.8	-1	mA
IV_{CMAX}	Maximum Sink Current	V_{FB} = 5.6V	1	1.8	4	mA
A_{OL}	Voltage Gain	$/I_{VC}/$ = 500µA, Note 3	44	50	-	dB
V_{CMAX}	Short Circuit Recovery Comparator Rising Threshold Voltage		5.4	6.6	8.9	V
V_{CHYS}	Short Circuit Recovery Comparator Hysteresis Voltage		0.7	1.1	1.8	V
IVC_{OVER}	V_C Over-Voltage Current	$V_{DD} = V_G$ = 10.8V, $V_C = V_{CMAX}$	0	10	25	mA
CLOCK						
fq	Internal Clock Frequency		210	250	290	kHz
DMOS TRANSISTOR						
$r_{DS(ON)}$	Drain-Source On-State Resistance	I_{DRAIN} = 5A, $V_{DD} = V_G$ = 10.8V $T_J = +25^oC$	-	0.15	0.22	Ω
$r_{DS(ON)}$	Drain-Source On-State Resistance	I_{DRAIN} = 5A, $V_{DD} = V_G$ = 10.8V $T_J = +105^oC$	-	-	0.33	Ω
I_{DSS}	Drain-Source Leakage Current	V_{DRAIN} = 60V	-	0.5	10	µA
I_{DSH}	Average Drain Short Circuit Current	V_{DRAIN} = 5V, Note 4	-	-	5	A
C_{DRAIN}	DRAIN Capacitance	Note 4	-	200	-	pF

Electrical Specifications $V_{DD} = V_G = 12V$, $V_C = 5V$, $V_{FB} = 5.1V$, SOURCE = GND = DRAIN = 0V, $T_J = 0^oC$ to $+105^oC$, Unless Otherwise Specified **(Continued)**

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
CURRENT CONTROLLED PWM						
$g_m(V_C)$	$\Delta I_{DRAIN, PEAK} / \Delta V_C$	Note 3	1.4	2.2	3.0	A/V
V/I_{REF}	Voltage to Current Converter Reference Voltage	I_{DRAIN} = 0.25A, Note 3	2.4	2.8	3.1	V
t_{BT}	Current Comparator Blanking Time	Note 3	40	100	175	ns
t_{ONMIN}	Minimum DMOS “ON” Time	Note 3	60	150	250	ns
t_{OFFMIN}	Minimum DMOS “OFF” Time	Note 3	40	125	200	ns
MinCI	Minimum Controllable DMOS Peak Current	Note 3	-	100	250	mA
MaxCI	Maximum Controllable DMOS Peak Current	Duty Cycle = 6% to 30%, Note 3	7	9.5	12	A
MaxCI	Maximum Controllable DMOS Peak Current	Duty Cycle = 30% to 96%, Note 3	5	8	12	A
CURRENT COMPENSATION RAMP						
$\Delta I/\Delta t$	Compensation Ramp Rate	$\Delta I_{DRAIN, PEAK} / \Delta$Time, Note 3	-1.4	-0.85	-0.45	A/µs
t_{RD}	Compensation Ramp Delay	Note 3	1.3	1.5	1.8	µs
START-UP						
V_{DDMIN}	Rising V_{DD} Threshold Voltage	V_{FB} = 4V	9.3	10.3	10.8	V
V_{DDHYS}	Power-On Hysteresis	V_{FB} = 4V	0.3	0.45	0.6	V
V_{CEN}	Enable Comparator Threshold Voltage		1.0	1.5	2.0	V
R_{VC}	Power-Up Resistance	$4V < V_{DD} < 10.8V$, $V_C = 0.8V$	50	500	3000	Ω
THERMAL MONITOR						
T_J	Substrate Temperature for Thermal Monitor to Trip	Note 4	105	-	145	^oC
T_{JHY}	Temperature Hysteresis	Note 4	-	5	-	^oC

NOTES:

1. All Voltages relative to pin 1, GND.
2. $V_D = 10V$, Starting $T_J = +25^oC$, L = 4mH, $I_{PEAK} = 7A$.
3. Test is performed at wafer level only.
4. Determined by design, not a measured parameter.

TABLE 1. CONDITIONS FOR UNCLAMPED ENERGY CIRCUIT

V_D (V)	I_L (PEAK AMPS)	L (mH)	EAS (mJ)
10	5	40	550
10	7	4TZ	120
6	10	0.33	18
6	12.5	0.14	12

NOTE: Device Selected to Obtain Peak Current without Clocking

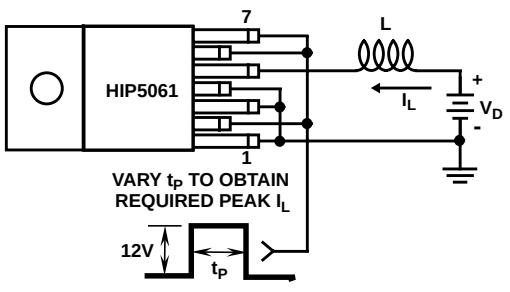


FIGURE 1. UNCLAMPED ENERGY TEST CIRCUIT

Definitions of Electrical Specifications

Refer to the Functional Block Diagram of Figure 1 for locations of functional blocks and devices.

Device Parameters

I_{DD}, Quiescent Supply Current - Supply current with the chip disabled. The Clock, Error Amplifier, Voltage-to-Current Converter, and Current Ramp circuits draw only quiescent current. The supply voltage must be kept lower than the turn-on voltage of the V_{DD} clamp or else the supply current increases dramatically.

I_{DD}, Operating Supply Current - Supply current with the chip enabled. The Error Amplifier is drawing its maximum current because V_{FB} is less than its reference voltage. The voltage-to-current amplifier is drawing its maximum because V_C is at its maximum. The ramp circuit is drawing its maximum because it is not being disabled by the DMOS transistor turning off.

IV_G, Quiescent Gate Driver Current - Gate Drivers supply current with the IC disabled. The Gate Driver is not toggling and so it draws only leakage current.

IV_G, Operating Gate Driver Current - Gate Drivers supply current with the IC enabled. The DMOS transistor drain is loaded with a large resistor tied to 60V so that it is swinging from 0V to 60V during each cycle.

V_{DDC}, V_{DD} Clamp - V_{DD} voltage at the maximum allowed current through the V_{DD} Clamp.

V_{REF}, Reference Voltage - The voltage on FB that sets the current on V_C to zero. This is the reference voltage for the DC/DC converter.

Amplifiers

$|I_{FB}|$, Input Current - Current through FB pin when it is at its normal operating voltage. This current must be considered when connecting the output of a DC/DC convertor to the FB pin via a resistor divider.

$g_m(V_{FB})$, Transconductance - The change in current through the V_C pin divided by the change in voltage on FB. The g_m times the resistance between V_C and ground gives the voltage gain of the Error Amplifier.

IV_{CMAX}, Maximum Source Current - The current on V_C when FB is more than a few hundred millivolts less than V_{REF}.

IV_{CMAX}, Maximum Sink Current - The current on V_C when FB is more than a few hundred millivolts more than V_{REF}.

A_{OL}, Voltage Gain - Change in the voltage on V_C divided by the change in voltage on FB. There is no resistive load on V_C. This is the voltage gain of the error amplifier when g_m times load resistance is larger than this gain.

V_{CMAX}, V_C Rising Threshold - The voltage on V_C that causes the Voltage-to-Current Amplifier to reach full-scale. When V_C reaches this voltage, the V_C NMOS transistor (transistor with its drain connected to the V_C pin in the Functional Block Diagram of Figure 2) turns on and tries to lower the voltage on V_C.

V_{CHYS}, V_{CMAX} Hysteresis - The voltage on V_C that causes the NMOS transistor to turnoff if it had been turned on by V_C exceeding V_{CMAX}. At this voltage the current out of the Voltage-to-Current Converter is at roughly three quarters of full-scale.

IVC_{OVER}, V_C Over-Voltage Current - The current drawn through the V_C pin after the NMOS transistor is turned on due to excessive voltage on V_C. The NMOS transistor connected to the V_C pin draws more than enough current to overcome the full scale source current of the Error Amplifier.

Clock

fq, Frequency - The frequency of the DC/DC converter. The Clock actually runs faster than this value so that various control signals can be internally generated.

DMOS Transistor

$r_{DS(ON)}$, "On" Resistance - Resistance from DMOS transistor Drain to Source at maximum drain current and minimum Gate Driver voltage, V_G.

I_{DSS}, Leakage Current - Current through DMOS transistor at the Maximum Rated Voltage.

Current Controlled PWM

$g_m(V_C)$, Transconductance - The change in the DMOS transistor peak drain current divided by the change in voltage on V_C. When analyzing DC/DC converters the DMOS transistor and the inductor tied to the drain are sometimes modelled as a voltage-controlled current source and this parameter is the gain of the voltage-controlled current source.

V/I_{REF}, Current Control Threshold - The voltage on V_C that causes the DMOS transistor to shut off at the minimum controllable current. This voltage is greater than the Enable Comparator Threshold (V_{CEN}) so that as V_C rises the IC does not jump from the disabled state to the DMOS transistor conducting a large current.

t_{BT}, Blanking Time - At the beginning of each cycle there is a blanking time that the DMOS transistor turns-on and stays-on no matter how high drain the current. This blanking time permits ringing in the external parasitic capacitances and inductances to dampen and for the charging of the reverse bias on the rectifier diode.

t_{ONMIN}, Minimum DMOS Transistor "On" Time - The minimum on-time for the DMOS transistor where small changes in the V_C voltage make predictable changes in the DMOS transistor peak current. Converters should be designed to avoid requiring pulse widths less than the minimum on time.

t_{OFFMIN}, Minimum DMOS Transistor "Off" Time - The minimum off-time for the DMOS transistor that allows enough time for the IC to get ready for the next cycle. Converters should be designed to avoid requiring pulse widths so large that the minimum off time is violated. (However, zero off time is allowed, that is, the DMOS transistor can stay on from one cycle to the next.)

MinCI, Minimum Controllable Current - When the voltage on V_C is below V/I_{REF}, the peak current for the DMOS transistor is too small for the Current Comparator to operate reliably. Converters should be designed to avoid operating the DMOS transistor at this low current.

MaxCl, Maximum Controllable Current - The peak current for the DMOS transistor when the Voltage-to-Current Converter is at its full scale output. The DMOS transistor current may exceed this value during the blanking time so proper precautions should be taken. This parameter is unchanged for the first 3/8 of the cycle and then decreases linearly with time because of the Current Ramp becoming active.

Current Compensation Ramp

$\Delta I/\Delta t$, Compensation Ramp Rate - At a given voltage on V_C the DMOS transistor will turn off at some current that stays constant for about the first 1.5µs of the cycle. After 1.5µs, the turnoff current starts to linearly decrease. This parameter specifies the change in the DMOS transistor turnoff current.

t_{RD}, Compensation Ramp Delay - The time into each cycle that the compensation ramp turns on. The Current Compensation Ramp, used for Slope Compensation, is developed by the Current Ramp block shown in the FUNCTIONAL BLOCK DIAGRAM of Figure 2.

Start-Up

V_{DDMIN}, Rising V_{DD} Threshold Voltage - The minimum voltage on V_{DD} needed to enable the IC.

V_{DDHYS}, Power - On Hysteresis Voltage - The difference between the voltage on V_{DD} that enables the IC and the voltage that disables the IC.

V_{CEN}, Enable Comparator Threshold Voltage - The minimum voltage on V_C needed to enable the IC. The IC can be shutdown from an open-collector logic gate by pulling down the V_C pin to GND.

R_{VC}, Power - Up Resistance - When V_{DD} is below V_{DDMIN}, the NMOS transistor connected to the V_C pin is turned on to make sure the V_C node is low. Thus the voltage on V_C can gradually build up as will the trip current on the DMOS transistor. This is the only form of “soft start” included on the IC. The resistance is measured between the V_C and GND pins.

Thermal Monitor

T_J, Rising Temperature Threshold - The IC temperature that causes the IC to disable itself so as to prevent damage. Proper heat-sinking is required to avoid over-temperature conditions, especially during start-up when the DMOS transistor may stay on for a long time if an external soft-start circuit is not added.

T_{JHY}, Temperature Hysteresis - The IC must cool down this much after it is disabled by being too hot before it can resume normal operation.

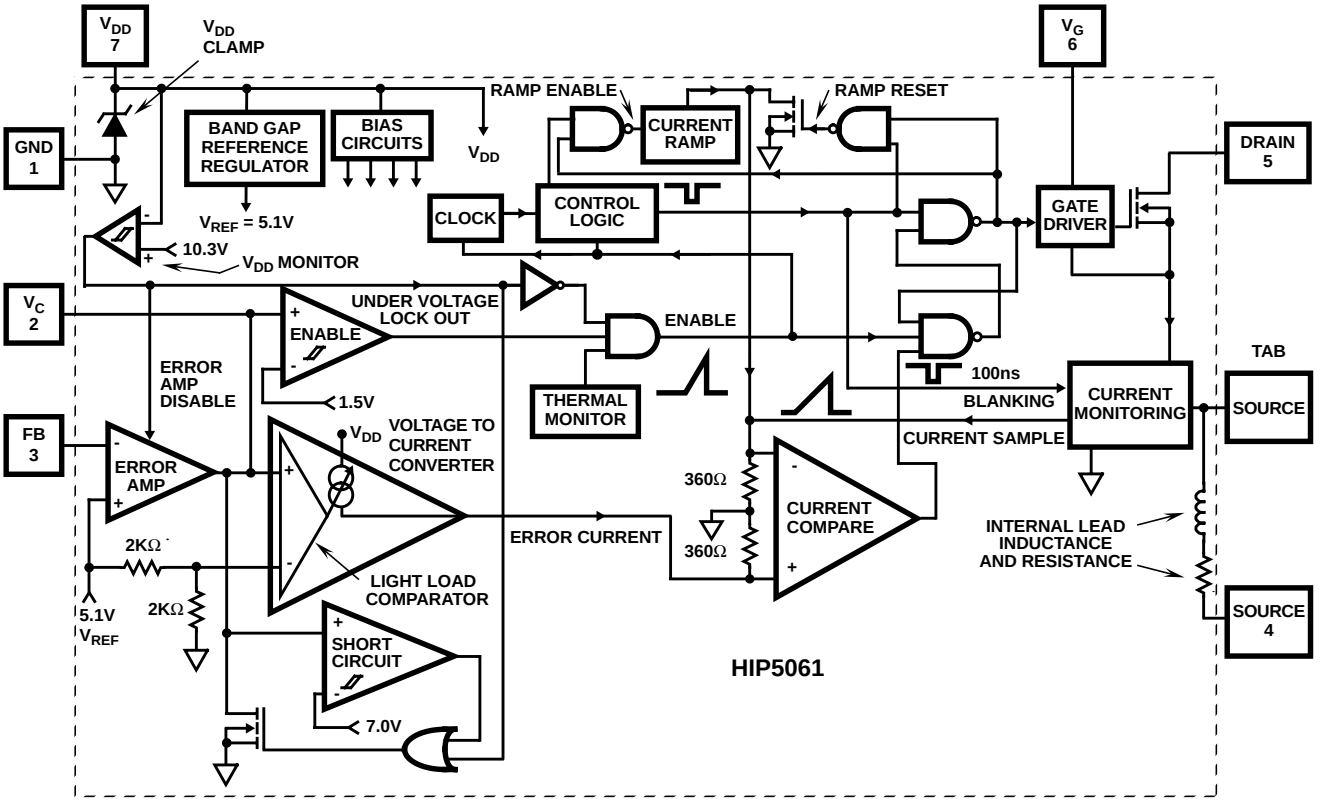


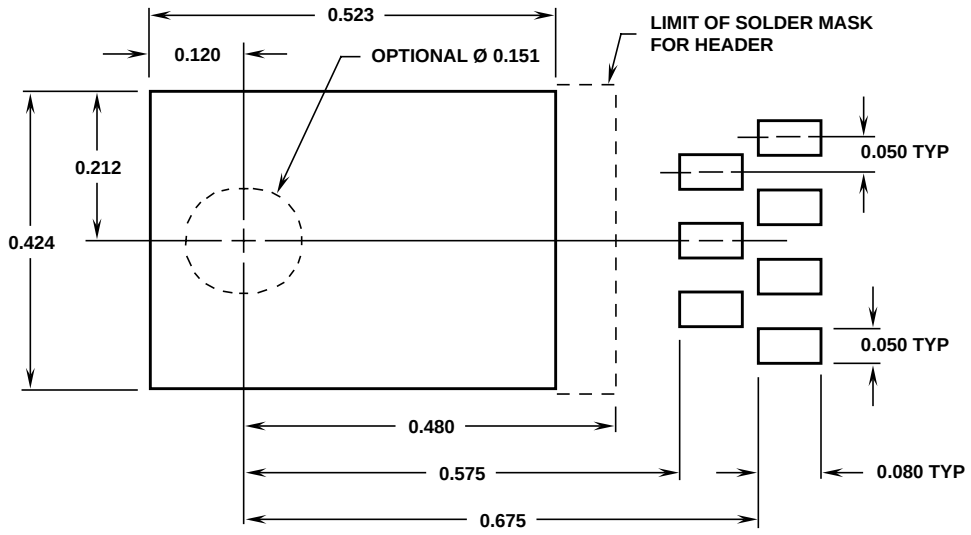
FIGURE 2. FUNCTIONAL BLOCK DIAGRAM OF THE HIP5061

Pin Description

TERMINAL NUMBER	DESIGNATION	DESCRIPTION
1	GND	This is the analog ground terminal of the IC.
2	V_C	The output of the transconductance amplifier appears at this terminal. Input to the internal voltage to current converter also appears at this node. Transconductance amplifier gain and loop response are set at this terminal. When the V_{DD} terminal voltage is below the starting voltage, V_{DDMIN}, this terminal is held low. When the voltage at this terminal exceeds V_{CMAX}, 7V typical, implying an over-current condition, a typical 10mA current, I_{VCOVER} pulls this terminal towards ground. This current remains "ON" until the voltage on the V_C terminal falls by V_{CHYS}, typically 1.1V, below the upper threshold, V_{CMAX}. When the voltage on this terminal falls below V_{CEN}, typically 1.5V, the IC is disabled.
3	FB	Feedback from the regulator output is applied to this terminal. This terminal is the input to the transconductance amplifier. The amplifier compares the internal 5.1V reference and the feedback signal from the regulator output.
4	SOURCE	The terminal, labeled TAB, has a connection to this terminal, but because of the long lead length and resulting high inductance of this terminal, it should not be used as a means of bypassing. Therefore, this terminal is labeled "Do Not Use."
5	DRAIN	Connection to the Drain of the internal power DMOS transistor is made at this terminal.
6	V_G	Gate drive supply voltage is provided at this terminal. A 10Ω to 150Ω resistor connected between this terminal and the V_{DD} terminal provides decoupling and the supply voltage for the gate drivers.
7	V_{DD}	External supply input to the IC. A nominal 14V shunt regulator is connected between this terminal and the TAB. A series resistor should be connected to this terminal from the external voltage source to supply a minimum current of 33mA and a maximum current of 105mA under the worst cast supply voltage. The series resistor is not required if the supply voltage is 12V, ±10%.
TAB	SOURCE	This is the internal power DMOS transistor Source terminal. It should be used as the ground return for the V_{DD} bypass capacitor. In addition high frequency bypassing for both the regulator output load voltage and supply input voltage should be returned to this terminal.

For more information refer to Application Notes AN9208, AN9212, AN9323.

Foot Print For Soldering



TO-220 STAGGERED GULL WING SIP

Typical Performance Curves

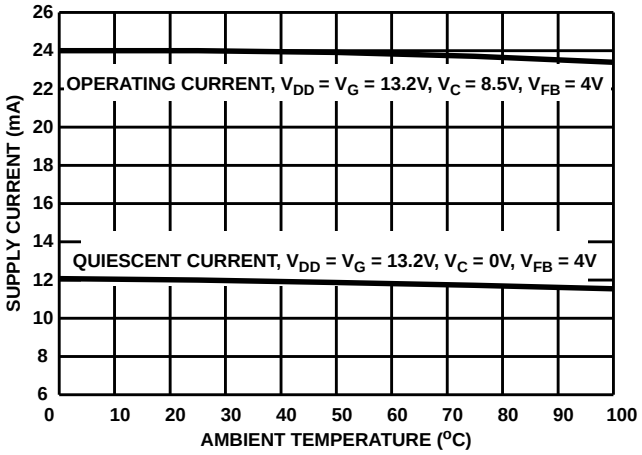


FIGURE 3. TYPICAL SUPPLY CURRENT vs TEMPERATURE

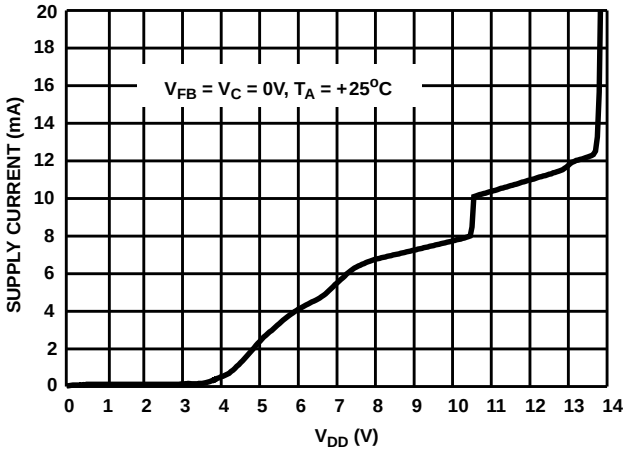


FIGURE 4. TYPICAL SUPPLY CURRENT vs SUPPLY VOLTAGE

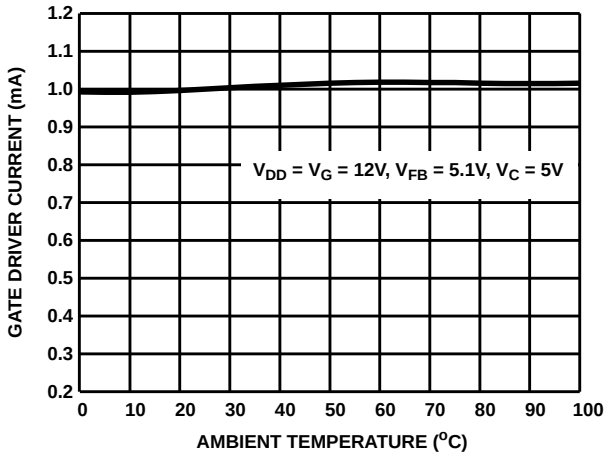


FIGURE 5. TYPICAL GATE DRIVER OPERATING CURRENT vs TEMPERATURE

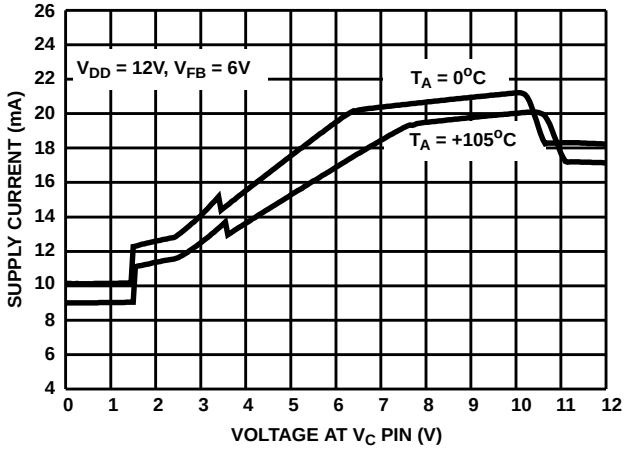


FIGURE 6. TYPICAL SUPPLY CURRENT vs VOLTAGE AT PIN V_C FOR 0^oC AND $+105^oC$

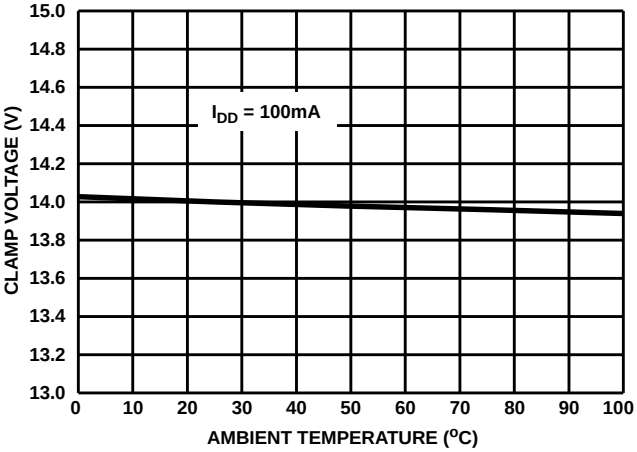


FIGURE 7. TYPICAL CLAMP VOLTAGE vs TEMPERATURE

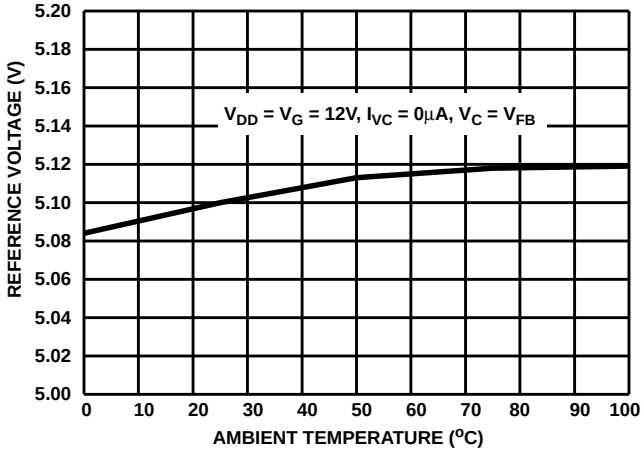


FIGURE 8. TYPICAL REFERENCE VOLTAGE vs TEMPERATURE

Typical Performance Curves (Continued)

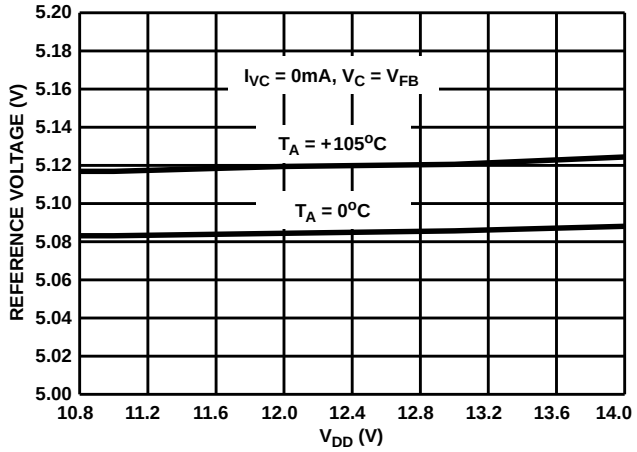


FIGURE 9. TYPICAL REFERENCE VOLTAGE vs SUPPLY VOLTAGE FOR 0°C AND +105°C

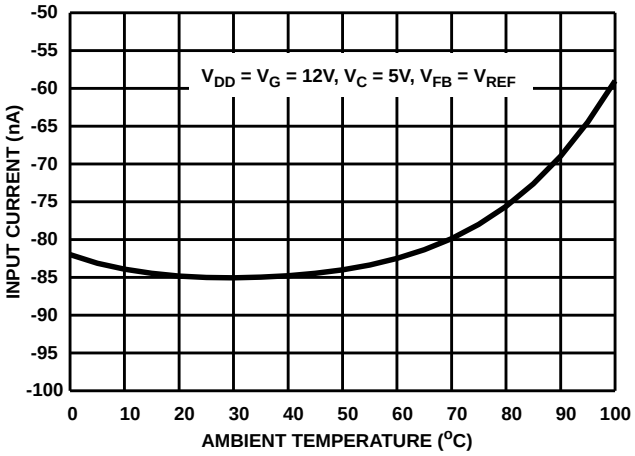


FIGURE 10. TYPICAL INPUT CURRENT TO FB PIN vs TEMPERATURE

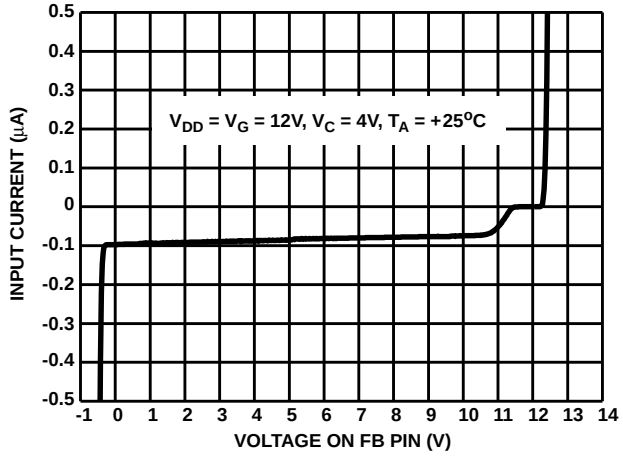


FIGURE 11. TYPICAL INPUT CURRENT TO FB PIN vs V_{FB}

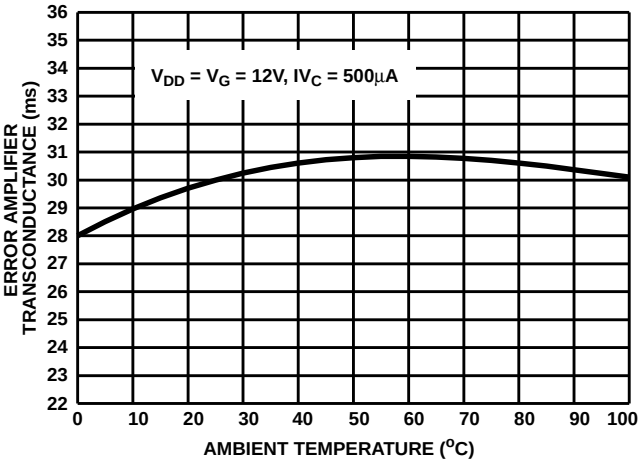


FIGURE 12. TYPICAL ERROR AMPLIFIER TRANSCONDUCTANCE vs TEMPERATURE

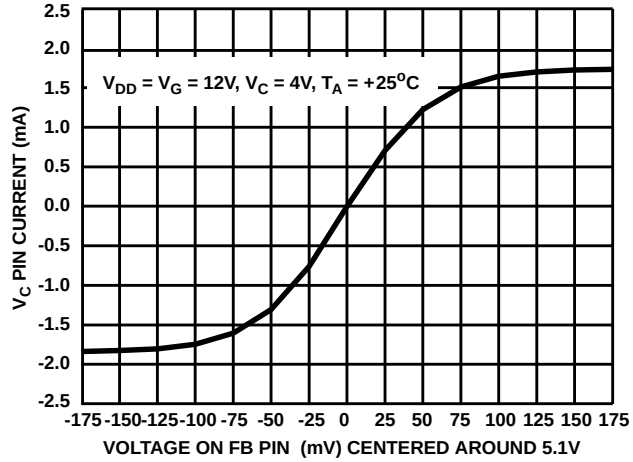


FIGURE 13. TYPICAL V_C PIN CURRENT IV_C PIN vs VOLTAGE ON FB PIN (SHOWS ERROR AMPLIFIER TRANSCONDUCTANCE)

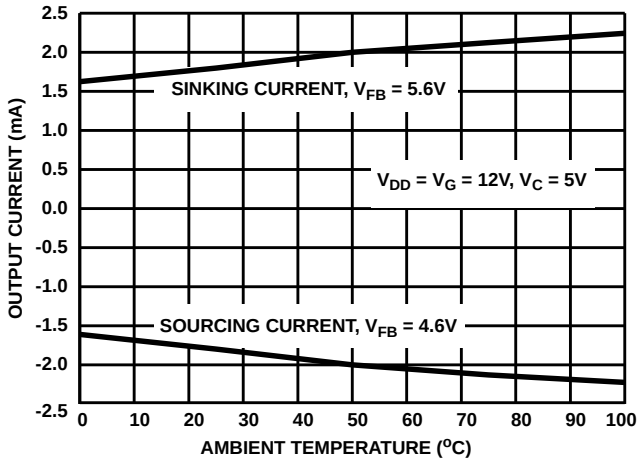


FIGURE 14. TYPICAL ERROR AMPLIFIER SINKING AND SOURCING CURRENT vs TEMPERATURE

Typical Performance Curves (Continued)

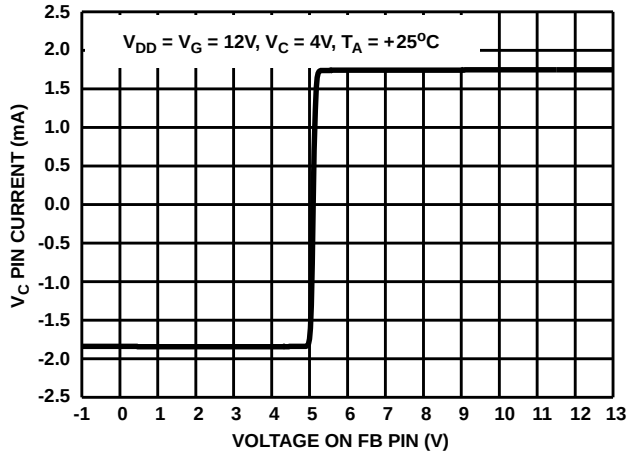


FIGURE 15. TYPICAL V_C PIN CURRENT vs VOLTAGE ON FB PIN

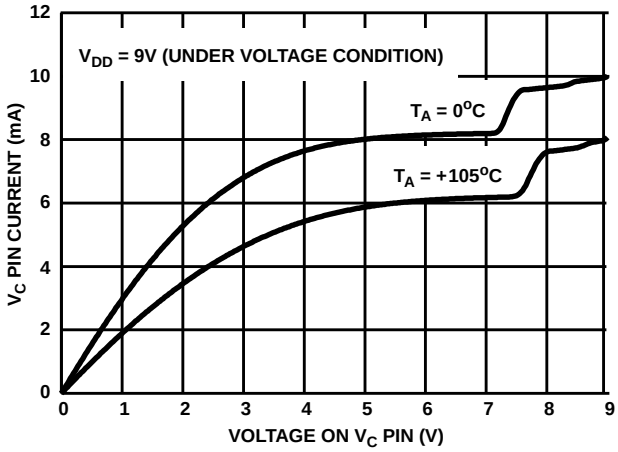


FIGURE 16. TYPICAL V_C PIN CURRENT vs VOLTAGE ON V_C PIN FOR 0^oC AND $+105^oC$

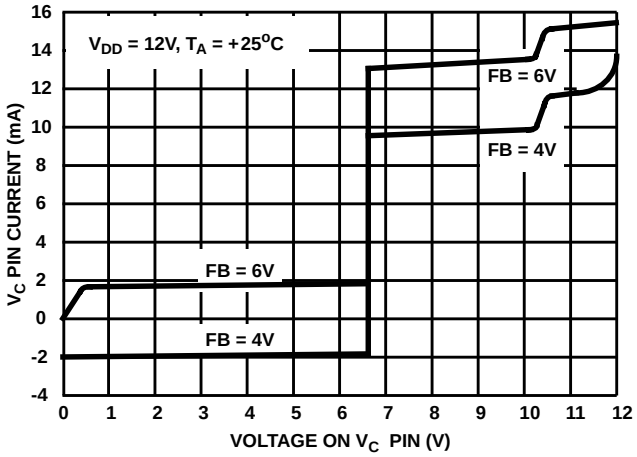


FIGURE 17. TYPICAL V_C PIN CURRENT vs VOLTAGE ON V_C PIN FOR VOLTAGES ABOVE AND BELOW V_{REF}

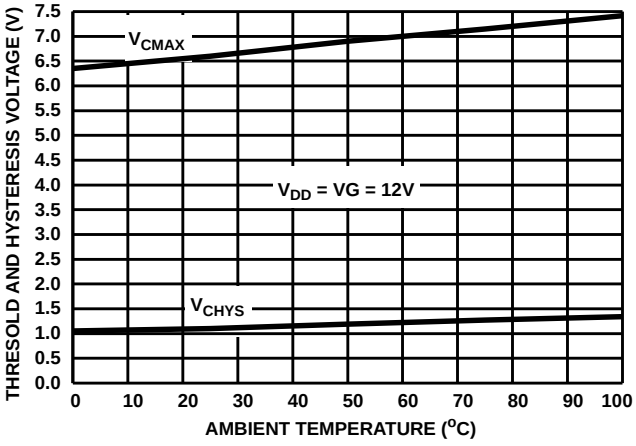


FIGURE 18. TYPICAL SHORT CIRCUIT COMPARATOR THRESHOLD VOLTAGE vs TEMPERATURE

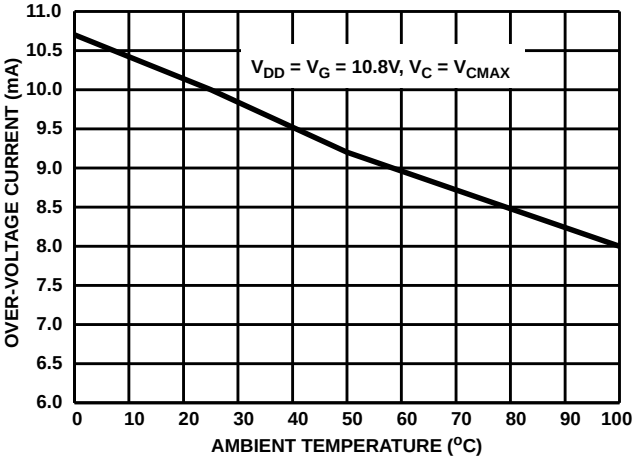


FIGURE 19. TYPICAL OVER-VOLTAGE CURRENT vs TEMPERATURE

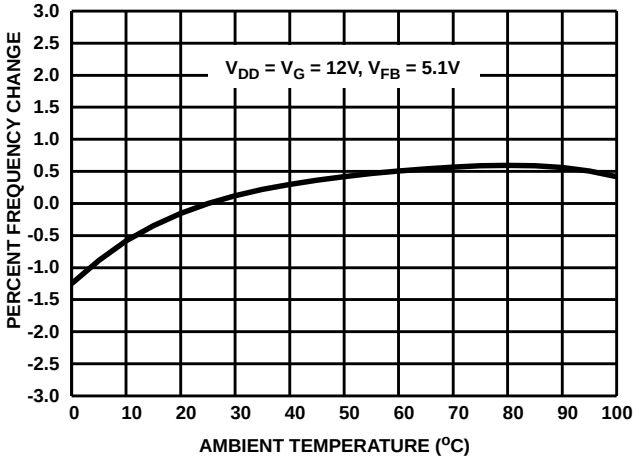


FIGURE 20. TYPICAL CLOCK FREQUENCY PERCENT CHANGE vs TEMPERATURE

Typical Performance Curves (Continued)

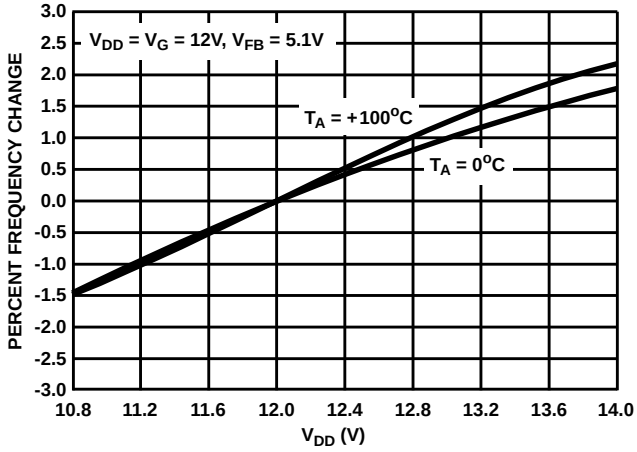


FIGURE 21. TYPICAL CLOCK FREQUENCY PERCENT CHANGE vs SUPPLY VOLTAGE V_{DD} AT 0^oC AND $+100^oC$

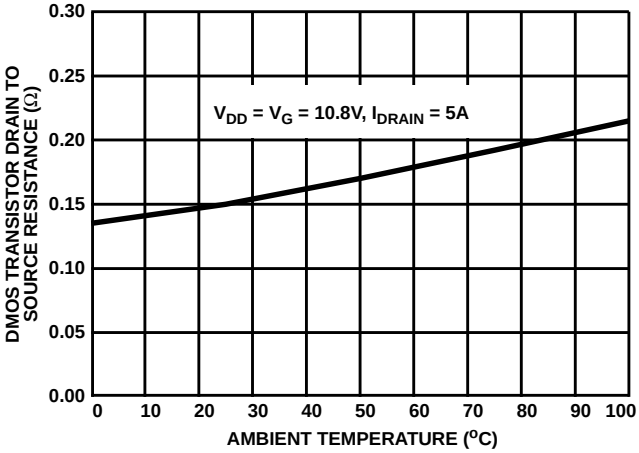


FIGURE 22. TYPICAL DMOS TRANSISTOR DRAIN TO SOURCE RESISTANCE vs TEMPERATURE

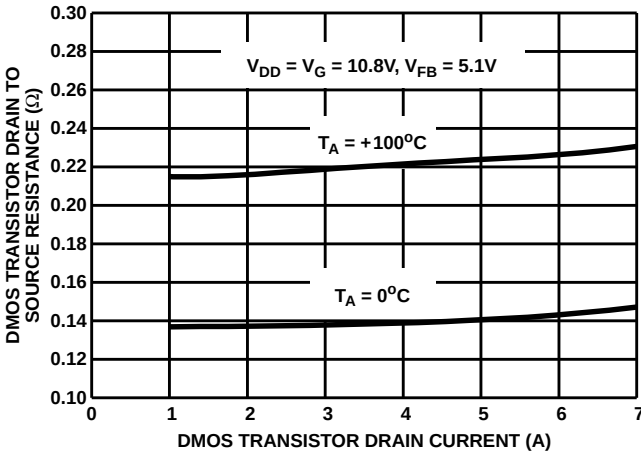


FIGURE 23. TYPICAL DMOS TRANSISTOR DRAIN TO SOURCE RESISTANCE vs DRAIN CURRENT I_{DRAIN} AT 0^oC AND $+100^oC$

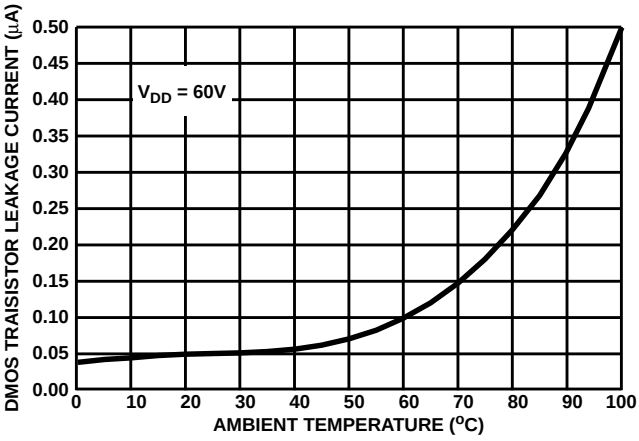


FIGURE 24. TYPICAL DMOS TRANSISTOR DRAIN TO SOURCE LEAKAGE CURRENT vs TEMPERATURE

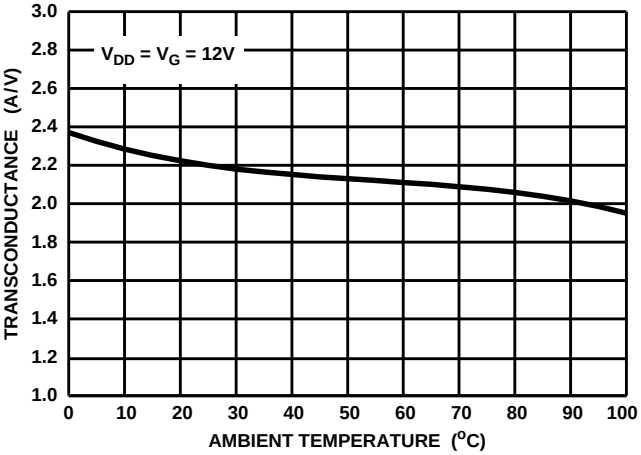


FIGURE 25. TYPICAL TRANSCONDUCTANCE FROM V_C PIN TO DMOS TRANSISTOR DRAIN (PEAK CURRENT) vs TEMPERATURE

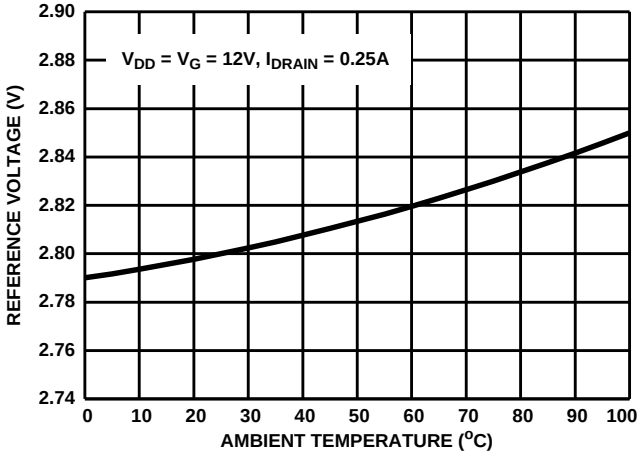


FIGURE 26. TYPICAL VOLTAGE TO CURRENT CONVERTER REFERENCE VOLTAGE vs TEMPERATURE

Typical Performance Curves (Continued)

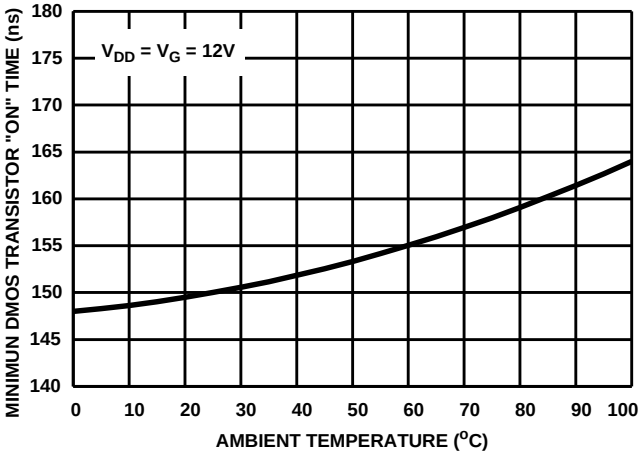


FIGURE 27. TYPICAL MINIMUM DMOS TRANSISTOR "ON" TIME vs TEMPERATURE

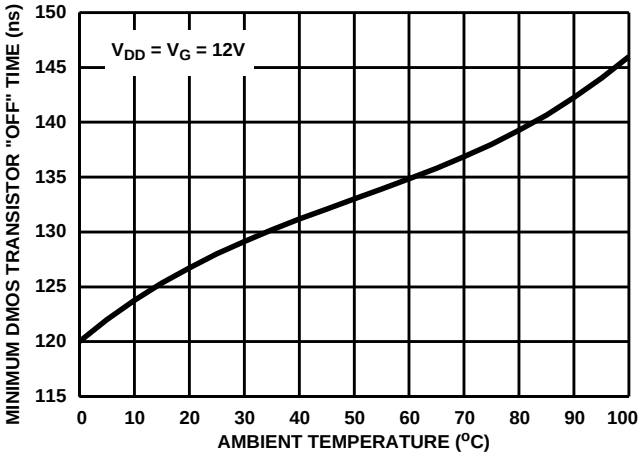


FIGURE 28. TYPICAL MINIMUM DMOS TRANSISTOR "OFF" TIME vs TEMPERATURE

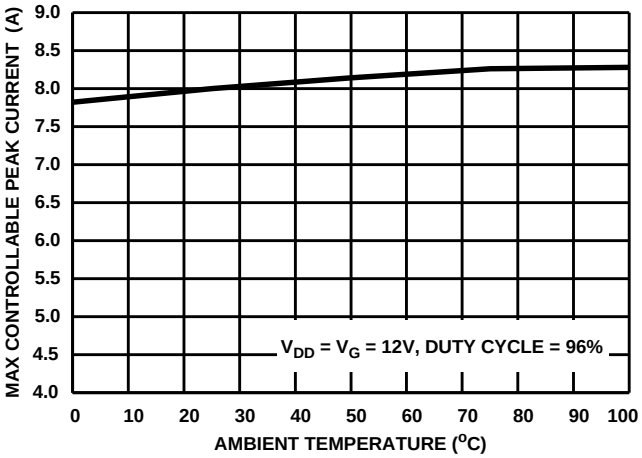


FIGURE 29. TYPICAL MAXIMUM CONTROLLABLE PEAK DMOS DRAIN CURRENT vs TEMPERATURE

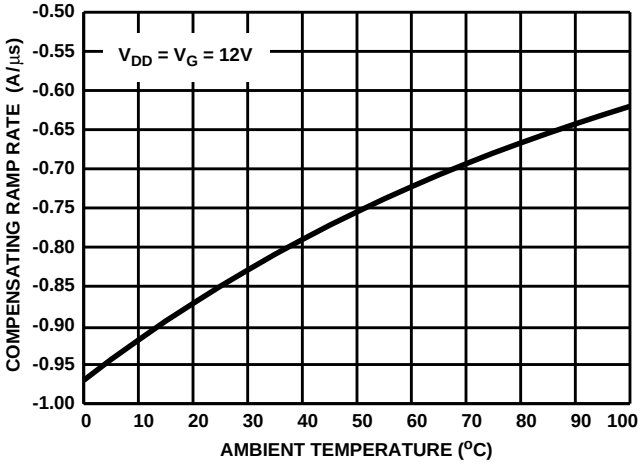


FIGURE 30. TYPICAL COMPENSATING RAMP RATE vs TEMPERATURE

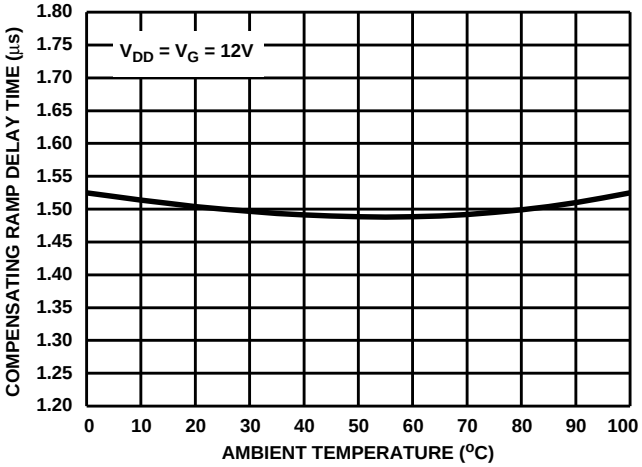


FIGURE 31. TYPICAL COMPENSATION RAMP DELAY TIME vs TEMPERATURE

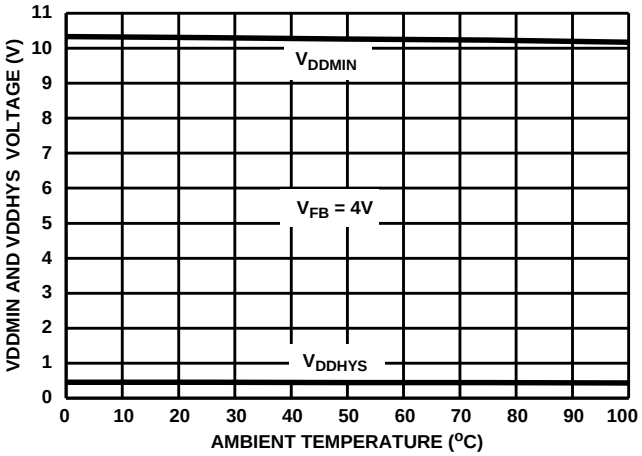


FIGURE 32. TYPICAL RISING V_{DD} COMPARATOR THRESHOLD VOLTAGE vs TEMPERATURE

Typical Application Circuit

Figure 33 shows a Simplified Block Diagram of the HIP5061 in a typical Boost converter. A resistor connected from the V_{IN} supply to the V_{DD} terminal of the IC powers the internal 14V shunt regulator. The Gate Driver supply is decoupled from the main supply by a small external resistor connected between V_{DD} and the V_G terminal. A bypass capacitor is connected between the V_{DD} terminal and ground to reduce coupling between analog and digital circuitry. A Schottky diode insures efficient energy transfer from the DMOS drain circuit inductor to the load. To set the output voltage, two resistors are used to scale the output supply voltage down to the 5.1V internal reference.

The heart of the IC is the high current DMOS power transistor with its associated gate driver and high-speed peak current control loop. A portion of the converters DC output is applied to a transconductance error amplifier that compares the fed back signal with the internal 5.1V reference. The output of this amplifier is brought out at the V_C terminal to provide for soft start and frequency compensation of the control loop. This same signal is also applied internally to program the peak DMOS transistor drain current. To assure precise current control, the response time of this peak current control loop is less than 50ns.

A 2MHz internal clock provides all the timing signals for the converter operating at 250kHz. A slope compensation circuit is also incorporated within the converter IC to eliminate sub-harmonic oscillation that occurs in continuous-current mode converters operating with duty cycles greater than 50%.

HIP5061 Description of Operation

Figure 2 shows a more detailed Functional Block Diagram of the HIP5061. An internal 14V shunt regulator in conjunction with an external series resistor provides internal operating voltage to the IC in applications where no 12V auxiliary supply is available. Note that In applications where the input voltage at V_{DD} is 12V, +/-10%, the regulator is not used. This regulator is shown as a zener diode on the diagrams of Figure 2 and Figure 33.

The 2MHz clock is processed in the Control Logic block to provide various timing signals. A cycle of operation begins when a 100ns pulse (which occurs at a 4µs interval) triggers the latch that initiates the DMOS transistor on-time. This pulse also provides a blanking interval in the Current Monitoring block to eliminate false turn-offs caused by high transient pulse currents that occur during turn-on. The output of

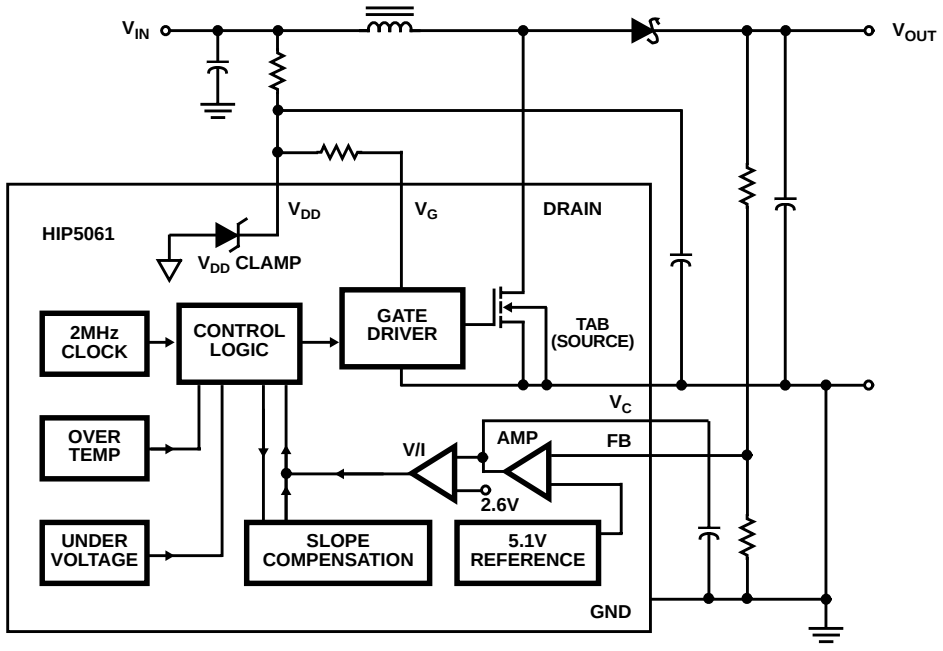


FIGURE 33. SIMPLIFIED BLOCK DIAGRAM OF THE HIP5061 IN A TYPICAL "BOOST" CONFIGURATION

the Current Ramp block is summed with the sensed DMOS transistor current (to provide slope compensation) before being compared with the Error Current signal. The current ramp, -0.45A/µs, is inhibited for the first 1.5µs (37.5%) of the duty cycle by the Ramp Enable signal, since ramp is not needed for slope compensation during this interval. Inhibiting of the compensating ramp has the effect of reducing the peak short-circuit current.

The output of the power supply is divided down and monitored at the FB terminal. A transconductance error amplifier compares the DC level of the fed back voltage with an internal bandgap reference, while providing voltage loop compensation by means of external resistors and capacitors. The Error Amplifier output (the error voltage) is then converted into a current (the Error Current) that is used to program the required peak DMOS transistor current that produces the desired output voltage. When the sum of the sensed DMOS transistor current and the compensating ramp exceed the Error Current signal, the latch is reset and the DMOS transistor is turned off. Current comparison around this loop takes place in less than 50ns, allowing for excellent 250kHz converter operation. The latch can also be reset by an under-voltage (V_{DD} < 10.3V typical), over temperature (T_J > +125^oC typical) or a shutdown signal externally applied at the V_C terminal. See Figure 36.

Note that if the error voltage (at the V_C pin) is less that 2.55V, then the output of the Voltage-to-Current Converter will be held at zero. This condition will produce the minimum possible pulse width, typically 150ns (100ns blanking pulse plus 50ns delay). Error voltages lower than this 2.55V level will not produce shorter pulse widths. Under very light loads (when V_C goes below 1.5V), the Enable Comparator will temporarily hold-off the PWM latch (and the DMOS transistor) until the V_C voltages rises above 1.5V. This low V_C inhibit circuit results in a burst-mode of operation that maintains regulation under light or no loads.

During an over-current condition, the output of the Error Amplifier will attempt to exceed the 7.0V threshold. At this point, the Short-Circuit Comparator will pull down on this signal and induce a low-level oscillation about the threshold, serving to clamp the peak error voltage. This clamping action, in turn, will limit the peak current in the DMOS transistor, reducing the duty ratio of the switch as the demand for current continues to increase. This action, in conjunction with the Thermal Monitor, serves to protect the IC from over-current (short-circuit) conditions.

Using the Transconductance Error Amplifier

A transconductance amplifier with a typical g_m of 30mS is used as the input gain stage where the power supply output voltage is compared with the internally generated 5.1V reference voltage. A PNP transistor input structure allows this amplifier to accommodate large negative going transient voltages without causing amplifier phase reversal, often associated with PNP input structures. Negative transients up to 5V applied to the input though at least 5.1k will not result in phase reversal. The amplifier output stage has the customary drain to drain output to help improve the output impedance, ideally infinity. The amplifier gain is typically 50dB and is not significantly altered when operating into the stages that follow within the IC. To minimize the output stage idling current, while providing high peak currents to insure rapid response to load and input transients, a class B type of output stage was used in the amplifier. Placing a 100k resistor from the amplifier output terminal, V_C, to ground will bias the output stage to an active state and still minimize power consumption. In all cases, the resistor shunting the transconductance amplifier output must be greater than 10kΩ to insure that the output will rise sufficiently high to obtain the maximum DMOS transistor drain current.

Start-Up Sequence

Upon initial power up of the HIP5061 in a typical application circuit, the voltage at V_C will be zero, and the DMOS transistor will be off. When the voltage at V_{DD} rises above the 10.3V typical threshold, the error amplifier output is enabled and the V_C voltage begins to rise in response to the low voltage at the FB terminal. When the V_C voltage rises above 1.5V the DMOS transistor begins to switch at the minimum duty cycle, and when it rises above 2.55V the duty cycle begins to increase. The V_C voltage (and peak DMOS transistor current) will then continue to rise until the voltage loop gains control and establishes regulation. Note that the rate of rise in the V_C voltage can be controlled by an external soft start circuit (See **Soft Start Implementation**).

If the V_C voltage is unrestricted in its rate of rise, then it will typically rise quickly to its maximum (peak current) value, causing the DMOS transistor to turn-on and stay on until it reaches the peak current value. At this point, the DMOS transistor begins switching, and the V_C voltage (and peak DMOS transistor current) will drop down to the level commanded by the voltage loop.

Using the Shunt Regulator

The internal 14V shunt regulator in conjunction with an external series resistor allows the IC to operate from quite high input voltages, limited only by power dissipation in the external resistor. When only higher voltages are available, a bootstrap or other 12V auxiliary supply can be used to eliminate this dissipation. The series resistor should be chosen to be as large as possible to reduce power dissipation at high line, while ensuring adequate V_{DD} voltage at low line. The maximum value for this resistor, ***R***, is given by:

$$R_{MAX}(\Omega) = \frac{V_{I,MIN} - 10.5}{0.033}$$

Where $\mathbf{V_I}$ is the input voltage to the power supply. The value chosen for this resistor must also result in a current, ***I***, into the V_{DD} clamp that is less than 105mA when the input voltage is at its maximum:

$$I_{MAX}(A) = \frac{\left(V_{I,MAX} - 13.3\right)}{R_{MAX}}$$

Inductor Selection

The selection of the energy storage inductor(s) L_{STOR} for a DC to DC converter has tremendous influence on the behavior of the converter. It is particularly important in light of the high level of integration (and necessarily few degrees of freedom) achieved in the HIP5061. There are several factors influencing the selection of this inductor. First, the inductance of L_{STOR} will determine the basic mode of operation for the converter: continuous or discontinuous current. In order to maximize the output power for the given maximum controllable DMOS transistor current, a converter may be designed to operate in continuous current mode (CCM). However, this tends to require a larger inductor, and for many converter topologies results in a feedback loop tha is difficult to stabilize. For these and other reasons, the inductor L_{STOR} may be chosen so as to operate the converter in discontinuous current mode (DCM). The relative merits of CCM and DCM operation for various topologies and the corresponding selection of L_{STOR} is well documented and will not be covered here.

A second factor influencing the selection of L_{STOR} is the stability requirement for current-mode control. This constraint is only applicable for converters operating in CCM, since open-loop instabilities of this type are not observed in converters operating in DCM. For marginal stability, the compensating ramp (internal to the HIP5061) must have a slope that is greater than one-half the difference between the inductor current's down slope and up slope. (To ensure stability for duty ratios D > 0.8, the slope of the compensating ramp should be equal to the inductor current downslope.) A generally accepted goal is to set the slope of the compensating ramp to be at least one-half of the inductor current down slope. Since there is no external control over the internal compensating ramp, one must be sure that the inductor is large enough so that the down slope of the inductor current is not too large. Table 2 summarizes this requirement for minimum inductance for several common topologies.

A third constraint on the size of the inductor is one that is common among current-mode controlled PWM converters, and applies to both DCM and CCM operation. The stable generation of the desired DMOS transistor pulse width depends on the accurate comparison of the error signal and the peak L_{STOR} (DMOS) transistor drain current. Thus, as the peak L_{STOR} ripple current becomes smaller, immunity from noise on the error signal is eventually reduced until the pulse width can no longer be adequately controlled. For the HIP5061, the inductor current ripple must be at least 200mA peak to peak to ensure proper control of the DMOS transistor current. This effectively establishes a maximum value for the inductor L_{STOR}, so as to maintain at least 200mA of ripple. Note that under extremely light or no load conditions, all converters will eventually operate in DCM, and the 200mA requirement will eventually be violated. Under these conditions, the HIP5061 will continue to regulate, although the switching of the DMOS transistor will be in a burst-mode, controlled by the Light Load Comparator. (See Figure 2.)

TABLE 2. MINIMUM INDUCTANCE FOR STABLE CCM OPERATION ABOVE 50% DUTY CYCLE

CONVERTER TYPE	MINIMUM INDUCTANCE
Boost	$L = \frac{V_O + V_D - V_{I,MIN}}{2M_{R,MIN}}$
SEPIC (Note 1)	$\frac{L_1 L_2}{L_1 + L_2} > \frac{V_O + V_D}{2M_{R,MIN}}$
Cuk (Note 2)	$\frac{L_1 L_2}{L_1 + L_2} > \frac{V_O - V_D}{2M_{R,MIN}}$
Flyback	$L_P > \left(\frac{N_P}{N_S}\right)\frac{(V_O + V_D)}{2M_{R,MIN}}$
Forward	$L > \left(\frac{N_S}{N_P}\right)\frac{(V_O + V_D)}{2M_{R,MIN}}$

NOTES:

1. Assumes that L_1 and L_2 are both CCM.
2. L = Inductance in Henrys, V_O = Output Voltage, V_D = Diode Voltage Drop, V_I = Input Voltage, $M_{R,MIN} = (\Delta I/\Delta t)_{MIN} = 0.45A/\mu s$, L_1 = Drain Inductor, L_2 = Secondary Inductor, N_P = Primary Turns, N_S = Secondary Turns

DMOS Transistor Turn-Off Snubber

In order to reduce dissipation in the DMOS transistor due to turn-off losses, the turn-off time has been minimized. However, the rapid reduction of current that occurs in the drain of the DMOS transistor can result in large transient voltages being induced across any parasitic inductance in the drain path. For this reason, it is important that such parasitic inductance be reduced by good, high frequency layout practices. Nevertheless, there are many instances (e.g., transformer isolated topologies) in which voltages in excess of 60V may be developed at the DMOS transistor drain. In some cases, a simple R-C snubber may be added to reduce the overshoot of the drain voltage to a safe level.

It is also possible that the large amount of ringing that can occur at the DMOS transistor drain at turn-off will induce noise in the IC. This noise may result in false triggering of the PWM latch, particularly at high peak DMOS transistor drain currents. Noise related instability can also be eliminated by the addition of a snubber, which will rapidly damp out such turn-off ringing. Good layout practices will reduce the need for such protective measures, and ensure that the DMOS transistor is not overstressed.

Under-Voltage Lockout

The V_{DD} input voltage is monitored by a comparator that holds off the DMOS transistor gate drive signal when the V_{DD} voltage is less that about 10.3V. The typical 0.5V hyster-

esis of this comparator is intended to reduce oscillation when the voltage at V_{DD} is in the vicinity of 10V. Note, however, that when an external series resistor is used to feed the shunt regulator, the voltage drop across this resistor (which sharply decreases when the IC shuts down), effectively reduces the hysteresis. To reduce the tendency for oscillation in the vicinity of the 10V threshold, the impedance of the source that feeds the DC to DC converter input should be minimized. The addition of a capacitor (1µF-47µF) at the V_{DD} terminal can also help to provide smooth turn-on or turn-off of the converter if the input supply rises or falls gradually through the V_{DD} Comparator threshold.

Peak Controllable DMOS Transistor Current

Figure 34 shows the guaranteed minimum, peak controllable DMOS transistor current versus duty cycle. This peak current value is established by the current limit circuitry, which effectively clamps the voltage at V_C (the error voltage) to perform current limiting. Since the sensed DMOS transistor current is summed with a compensating current ramp that begins its rise 1.5µs after the initiation of a cycle, current limiting will *begin* to occur at a peak DMOS transistor current that varies with the operating duty cycle. The highest current limit threshold occurs for D<0.375, where no ramp is added to the sensed DMOS transistor current. At higher operating duty ratios, the onset of current limit will occur at increasingly lower currents, due to the effect of adding the compensating ramp to the sensed current. Note that this curve represents guaranteed minimum values. The guaranteed maximum values are considerable higher, although they are still limited to levels that protect the IC.

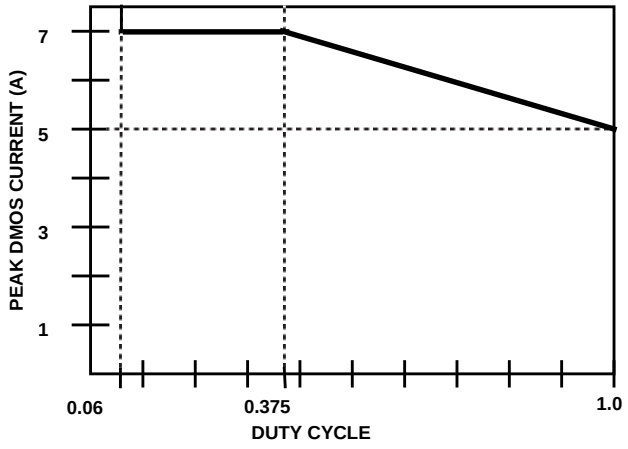


FIGURE 34. PEAK DMOS TRANSISTOR DRAIN CURRENT vs DUTY CYCLE

When the DMOS transistor first turns ON there may be substantial current spikes exceeding the normal maximum peak current established by the current control stages within the IC. To prevent these spurious spikes from conveying erroneous information to the Current Comparator, a 100ns blanking signal is applied to the current monitoring circuitry. Thus, there is no peak current protection during the first 6% of the duty cycle (see Figure 36).

DMOS Transistor Turn-On Noise

Although the large DMOS transistor turn-on current spikes are “blanked over” by the control circuit, it is important to minimize these current spikes, since they often result in voltage spikes considerably below the device substrate that can activate parasitic devices within the IC. Such activation of parasitic devices will often result in improper operation of the IC. An external terminal labeled V_G brings out the power supply to the gate drive circuitry. This allows for the control of the peak current delivered to the gate of the DMOS transistor, which in turn establishes the turn-on speed. The V_G pin may be externally bypassed for the fastest possible turn-on, or series resistance may be added with no bypassing capacitor to slow down the turn-on of the DMOS transistor. Depending upon the actual layout of the supply, it is generally recommended that a series resistor be added (10Ω-150Ω) so that the DMOS transistor turn-on speed is reduced. By properly adjusting the turn-on speed, undershoot can be avoided while turn-on switching losses are kept to a minimum.

Soft Start Implementation

It is often desirable to allow the regulator to start up slowly, Figure 35 shows one means of implementing this action. The normally high output current from the HIP5061 transconductance amplifier (when V_{FB} = 0 and V_{REF} = 5.1V) is directed to an external capacitor through a diode. This slows down the rate of rise of the voltage at the V_C terminal. After the regulator starts, the external capacitor is charged to V_{DD} and is effectively removed from the frequency compensation network by a reverse biased diode. To ensure rapid recycling of the capacitor voltage with removal of power, a diode is placed across the 100kΩ resistor. Logic Shutdown Input (V_C Pin).

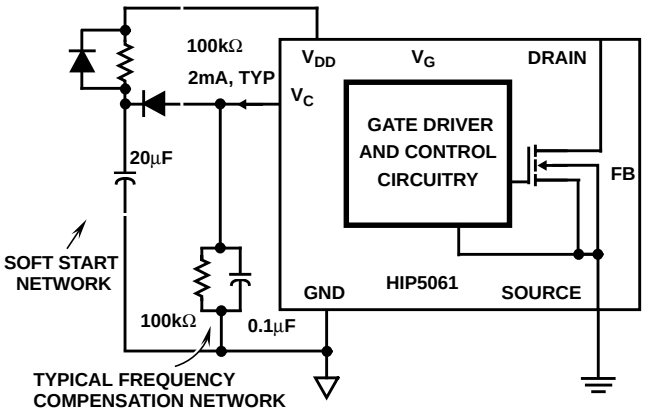


FIGURE 35. SOFT START CIRCUIT FOR THE HIP5061

The DC to DC converter may be shut down by returning the V_C output terminal to ground. A sinking current greater than 4mA will insure that this output is pulled to ground. It must be remembered that once switching operation ceases, the drain of the DMOS transistor is open. When the supply is in the Boost configuration, the output voltage is not zero but the input voltage less diode and inductor voltage drops. If the SEPIC

topology is used, this is not the case. Shutting down the regulator via the V_C terminal will cut off the output. Figure 36 shows two methods of shutting down the IC. In each case the current sinking circuit must be able to sink at least 4mA, the maximum current from the HIP5061 V_C terminal.

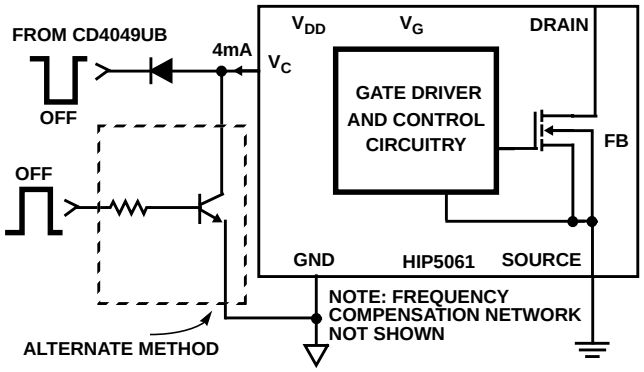


FIGURE 36. TWO METHODS OF SHUTTING DOWN THE HIP5061

Mounting, Layout and Component Selection

The TO-220 package with its gullwing leads was designed to be surface mounted. To aid in the external reduction of lead length and hence inductance and resistance, the IC leads were staggered. To keep the inductance and resistance of the critical drain terminal as low as possible, it is suggested that the PC trace to the DMOS transistor drain terminal be made as wide as possible. The adjacent source terminal is not recommended to be used and therefore allows the metal to the drain terminal to be widened beyond the normal widths for these terminals. Figure 37 illustrates these points.

One of the most important aspects to the proper application of this device is high frequency bypassing. In a Boost converter, for example, there should be a low-inductance interconnect from the DMOS transistor drain, through the output diode and capacitors, and returning to the TAB (source) of the HIP5061. Inductance in this line results in large transient voltages on the DMOS transistor drain terminal which can result in voltages above the maximum DMOS transistor drain voltage rating.

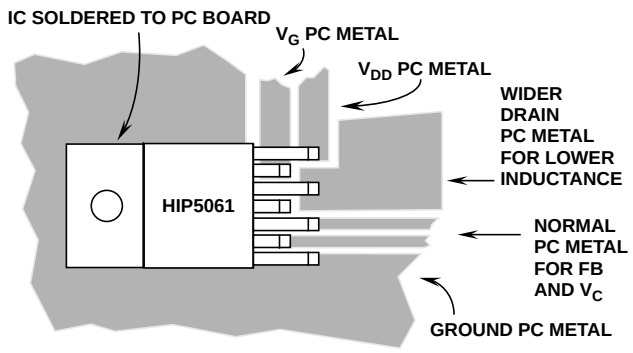


FIGURE 37. SHOWING WIDER PC BOARD METAL FOR CRITICAL

All the capacitors shown with values of 1µF or less are of the multilayer ceramic type with the X7R dielectric material. This material has a fairly flat voltage and temperature coefficient that assures that the capacitance remains comparatively constant at extreme operating temperatures and voltages. The multilayer construction allows for comparatively large values with good volumetric efficiency and low inductance. Capacitors around the power input and output circuits should be returned to the device TAB via a low inductance ground plane. This TAB is internally connected to the DMOS transistor source. The schematic diagram of Figure 38 was drawn with the diagonal leads to show the critical paths for the various high frequency elements. These short interconnects assure the lowest inductance around the output power circuit.

Design of a 28V, 1.8A Boost Converter

Figure 38 shows the schematic diagram and a parts list of a 50W supply designed with the HIP5061. Table 3 tabulates the performance of the power supply.

TABLE 3. TYPICAL LABORATORY PERFORMANCE OF 50W, 28V/1.8A REGULATOR

Input Voltage	11V to 16V
Line Regulation	12mV/V
Output Voltage	28.0V
Load Regulation	64mV/A
Output Ripple, FL (20MHz BW)	600mV P-P
Output Ripple, after Filter, FL (20MHz BW)	80mV P-P
Efficiency: V_I = 11V, I_L = 0.18A	90%
V_I = 11V, I_L = 1.8A	89%
V_I = 16V, I_L = 0.18A	73%
V_I = 16V, I_L = 1.8A	93%

Inductor Selection

In order to maximize the output power for the given maximum controllable DMOS transistor current, this converter has been designed to operate in continuous current mode (CCM). In this mode, the inductor value will generally be large, resulting in a lower inductor ripple current and a lower peak DMOS current. To ensure that the converter operates in CCM over the usable range of input voltage and output current, the value of L2 must be greater than the “critical inductance,” given by

$$L_{CRIT} = \frac{V_O V_{I,MAX}^2 \left(V_O + V_D - V_{I,MAX}\right) T_S}{2 P_{O,MIN} \left(V_O + V_D\right)^2}$$

$$= \frac{(28)(16)^2 (28 + 0.5 - 16) 4\times10^{-6}}{2(5.6)(28 + 0.5)^2}$$

$$= 39\mu H$$

where $P_{O,MIN}$ has been arbitrarily chosen as 5.6W, corresponding to an output current of 0.2A, and V_D is the forward voltage of CR1. Thus, for L2 > 39µH, the converter will be in CCM for V_I = 11V to 16V and I_L = 0.2A to 1.8A.

A second factor influencing the selection of L2 is the stability requirement for current-mode control. Using the above equation for L_{MIN} for the Boost converter:

$$L > \frac{V_O + V_D - V_{I,MIN}}{2 \times M_{RAMP,MIN}} = \frac{28 + 0.5 - 11}{2 \times \left(0.45 \times 10^6 A/S\right)} = 19\mu H$$

Thus, L2 must be at least 19µH to ensure good stability of the current loop, and a choice of L2 = 40µH satisfies this requirement, while maintaining CCM operation over an extremely wide load range.

The chosen core material for L2 is Kool Mu ferrous alloy powder from Magnetics, Inc. This material was chosen because of its relatively low cost, while its losses due to AC flux are five to ten times less than conventional powdered iron.

Loop Compensation

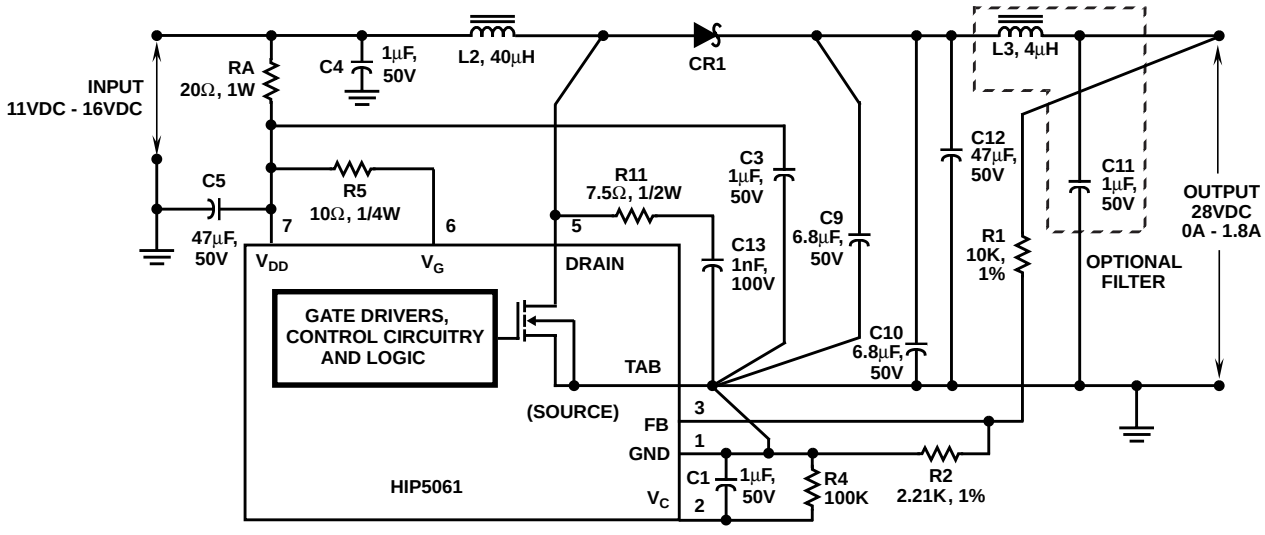
The control to output transfer function for this current-mode boost converter has the following characteristics over the specified load and line conditions:

D.C. Gain: 20dB-40dB
Pole at 88Hz-880Hz
LHP Zero at 1MHz
RHP Zero at 11.0kHz-110kHz
Double Pole at 80kHz (from filter)

To stabilize the voltage loop, it is necessary to establish the unity gain crossover frequency well below the RHP zero, since this zero introduces positive gain and negative phase. A crossover of 4kHz is fairly conservative, and is achieved by adding a 1µF capacitor at the VC pin, which provides near infinite DC gain, and about -5dB of gain at 4kHz. This results in a phase margin of about 15° at full load. Note that R4 is required for proper operation of the transconductance amplifier, since it is providing bias current for the output stage as discussed under Using the Transconductance Error Amplifier section.

Output Filter Design

Inductor L3 was chosen with C11 to provide at least 15dB of ripple attenuation at the switching frequency. The corner frequency (80kHz) of this filter is well above the crossover frequency of the voltage loop (4kHz), and has no effect on stability. This secondary LC filter was used to reduce output ripple instead of a lower-cost, high-value, low ESR aluminum electrolytic capacitor to demonstrate the reduction in volume possible at this switching frequency. A lower cost solution could achieve the same output ripple by replacing C9,10,12 and L3 with one or two large capacitors (e.g.,



PARTS LIST

RA	20Ω, 1W, Wirebound - Dale RWR81S20R0FR or Equivalent
R1	10K, 1%
R2	2.2K, 1%
R4	100K, 1/4W
R5	10Ω, 1/4W
R11	7.5Ω, 1/2W, Carbon - Allen Bradley EB75G5
C1, C3, C4 and C11	1µF, 50V, Ceramic - Murata Erie RPE113X7R105050V
C5 and C12	47µF, 50V, Alum - United Chemicon 515D476M050
C9 and C10	6.8µF, 50V, Ceramin - Mallory M60u6r8M50
C13	1nF, 100V, Ceramin - Kemet C322C102K1G5CA
CR1	Schottky Diode - Motorola MBRD360
L2	40µH at 5A, Pulse Engineering PE - 53571
L3	4µH at 5.5A, Pulse Engineering PE - 53570

FIGURE 38. HIP5061 50W, 28V BOOST REGULATOR SCHEMATIC AND PARTS LIST

390µF, 50V, type 673D from United Chemicon). This change would also greatly improve load transient response, provided that the loop compensation is appropriately adjusted. Note that in the circuit of Figure 38, capacitor C12 does not significantly affect output ripple, but is necessary to absorb the energy stored in L2 during severe load transients. In the event of a step change in load from 1.8A to 0A, C12 will limit the output voltage overshoot to about 10V and protect the drain of the DMOS transistor from overvoltage breakdown.

Input and V_{DD} Filters

Since the boost converter is current fed, input filtering is easily achieved by the addition of a small capacitor C4. This capacitor provides nearly 40dB of ripple current attenuation for the input, reducing the AC ripple current flowing into the converter to less than 200mA.

R5 and C3 have been chosen to provide good filtering of high frequency pulse currents. R5 provides isolation between the analog V_{DD} pin and the high pulse current V_G pin, and also provides a means to control the turn-on speed of the DMOS transistor by limiting the peak current available to the internal gate drive circuitry. Thus the output transition time may be increased to prevent drain voltage undershoot. Undershoot may result in activation of device parasitics and improper circuit operation. For the two-layer board used for this design, C3 could be reduced to 0.22µF without affecting circuit operation. C5 was added to provide low-frequency filtering at the V_{DD} pin. This reduces the tendency of the circuit to oscillate off and on when the voltage at the V_{DD} pin s in the vicinity of the under voltage lockout threshold, typically 10V, and the output power is high (30W - 50W).

Shunt Regulator Resistor

Resistor RA has been chosen to be as large as possible to reduce power dissipation at high line, while ensuring adequate V_{DD} voltage at low line. Note that the guaranteed range of input voltage for proper operation of this circuit is 11.2V to 15.3VDC, based upon data sheet limits. However, the circuit was found to perform well at room temperature for V_I = 10.7VDC to 17VDC. The maximum value for RA is

$$R_{MAX} = \frac{V_{I,MIN} - 10.5}{0.033} = 21\Omega$$

RA has been chosen as 20Ω, which results in a current into the V_{DD} clamp that is less than 105mA when the input voltage is at its maximum:

$$I_{MAX} = \frac{\left(V_{I,MAX} - 13.3\right)}{20.0} = 100mA < 105mA$$

Snubber Network

A snubber network has been added to reduce the ringing at the drain due to parasitic layout inductances. In particular, under severe load transient conditions, this snubber is necessary to protect the drain from voltage breakdown. A second benefit of reducing the noise and ringing at the drain is that it reduces the tendency of the HIP5061 to exhibit noise-related instabilities at high peak DMOS transistor currents (4A-6A). A value of 1000pF was chosen for C13, since this is adequate to dampen the ringing associated with the 200pF drain capacitance of the DMOS transistor. R11 was chosen as 7.5Ω to provide the best possible dampening given the parasitic inductances that exist in the layout. Note that this snubber may not be necessary if the layout of the circuit were improved, or if the application did not push the envelope of DMOS transistor current.

Other Power Supply Topologies

Figure 39 shows three other topologies besides the Boost that may be implemented with the grounded source DMOS power transistor used in the HIP5061. Other, more complex power supply topologies such as the Quadratic are also possible to implement with the HIP5061. One noteworthy feature of the Quadratic topology as shown in Figure 41 is the wide input to output voltage transfer ratio possible with reasonable duty cycles. Duty cycles that are not near the Minimum DMOS transistor “ON” Time specification shown in the Data Sheet. This permits easier control at the extremes of the transfer ratios. Compensating the control loop can pose challenges because of the wider changes in the transfer ratio and hence loop gain.

The SEPIC topology[11,13] does not have quite as wide input-output voltage range with reasonably controlled duty cycles as the Quadratic converter mentioned above, but it does allow both voltage increase and decrease with the same circuit. This is particularly advantageous when a power supply is being used in the stabilizing mode and isolation is not required. For example, in an application where a regulated 24V output is required and the input voltage varies ±20% from a nominal 24V. The SEPIC supply can provide both the Boost and Buck functions.

Another outstanding advantage of the SEPIC topology is its fault isolation of the input and output voltage. All energy is transferred via the coupling capacitor. Moreover if the clock stops, voltage transfer stops. If the switching transistor shorts there is no output. The Buck circuit will apply full input voltage to the load with a shorted transistor. This is reason that the SEPIC topology is referred to as the fail-safe Buck.

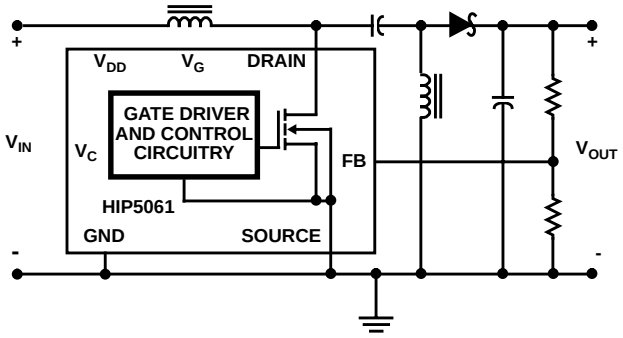


FIGURE 39A. SEPIC (FAIL-SAFE BUCK) CONVERTER

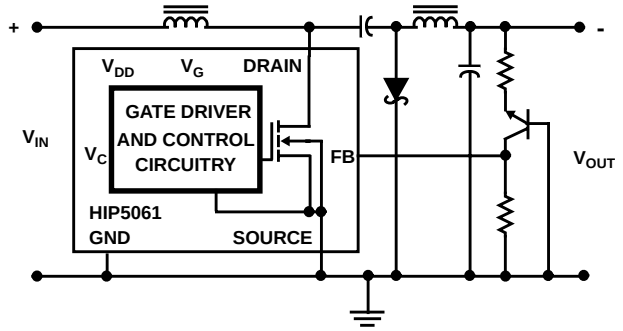


FIGURE 39B. CUK CONVERTER

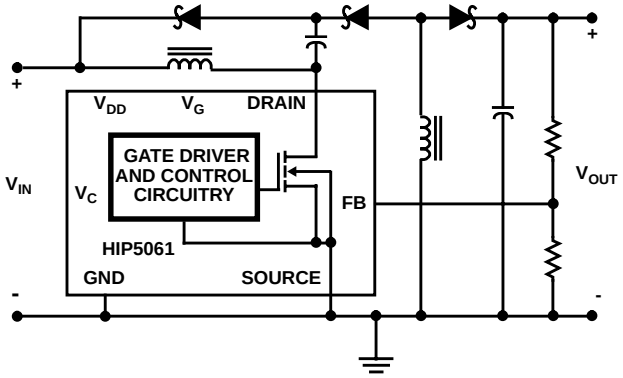


FIGURE 39C. QUADRATIC CONVERTER

FIGURE 39. THREE OTHER TOPOLOGIES

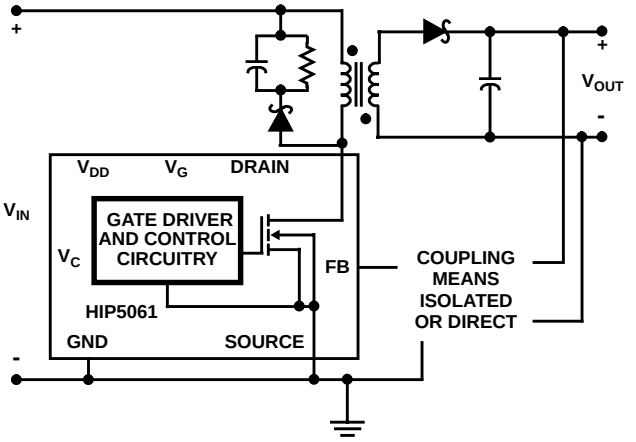


FIGURE 40. FLYBACK CONVERTER

It should be noted that when the Cuk topology is implemented, a transistor current source is used to convert the negative output voltage of the Cuk converter to a current that is level shifted to the FB terminal on the HIP5061.

Two other useful topologies that may be used are the Forward and the Flyback as shown in Figure 40 and Figure 41. As shown, they may either be operated as an isolated or non-isolated converter.

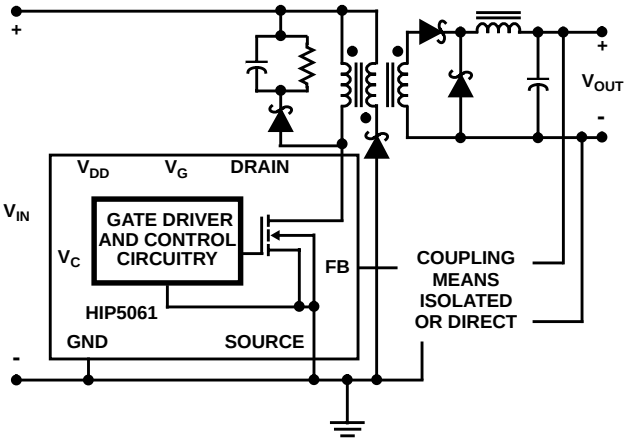


FIGURE 41. FORWARD CONVERTER

Both the SEPIC and the Boost topologies may be operated at high voltages with the addition of a high voltage cascode . Figure 42 shows the Cascode SEPIC converter that is essentially limited by the selection of the external power transistor. The burden of voltage, and power is placed upon the external transistor. The HIP5061 still performs the drain current sampling and the control function is the same as the non cascode configuration.

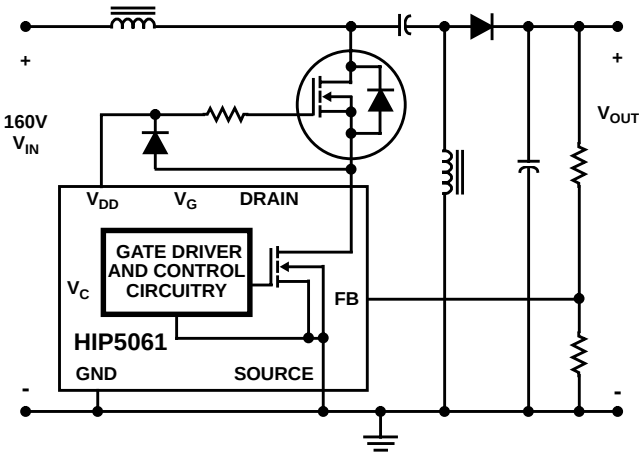


FIGURE 42. OFF LINE CASCODE SEPIC

Figure 43 shows the voltage transfer as a function of duty cycle for the power supply topologies discussed.

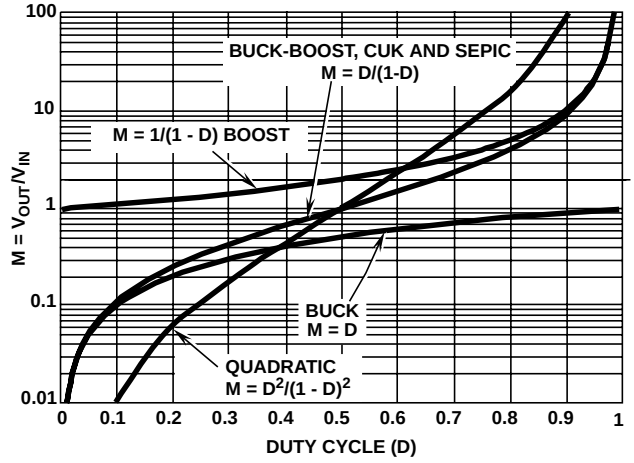


FIGURE 43. VOLTAGE TRANSFER AS A FUNCTION OF DUTY CYCLE FOR VARIOUS TOPOLOGIES

References

[1] Cassani, John C.; Hurd, Jonathan J. and Thomas, David R., Wittlinger, H.A.; Hodgins, Robert G.; *Sophisticated Control IC Enhances 1MHz Current Controlled Regulator Performance*, High Frequency Power Conversion (HFPC) conference proceedings, May 1992, pp. 167-173

[2] Smith, Craig D. and Cassani, *Distributed Power Systems Via ASICs Using SMT*, Surface Mount Technology, October 1990

[3] Maksimovic and Cuk, *Switching Converters With Wide DC Conversion Range*, High Frequency Power Conversion (HFPC) conference record, May 1989

[5] Maksimovic and Cuk, *General Properties and Synthesis of PWM DC-to-DC Converters*, IEEE Power Electronics Specialists Conference (PESC) record, June 1989

[6] Sokal and Sokal, *Class E - A New Class of High Efficiency Tuned Single-Ended Switching Power Amplifiers*, IEEE Journal of Solid-State Circuits, June 1975, pp. 168-176

[7] Mansmann, Jeff; Shafer, Peter and Wildi, Eric, *Maximizing the Impact of Power ICs Via a Time-to-Market CAD Driven Power ASIC Strategy*, Applied Power and Electronics Conference and Exposition (APEC) proceedings, February 1992, pp. 23-27

[8] Severns and Bloom, *Modern DC-to-DC Switchmode Power Converter Circuits*, Van Nostrand Reinhold, 1985

[9] Sum, K., *Switch Mode Power Conversion - Basic Theory and Design*, Marcel Dekker, In., 1984

[10] Pressman, A., *Switching and Linear Power Supply, Power Converter Design*, Hayden Book Co., 1977

[11] Massey, R.P. and Snyder, *E.C., High Voltage Single-Ended DC-DC Converter*, IEEE Power Electronics Specialists Conference (PESC) record, 1977, pp. 156-159

[12] Clarke, P., *A New Switched-Mode Power Conversion Topology Provides Inherently Stable Response*, POWERCON 10 proceedings, March 1983, pp. E2-1 through E2-7

[13] Intersil Application Notes AN9208 and AN9212.1