

# HM5116100 Series

16 M FP DRAM (16-Mword × 1-bit)  
4 k Refresh

# HITACHI

ADE-203-646E (Z)  
Rev. 5.0  
Nov. 1997

## Description

The Hitachi HM5116100 is a CMOS dynamic RAM organized 16,777,216-word × 1-bit. It employs the most advanced 0.5μm CMOS technology for high performance and low power. The HM5116100 offers Fast Page Mode as a high speed access mode. It is packaged in 26-pin plastic SOJ.

## Features

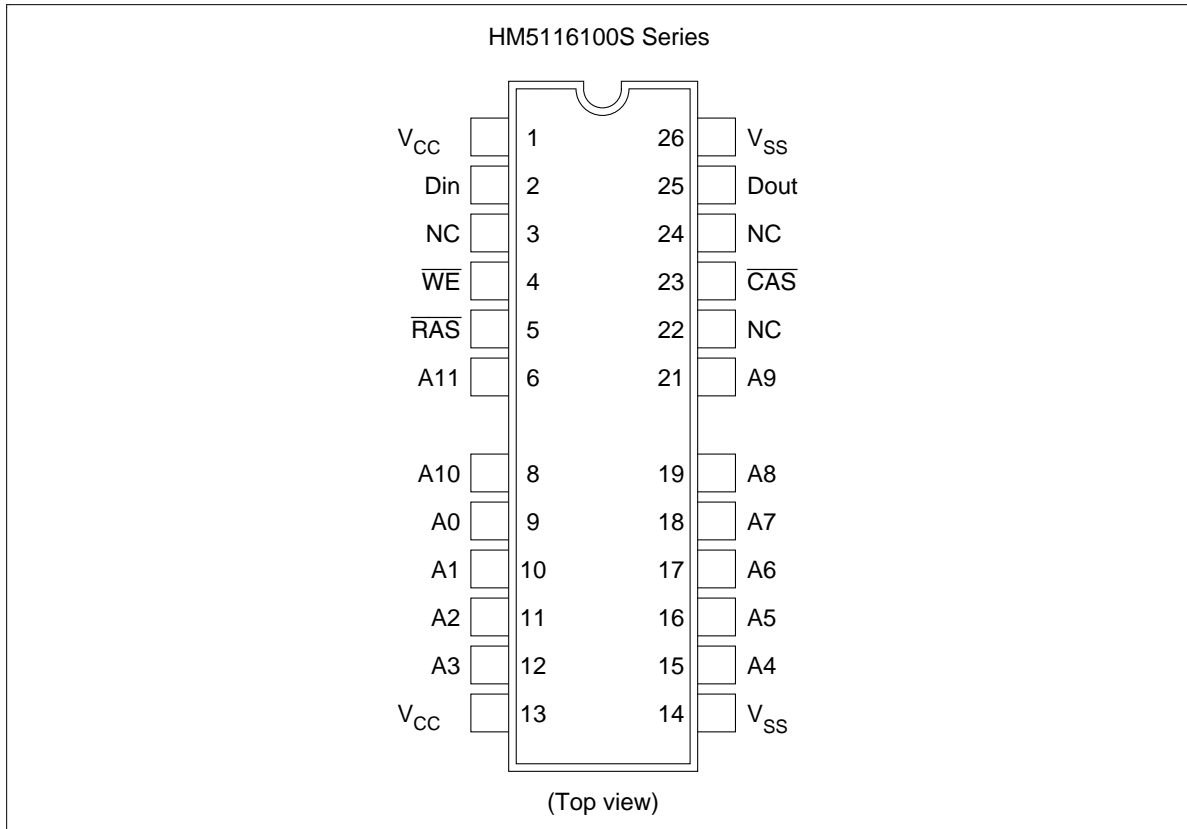
- Single 5 V (±10%)
- Access time: 60 ns/70 ns (max)
- Power dissipation
  - Active mode: 440 mW/385 mW (max)
  - Standby mode 11 mW (max)
- Fast page mode capability
- Refresh cycles
  - 4096 refresh cycles : 64 ms
- 3 variations of refresh
  - $\overline{\text{RAS}}$ -only refresh
  - CAS-before- $\overline{\text{RAS}}$  refresh
  - Hidden refresh
- Test function
  - 16-bit parallel test mode

## Ordering Information

Type No.	Access time	Package
HM5116100S-6	60 ns	300-mil 26-pin plastic SOJ (CP-26/24DB)
HM5116100S-7	70 ns	

## HM5116100 Series

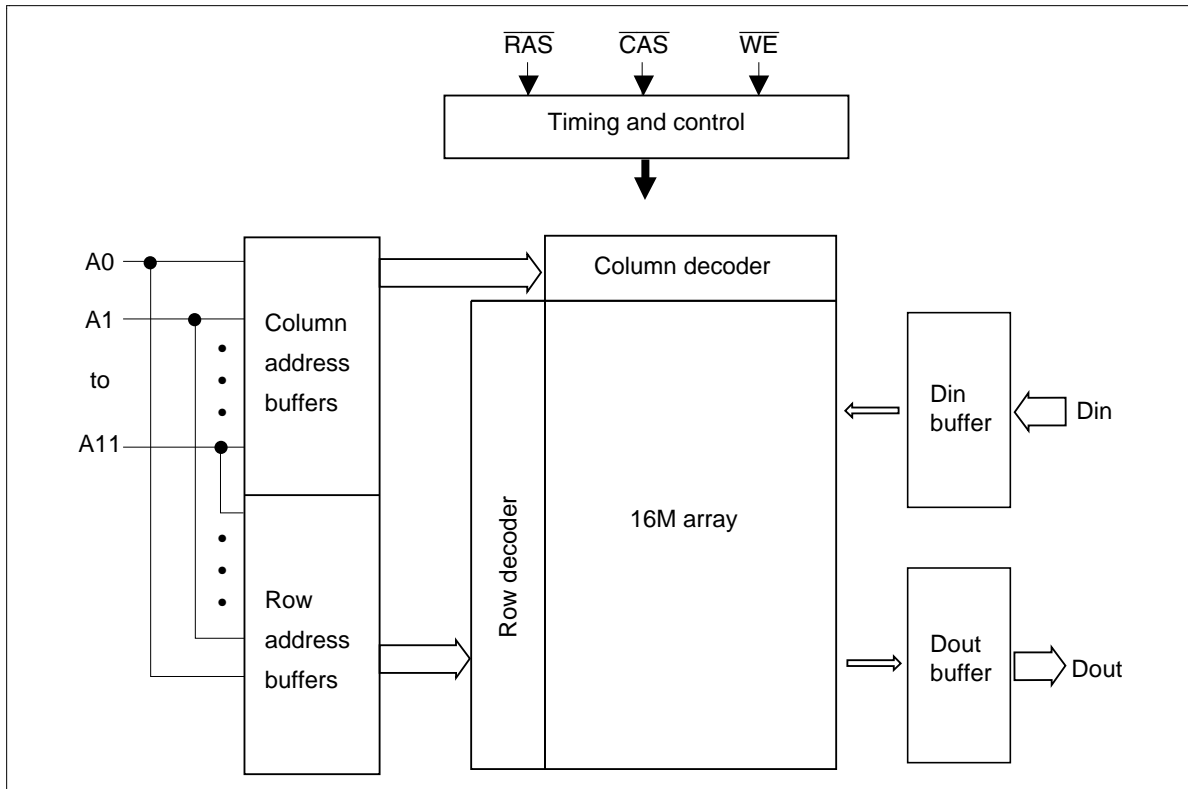
### Pin Arrangement



### Pin Description

Pin name	Function
A0 to A11	Address input <ul style="list-style-type: none"> <li>• Row/Refresh A0 to A11</li> <li>• Column A0 to A11</li> </ul>
Din	Data input
Dout	Data output
$\overline{\text{RAS}}$	Row address strobe
$\overline{\text{CAS}}$	Column address strobe
$\overline{\text{WE}}$	Read/write enable
$V_{\text{CC}}$	Power supply
$V_{\text{SS}}$	Ground
NC	No connection

**Block Diagram**



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## HM5116100 Series

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### Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
Voltage on any pin relative to $V_{SS}$	$V_T$	-1.0 to +7.0	V
Supply voltage relative to $V_{SS}$	$V_{CC}$	-1.0 to +7.0	V
Short circuit output current	$I_{out}$	50	mA
Power dissipation	$P_T$	1.0	W
Operating temperature	$T_{opr}$	0 to +70	°C
Storage temperature	$T_{stg}$	-55 to +125	°C

### Recommended DC Operating Conditions ( $T_a = 0$ to +70°C)

Parameter	Symbol	Min	Typ	Max	Unit	Note
Supply voltage	$V_{CC}$	4.5	5.0	5.5	V	1
Input high voltage	$V_{IH}$	2.4	—	6.5	V	1
Input low voltage	$V_{IL}$	-1.0	—	0.8	V	1

Note: 1. All voltage referred to  $V_{SS}$

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### DC Characteristics (Ta = 0 to +70°C, V<sub>CC</sub> = 5 V ± 10%, V<sub>SS</sub> = 0 V)

Parameter	Symbol	HM5116100				Unit	Test conditions
		-6		-7			
		Min	Max	Min	Max		
Operating current <sup>*1, *2</sup>	I <sub>CC1</sub>	—	80	—	70	mA	t <sub>RC</sub> = min
Standby current	I <sub>CC2</sub>	—	2	—	2	mA	TTL interface RAS, CAS = V <sub>IH</sub> Dout = High-Z
		—	1	—	1	mA	CMOS interface RAS, CAS ≥ V <sub>CC</sub> - 0.2V Dout = High-Z
RAS-only refresh current <sup>2</sup>	I <sub>CC3</sub>	—	80	—	70	mA	t <sub>RC</sub> = min
Standby current <sup>*1</sup>	I <sub>CC5</sub>	—	5	—	5	mA	RAS = V <sub>IH</sub> , CAS = V <sub>IL</sub> Dout = enable
CAS-before-RAS refresh current	I <sub>CC6</sub>	—	80	—	70	mA	t <sub>RC</sub> = min
Fast page mode current <sup>*1, *3</sup>	I <sub>CC7</sub>	—	70	—	60	mA	t <sub>PC</sub> = min
Input leakage current	I <sub>LI</sub>	-10	10	-10	10	μA	0 V ≤ Vin ≤ 7 V
Output leakage current	I <sub>LO</sub>	-10	10	-10	10	μA	0 V ≤ Vout ≤ 7 V Dout = disable
Output high voltage	V <sub>OH</sub>	2.4	V <sub>CC</sub>	2.4	V <sub>CC</sub>	V	High Iout = -5 mA
Output low voltage	V <sub>OL</sub>	0	0.4	0	0.4	V	Low Iout = 4.2 mA

- Notes: 1. I<sub>CC</sub> depends on output load condition when the device is selected. I<sub>CC</sub> max is specified at the output open condition.  
 2. Address can be changed once or less while RAS = V<sub>IL</sub>.  
 3. Address can be changed once or less while CAS = V<sub>IH</sub>.

### Capacitance (Ta = 25°C, V<sub>CC</sub> = 5 V ± 10%)

Parameter	Symbol	Typ	Max	Unit	Notes
Input capacitance (Address, Data-in)	C <sub>I1</sub>	—	5	pF	1
Input capacitance (Clocks)	C <sub>I2</sub>	—	7	pF	1
Output capacitance (Data-out)	C <sub>O</sub>	—	7	pF	1, 2

- Notes: 1. Capacitance measured with Booton Meter or effective capacitance measuring method.  
 2. CAS = V<sub>IH</sub> to disable Dout.

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**AC Characteristics** ( $T_a = 0$  to  $+70^\circ\text{C}$ ,  $V_{CC} = 5\text{ V} \pm 10\%$ ,  $V_{SS} = 0\text{ V}$ )<sup>\*1, \*2, \*16</sup>

### Test Conditions

- Input rise and fall time : 5 ns
- Input timing reference levels : 0.8 V, 2.4 V
- Output load : 2 TTL gate +  $C_L$  (100 pF) (Including scope and jig)

### Read, Write, Read-Modify-Write and Refresh Cycles (Common parameters)

Parameter	Symbol	HM5116100				Unit	Notes
		-6		-7			
		Min	Max	Min	Max		
Random read or write cycle time	$t_{RC}$	110	—	130	—	ns	
$\overline{\text{RAS}}$ precharge time	$t_{RP}$	40	—	50	—	ns	
$\overline{\text{CAS}}$ precharge time	$t_{CP}$	10	—	10	—	ns	
$\overline{\text{RAS}}$ pulse width	$t_{RAS}$	60	10000	70	10000	ns	
$\overline{\text{CAS}}$ pulse width	$t_{CAS}$	15	10000	18	10000	ns	
Row address setup time	$t_{ASR}$	0	—	0	—	ns	
Row address hold time	$t_{RAH}$	10	—	10	—	ns	
Column address setup time	$t_{ASC}$	0	—	0	—	ns	
Column address hold time	$t_{CAH}$	10	—	15	—	ns	
$\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ delay time	$t_{RCD}$	20	45	20	52	ns	3
$\overline{\text{RAS}}$ to column address delay time	$t_{RAD}$	15	30	15	35	ns	4
$\overline{\text{RAS}}$ hold time	$t_{RSH}$	15	—	18	—	ns	
$\overline{\text{CAS}}$ hold time	$t_{CSH}$	60	—	70	—	ns	
$\overline{\text{CAS}}$ to $\overline{\text{RAS}}$ precharge time	$t_{CRP}$	5	—	5	—	ns	
Transition time (rise and fall)	$t_T$	3	50	3	50	ns	5

## HM5116100 Series

### Read Cycle

Parameter	Symbol	HM5116100				Unit	Notes
		-6		-7			
		Min	Max	Min	Max		
Access time from $\overline{\text{RAS}}$	$t_{\text{RAC}}$	—	60	—	70	ns	6, 7, 17
Access time from $\overline{\text{CAS}}$	$t_{\text{CAC}}$	—	15	—	18	ns	7, 8, 15, 17
Access time from address	$t_{\text{AA}}$	—	30	—	35	ns	7, 9, 15, 17
Read command setup time	$t_{\text{RCS}}$	0	—	0	—	ns	
Read command hold time to $\overline{\text{CAS}}$	$t_{\text{RCH}}$	0	—	0	—	ns	10
Read command hold time to $\overline{\text{RAS}}$	$t_{\text{RRH}}$	0	—	0	—	ns	10
Column address to $\overline{\text{RAS}}$ lead time	$t_{\text{RAL}}$	30	—	35	—	ns	
Column address to $\overline{\text{CAS}}$ lead time	$t_{\text{CAL}}$	30	—	35	—	ns	
$\overline{\text{CAS}}$ to output in low-Z	$t_{\text{CLZ}}$	0	—	0	—	ns	
Output data hold time	$t_{\text{OH}}$	3	—	3	—	ns	
Output buffer turn-off time	$t_{\text{OFF}}$	—	15	—	15	ns	11

### Write Cycle

Parameter	Symbol	HM5116100				Unit	Notes
		-6		-7			
		Min	Max	Min	Max		
Write command setup time	$t_{\text{WCS}}$	0	—	0	—	ns	12
Write command hold time	$t_{\text{WCH}}$	10	—	15	—	ns	
Write command pulse width	$t_{\text{WP}}$	10	—	10	—	ns	
Write command to $\overline{\text{RAS}}$ lead time	$t_{\text{RWL}}$	15	—	18	—	ns	
Write command to $\overline{\text{CAS}}$ lead time	$t_{\text{CWL}}$	15	—	18	—	ns	
Data-in setup time	$t_{\text{DS}}$	0	—	0	—	ns	13
Data-in hold time	$t_{\text{DH}}$	10	—	15	—	ns	13

## HM5116100 Series

### Read-Modify-Write Cycle

Parameter	Symbol	HM5116100				Unit	Notes
		-6		-7			
		Min	Max	Min	Max		
Read-modify-write cycle time	$t_{RWC}$	130	—	153	—	ns	
$\overline{RAS}$ to $\overline{WE}$ delay time	$t_{RWD}$	60	—	70	—	ns	12
$\overline{CAS}$ to $\overline{WE}$ delay time	$t_{CWD}$	15	—	18	—	ns	12
Column address to $\overline{WE}$ delay time	$t_{AWD}$	30	—	35	—	ns	12

### Refresh Cycle

Parameter	Symbol	HM5116100				Unit	Notes
		-6		-7			
		Min	Max	Min	Max		
$\overline{CAS}$ setup time (CBR refresh cycle)	$t_{CSR}$	5	—	5	—	ns	
$\overline{CAS}$ hold time (CBR refresh cycle)	$t_{CHR}$	10	—	10	—	ns	
$\overline{WE}$ setup time (CBR refresh cycle)	$t_{WRP}$	0	—	0	—	ns	
$\overline{WE}$ hold time (CBR refresh cycle)	$t_{WRH}$	10	—	10	—	ns	
$\overline{RAS}$ precharge to $\overline{CAS}$ hold time	$t_{RPC}$	5	—	5	—	ns	

### Fast Page Mode Cycle

Parameter	Symbol	HM5116100				Unit	Notes
		-6		-7			
		Min	Max	Min	Max		
Fast page mode cycle time	$t_{PC}$	40	—	45	—	ns	
Fast page mode $\overline{RAS}$ pulse width	$t_{RASP}$	—	100000	—	100000	ns	14
Access time from $\overline{CAS}$ precharge	$t_{CPA}$	—	35	—	40	ns	7, 15, 17
$\overline{RAS}$ hold time from $\overline{CAS}$ precharge	$t_{CPRH}$	35	—	40	—	ns	



## HM5116100 Series

### Fast Page Mode Read-Modify-Write Cycle

Parameter	Symbol	HM5116100				Unit	Notes
		-6		-7			
		Min	Max	Min	Max		
Fast page mode read-modify-write cycle time	$t_{PRWC}$	60	—	68	—	ns	
$\overline{WE}$ delay time from $\overline{CAS}$ precharge	$t_{CPW}$	35	—	40	—	ns	12

### Test Mode Cycle \*16

Parameter	Symbol	HM5116100				Unit	Notes
		-6		-7			
		Min	Max	Min	Max		
Test mode $\overline{WE}$ setup time	$t_{WTS}$	0	—	0	—	ns	
Test mode $\overline{WE}$ hold time	$t_{WTH}$	10	—	10	—	ns	

### Refresh Cycle

Parameter	Symbol	Max	Unit	Note
Refresh period	$t_{REF}$	64	ms	4096 cycles

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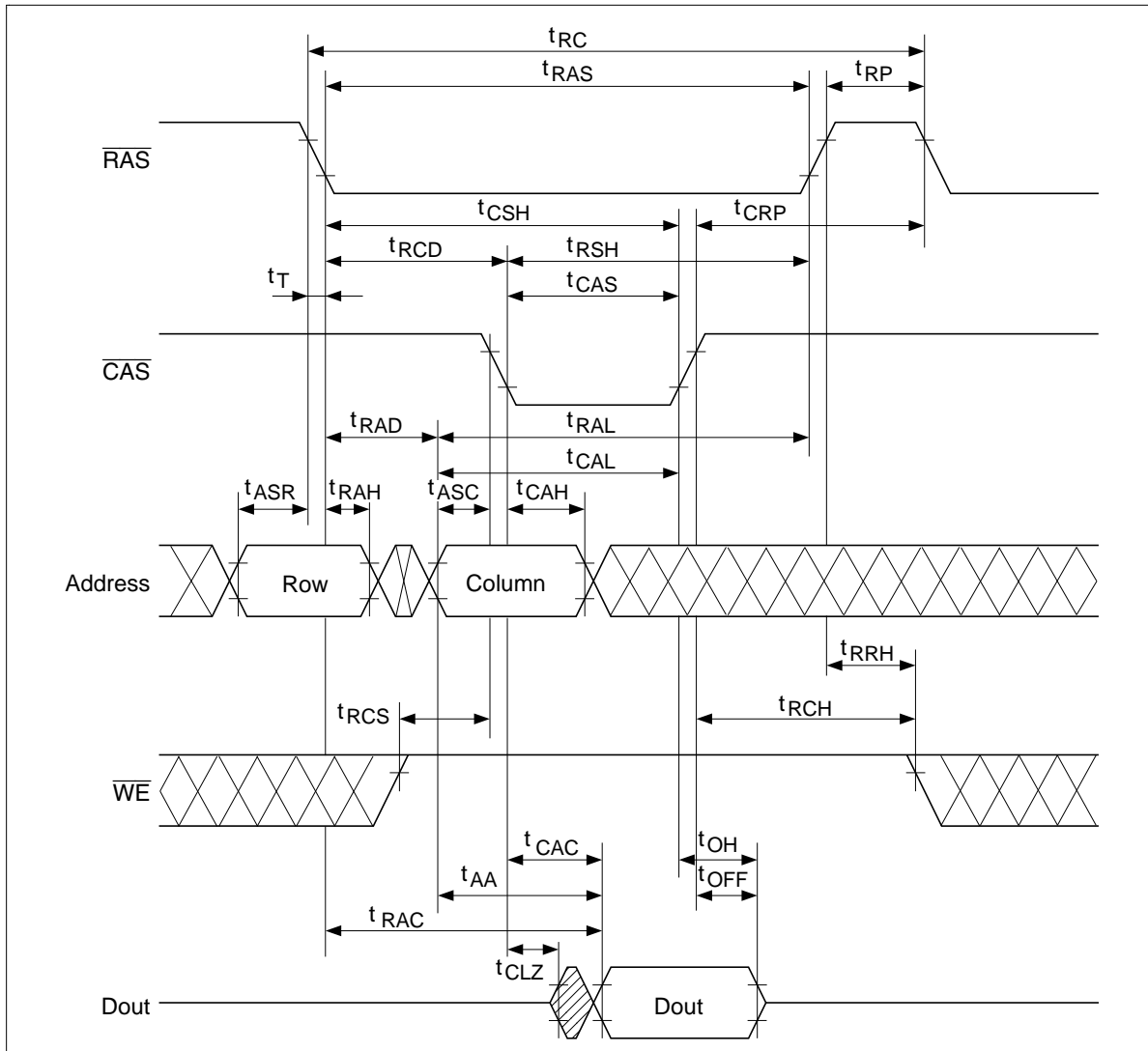
## HM5116100 Series

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- Notes:
1. AC measurements assume  $t_r = 5$  ns.
  2. An initial pause of 200  $\mu$ s is required after power up followed by a minimum of eight initialization cycles (any combination of cycles containing RAS-only refresh or CAS-before-RAS refresh). If the internal refresh counter is used, a minimum of eight CAS-before-RAS refresh cycles are required.
  3. Operation with the  $t_{RCD}$  (max) limit insures that  $t_{RAC}$  (max) can be met,  $t_{RCD}$  (max) is specified as a reference point only; if  $t_{RCD}$  is greater than the specified  $t_{RCD}$  (max) limit, then access time is controlled exclusively by  $t_{CAC}$ .
  4. Operation with the  $t_{RAD}$  (max) limit insures that  $t_{RAC}$  (max) can be met,  $t_{RAD}$  (max) is specified as a reference point only; if  $t_{RAD}$  is greater than the specified  $t_{RAD}$  (max) limit, then access time is controlled exclusively by  $t_{AA}$ .
  5.  $V_{IH}$  (min) and  $V_{IL}$  (max) are reference levels for measuring timing of input signals. Also, transition times are measured between  $V_{IH}$  (min) and  $V_{IL}$  (max).
  6. Assume that  $t_{RCD} \leq t_{RCD}$  (max) and  $t_{RAD} \leq t_{RAD}$  (max). If  $t_{RCD}$  or  $t_{RAD}$  is greater than the maximum recommended value shown in this table,  $t_{RAC}$  exceeds the value shown.
  7. Measured with a load circuit equivalent to 2 TTL loads and 100 pF.
  8. Assume that  $t_{RCD} \geq t_{RCD}$  (max) and  $t_{RAD} \leq t_{RAD}$  (max).
  9. Assume that  $t_{RCD} \leq t_{RCD}$  (max) and  $t_{RAD} \geq t_{RAD}$  (max).
  10. Either  $t_{RCH}$  or  $t_{RRH}$  must be satisfied for a read cycles.
  11.  $t_{OFF}$  (max) and  $t_{OEZ}$  (max) define the time at which the outputs achieve the open circuit condition and are not referred to output voltage levels.
  12.  $t_{WCS}$ ,  $t_{RWD}$ ,  $t_{CWD}$ ,  $t_{AWD}$  and  $t_{CPW}$  are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only; if  $t_{WCS} \geq t_{WCS}$  (min), the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout the entire cycle; if  $t_{RWD} \geq t_{RWD}$  (min),  $t_{CWD} \geq t_{CWD}$  (min), and  $t_{AWD} \geq t_{AWD}$  (min), or  $t_{CWD} \geq t_{CWD}$  (min),  $t_{AWD} \geq t_{AWD}$  (min) and  $t_{CPW} \geq t_{CPW}$  (min), the cycle is a read-modify-write and the data output will contain data read from the selected cell; if neither of the above sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.
  13. These parameters are referenced to  $\overline{CAS}$  leading edge in early write cycles and to  $\overline{WE}$  leading edge in delayed write or read-modify-write cycles.
  14.  $t_{RASP}$  defines  $\overline{RAS}$  pulse width in fast page mode cycles.
  15. Access time is determined by the longest among  $t_{AA}$ ,  $t_{CAC}$  and  $t_{CPA}$ .
  16. The 16M DRAM offers a 16-bit time saving parallel test mode. Address CA0, CA1, CA10 and CA11 for the  $16M \times 1$  are don't care during test mode. Test mode is set by performing a  $\overline{WE}$ -and- $\overline{CAS}$ -before- $\overline{RAS}$  (WCBR) cycle. In 16-bit parallel test mode, data is written into 16 bits in parallel at Din and read out from Dout.  
If 16 bits are equal (all 1s or 0s), data output pin is a high state during test mode read cycle, then the device has passed. If they are not equal, data output pin is a low state, then the device has failed. Refresh during test mode operation can be performed by normal read cycles or by WCBR refresh cycles.  
To get out of test mode and enter a normal operation mode, perform either a regular  $\overline{CAS}$ -before- $\overline{RAS}$  refresh cycle or RAS-only refresh cycle.
  17. In a test mode read cycle, the value of  $t_{RAC}$ ,  $t_{AA}$ ,  $t_{CAC}$  and  $t_{CPA}$  is delayed by 2 ns to 5 ns for the specified value. These parameters should be specified in test mode cycles by adding the above value to the specified value in this data sheet.
  18. XXX: H or L (H:  $V_{IH}$  (min)  $\leq V_{IN} \leq V_{IH}$  (max), L:  $V_{IL}$  (min)  $\leq V_{IN} \leq V_{IL}$  (max))  
/////: Invalid Dout

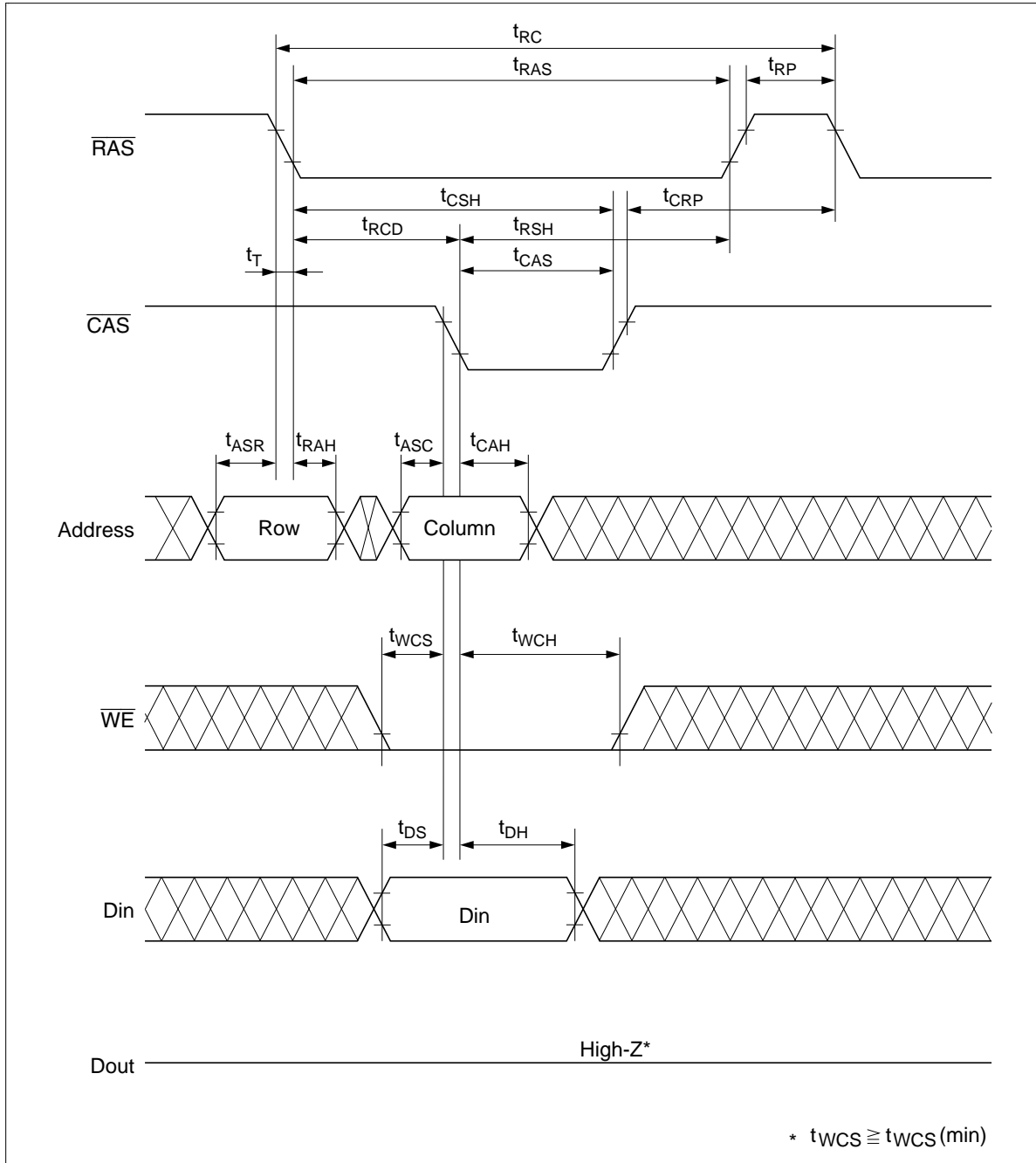
Timing Waveforms\*18

Read Cycle

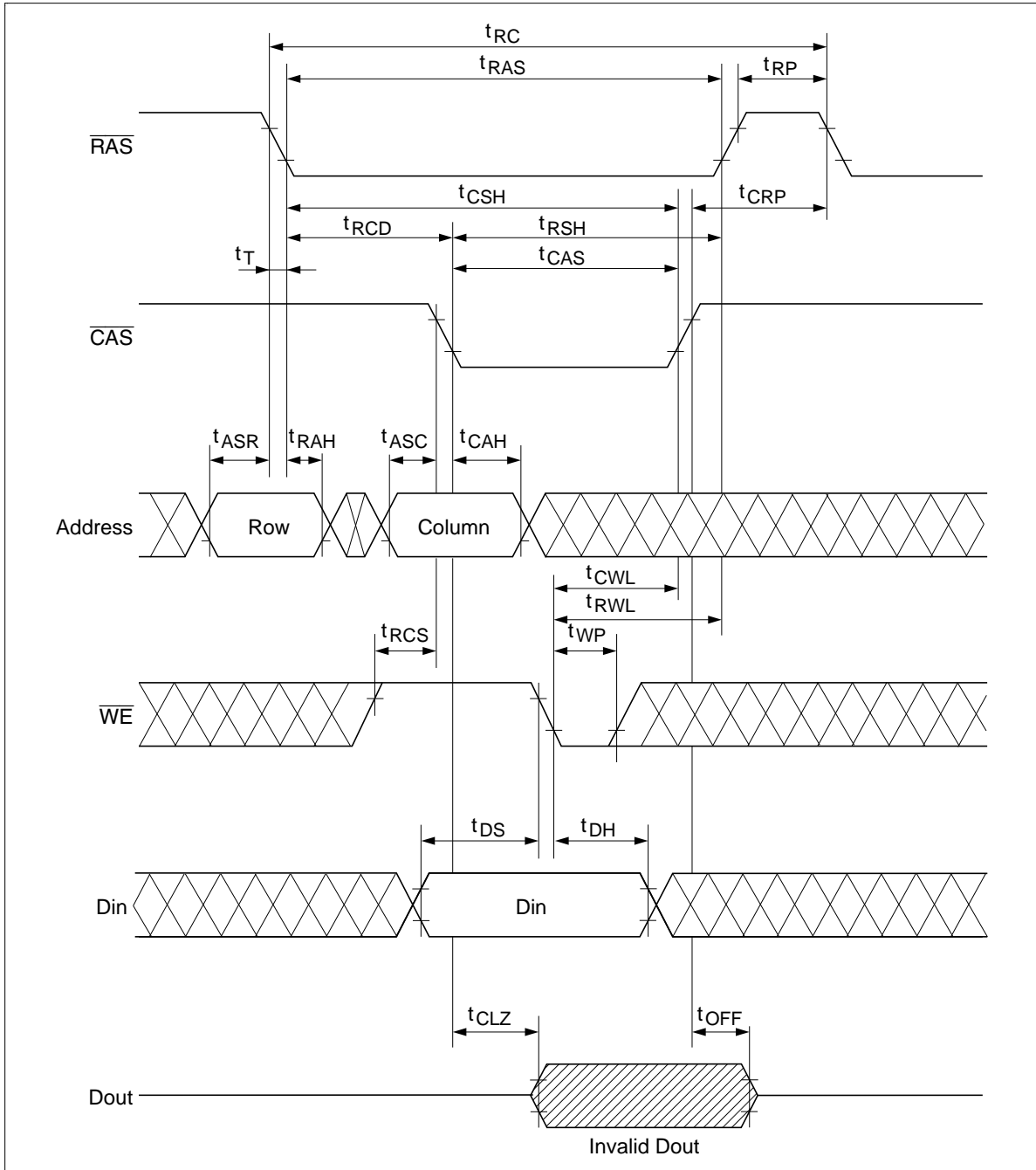


# HM5116100 Series

## Early Write Cycle

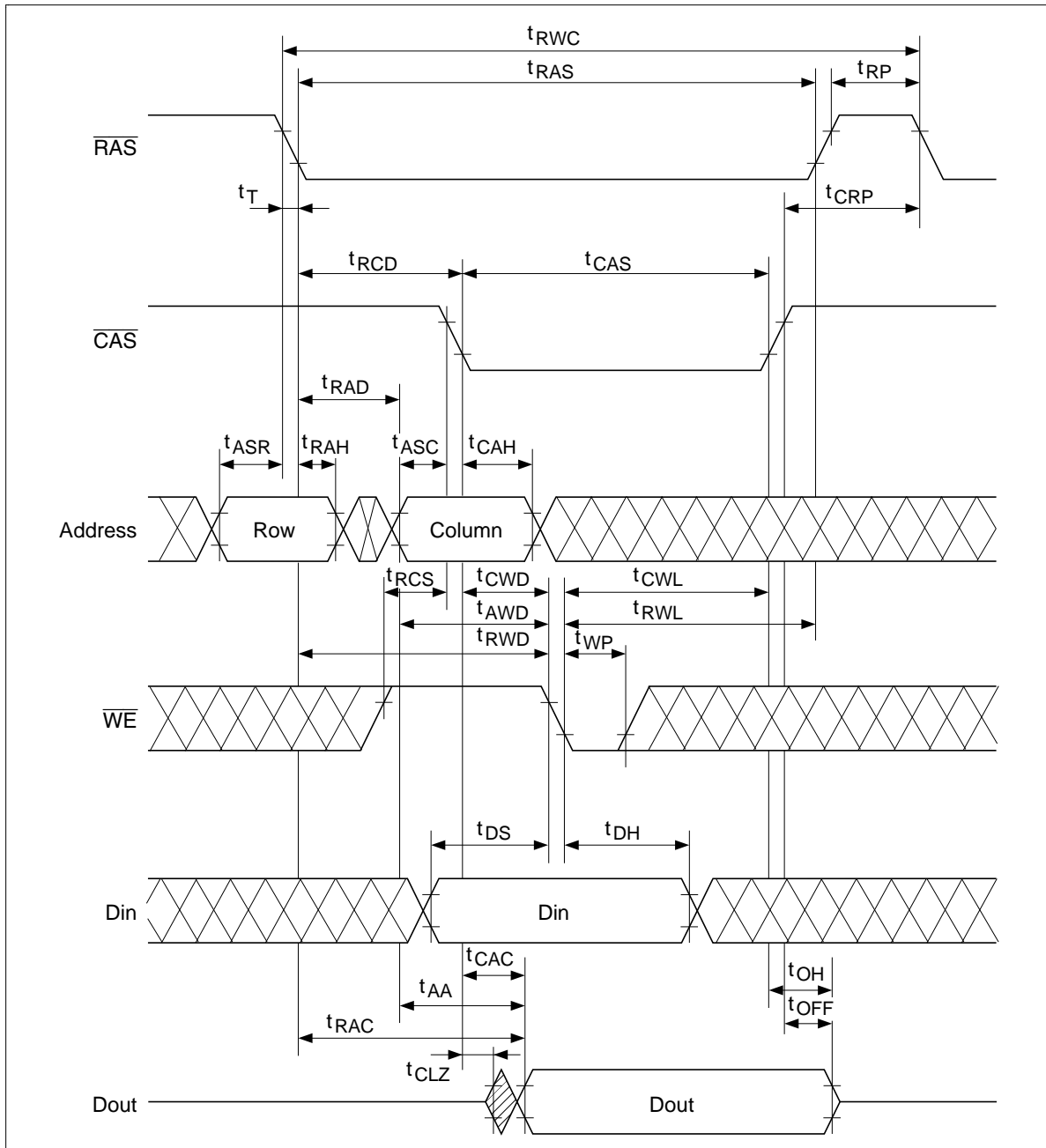


Delayed Write Cycle

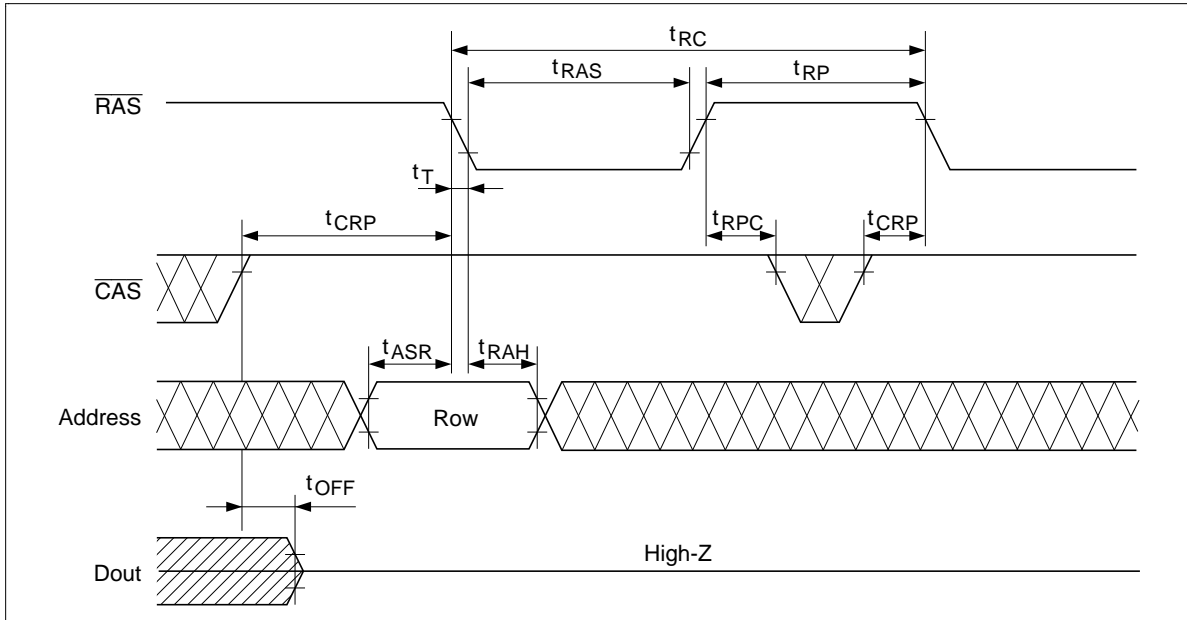


# HM5116100 Series

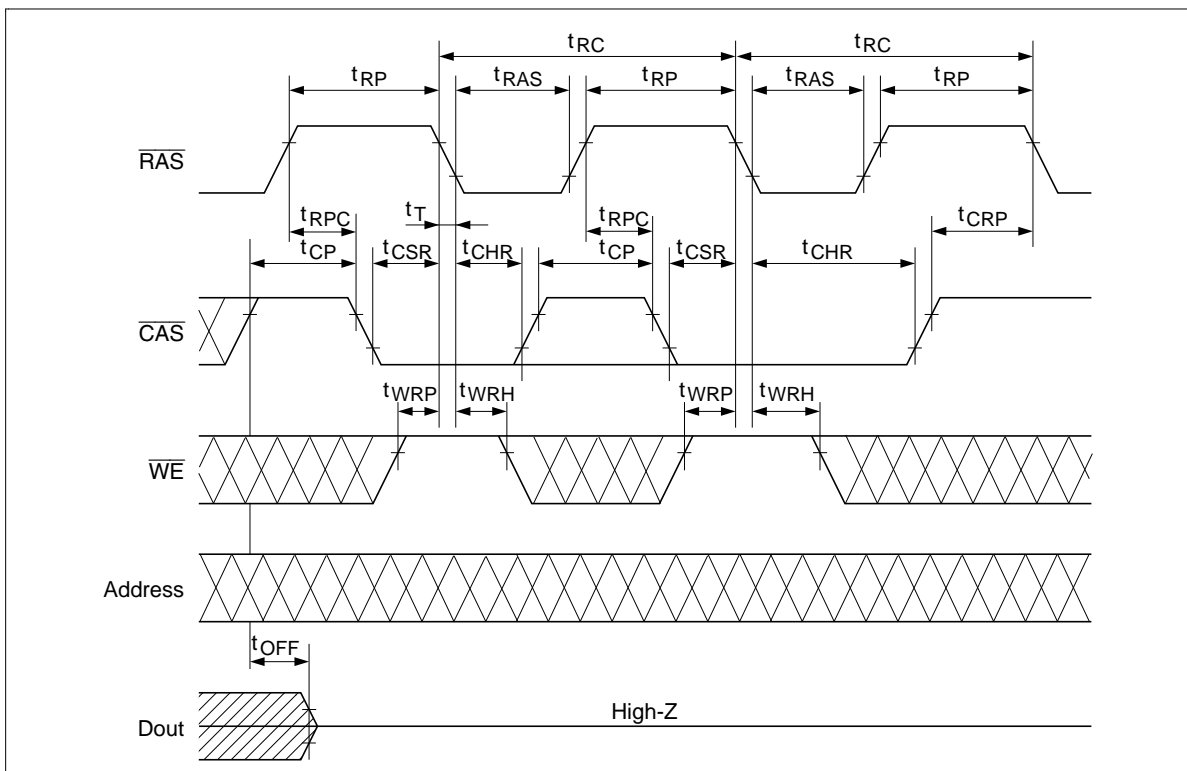
## Read-Modify-Write Cycle



**$\overline{\text{RAS}}$ -Only Refresh Cycle**

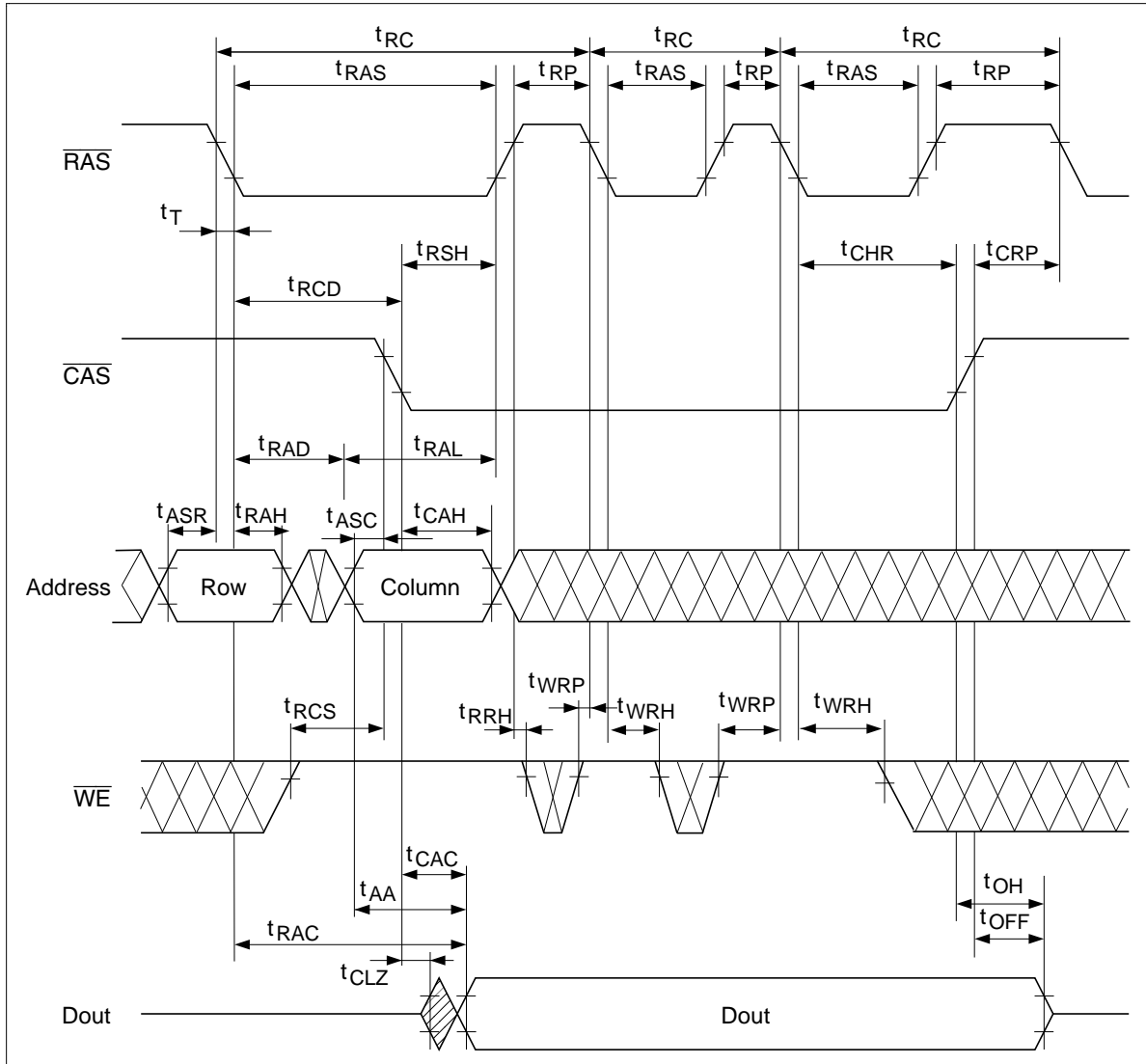


**$\overline{\text{CAS}}$ -Before- $\overline{\text{RAS}}$  Refresh Cycle**



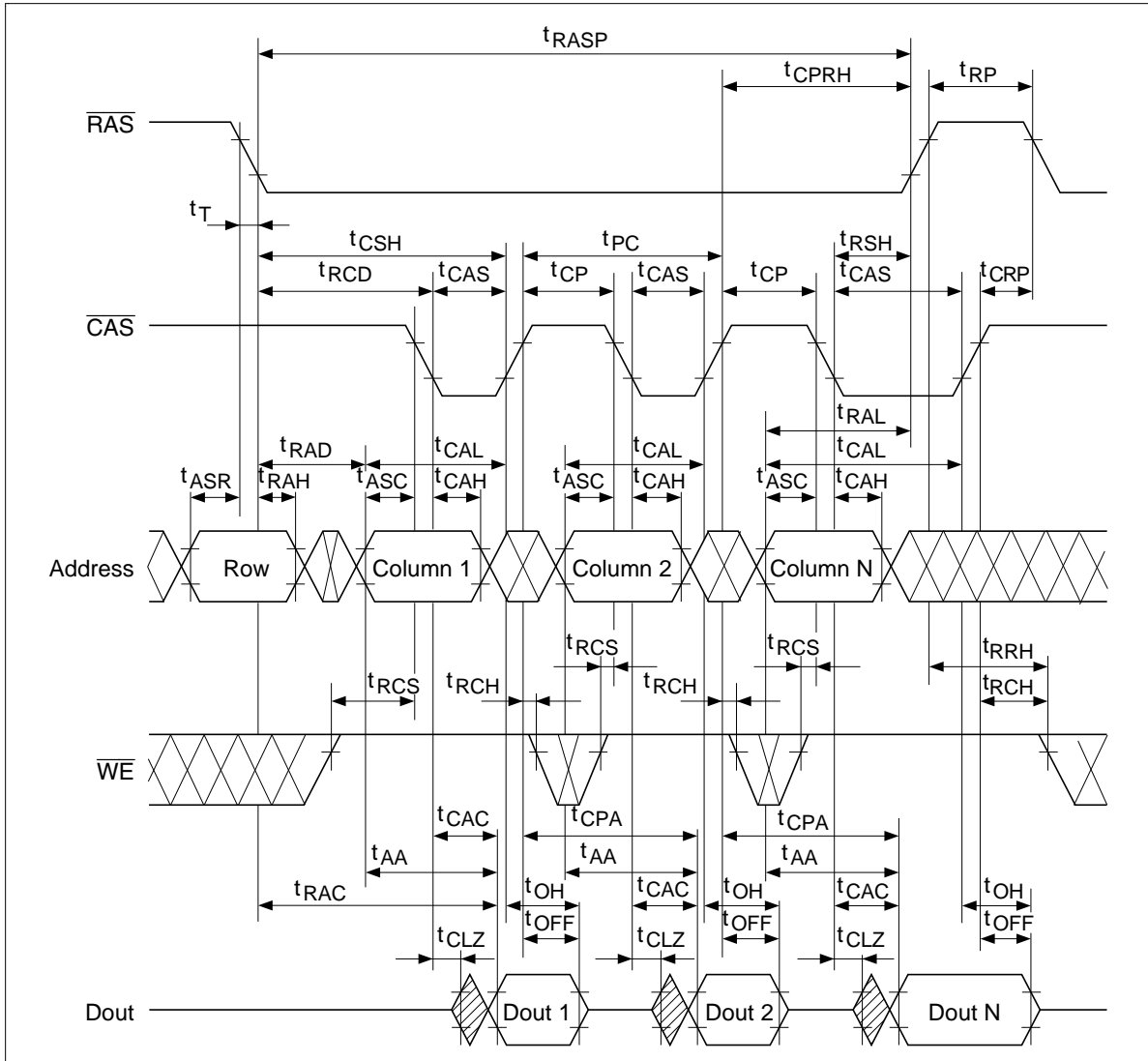
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## Hidden Refresh Cycle



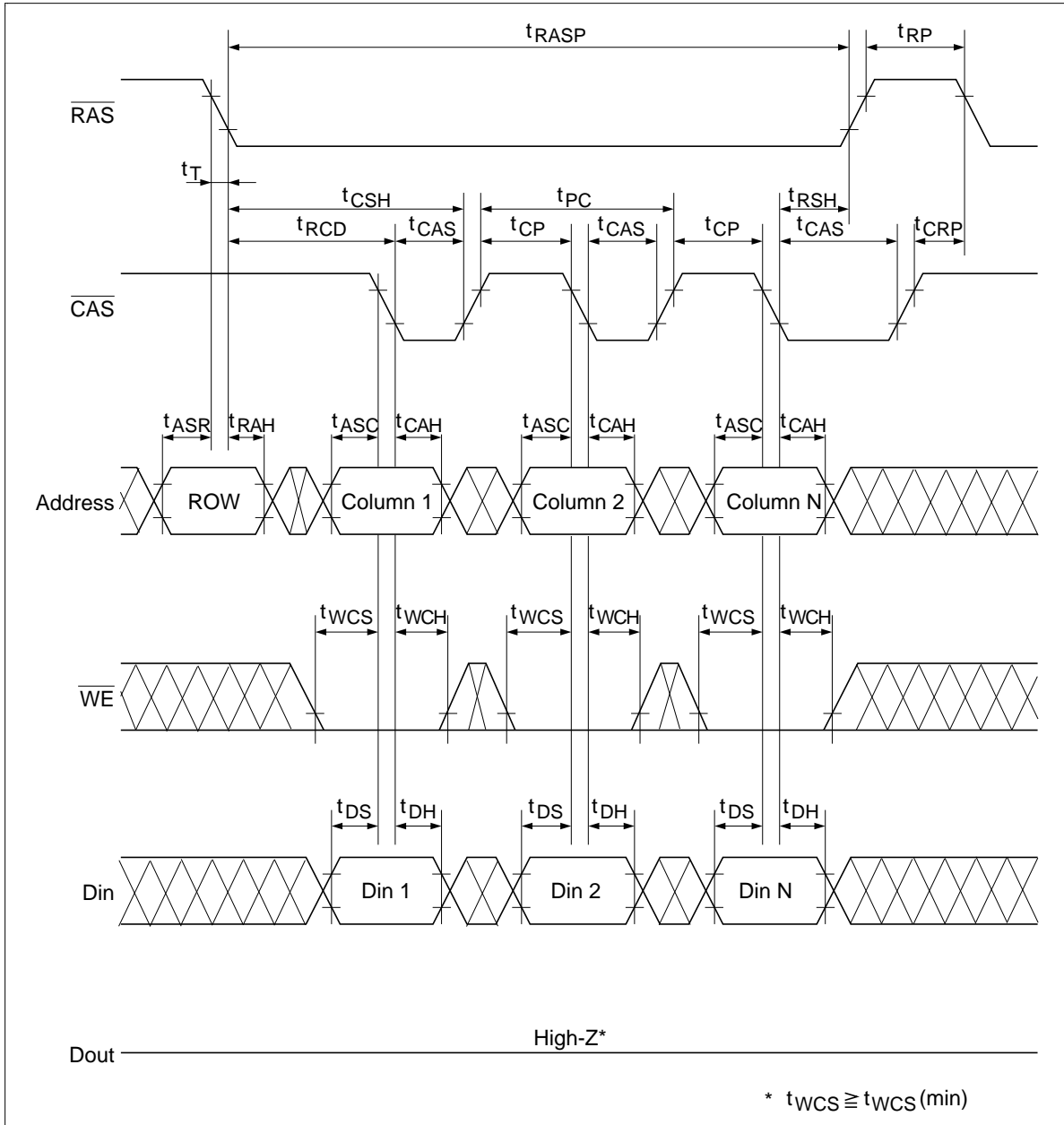


Fast Page Mode Read Cycle

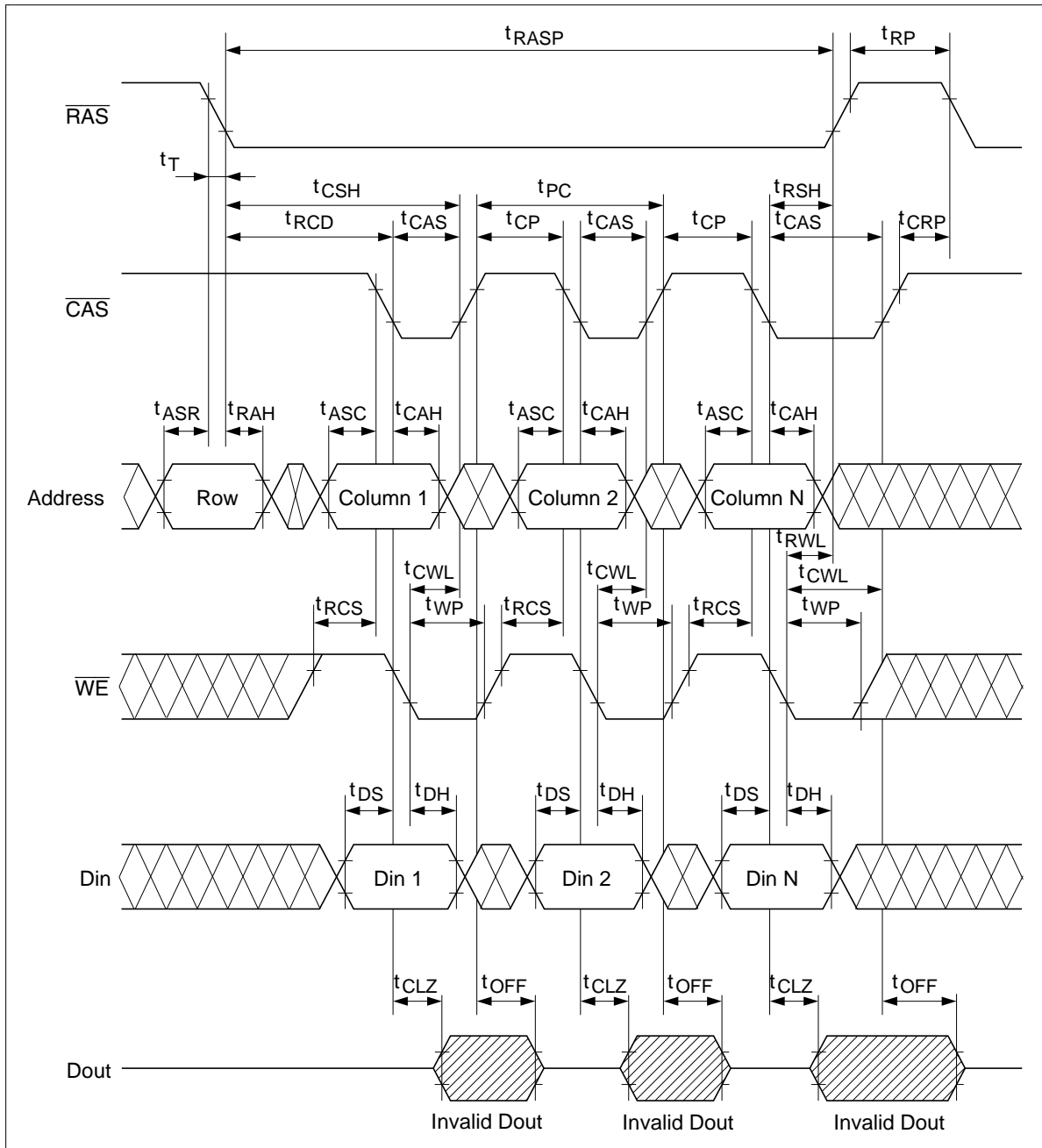


# HM5116100 Series

## Fast Page Mode Early Write Cycle

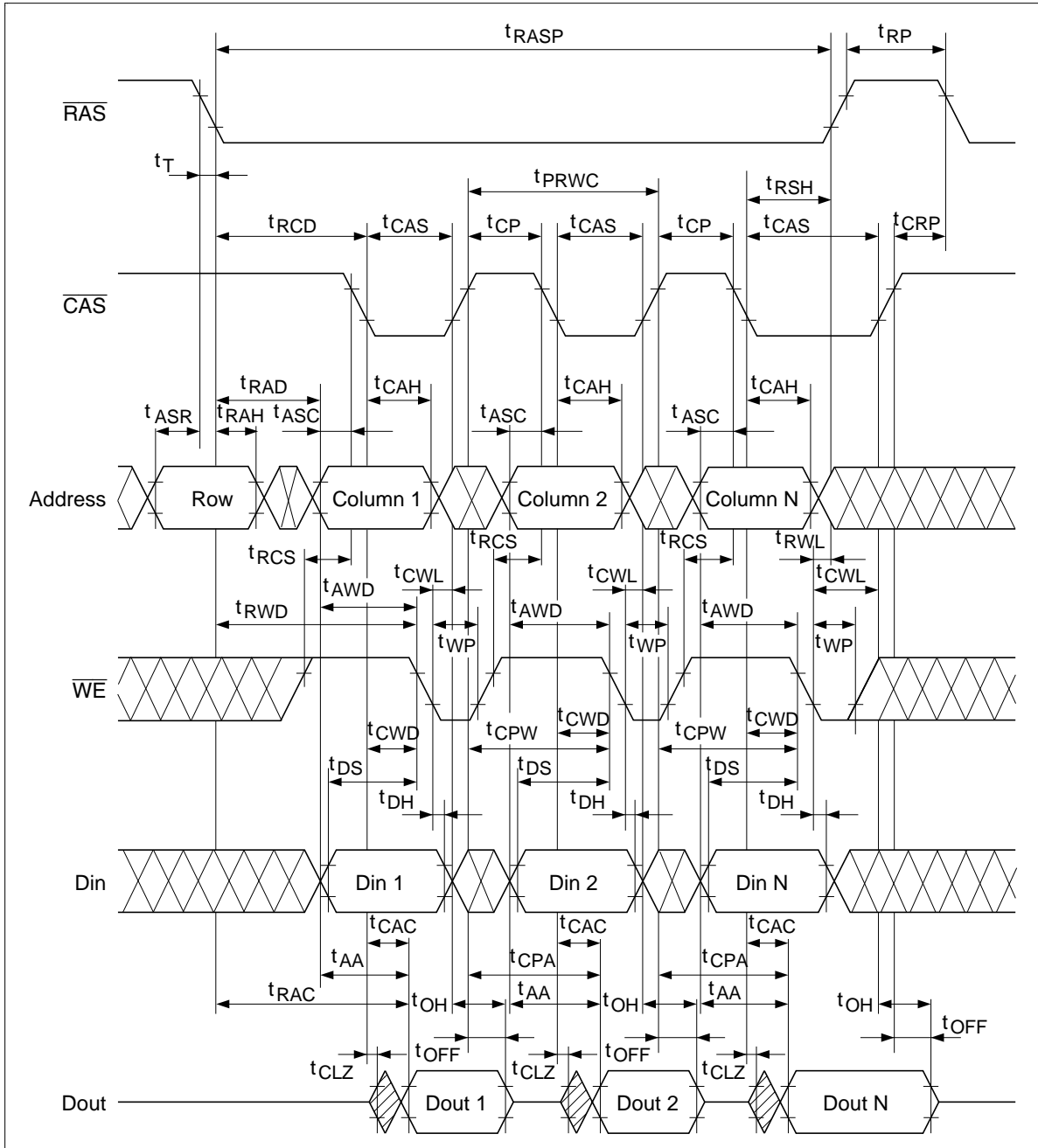


Fast Page Mode Delayed Write Cycle

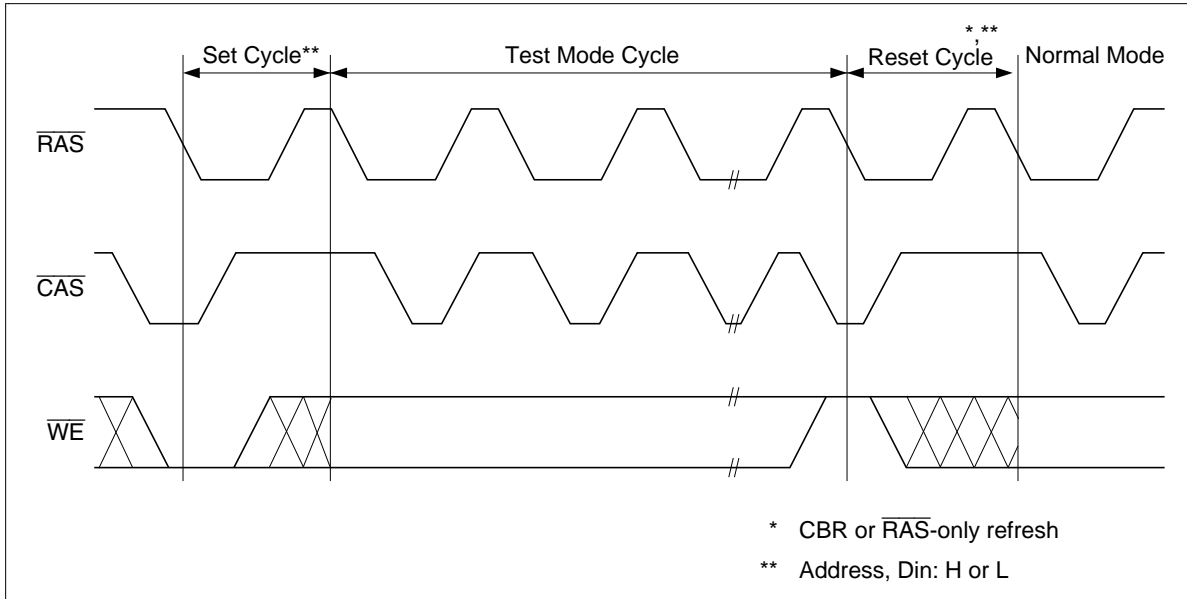


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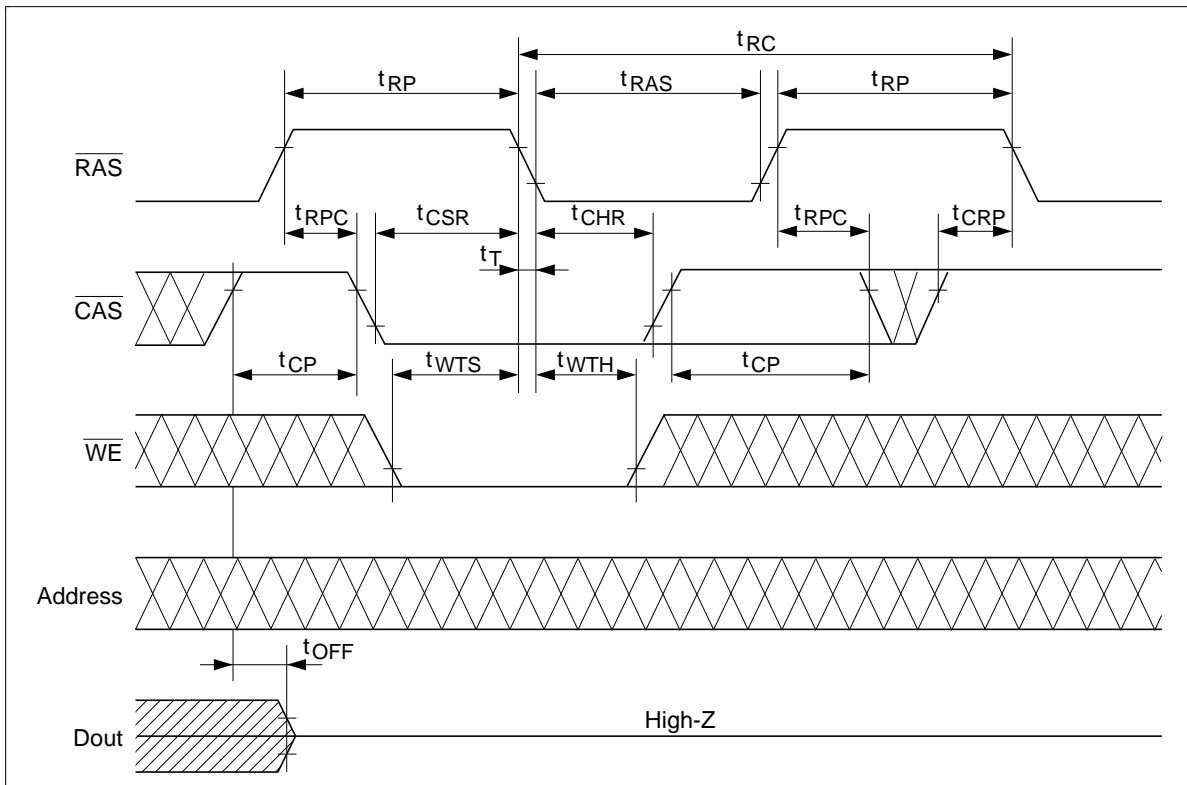
## Fast Page Mode Read-Modify-Write Cycle



Test Mode Cycle\*<sup>16</sup>



Test Mode Set Cycle

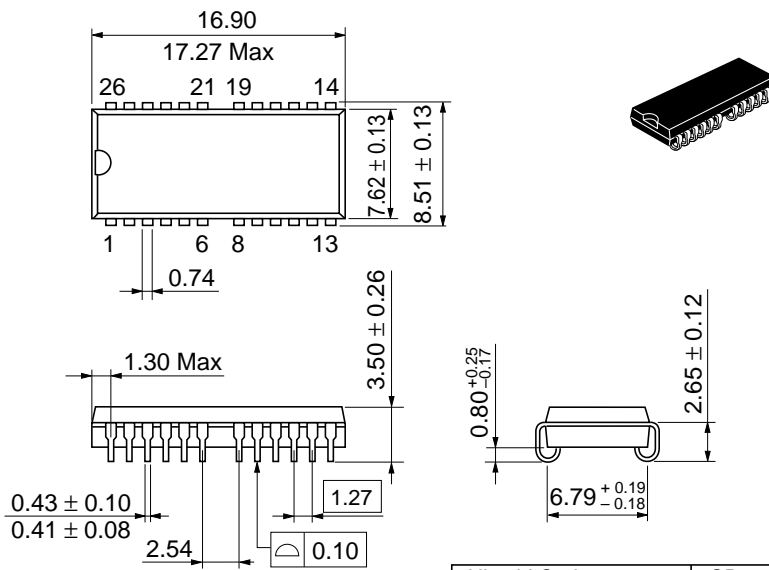


# HM5116100 Series

## Package Dimensions

HM5116100S Series (CP-26/24DB)

Unit: mm



Dimension including the plating thickness  
Base material dimension

Hitachi Code	CP-26/24DB
JEDEC	Conforms
EIAJ	Conforms
Weight (reference value)	0.8 g

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## HM5116100 Series

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### Revision Record

Rev.	Date	Contents of Modification	Drawn by	Approved by
1.0	Oct. 14, 1996	Initial issue	Y. Kasama	M. Mishima
2.0	Dec. 10, 1996	Addition of HM5116100-5 Series	Y. Kasama	Y. Matsuno
3.0	Feb. 27, 1997	AC Characteristics $t_{RRH}$ min: 5/5/5 ns to 0/0/0 ns	Y. Kasama	Y. Matsuno
4.0	Jun. 24, 1997	Deletion of HM5116100-5 Series	Y. Kasama	Y. Matsuno
5.0	Nov. 1997	Change of Subtitle		