

# HM6147H Series

# Maintenance Only

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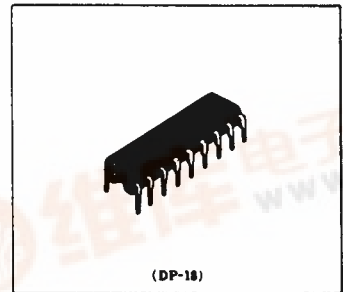
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急出货

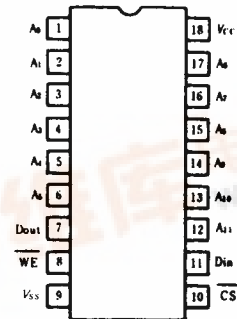
## 4096-word x 1-bit High Speed CMOS Static RAM

### FEATURES

- High Speed: Fast Access Time 35ns/45ns/55ns (max.)
- Low Power Standby and Low Power Operation, Standby: 100 $\mu$ W (typ.)/5 $\mu$ W (typ.) (L-version), Operation: 150mW typ.
- Single 5V Supply and High Density 18 Pin Package
- Completely Static Memory – No Clock nor Timing Strobe Required
- No Peak Power-On Current
- No Change of  $t_{ACS}$  with Short Chip Deselect Time
- Equal Access and Cycle Time
- Directly TTL Compatible – All Input and Output
- Separate Data Input and Output: Three State Output
- Plug-In Replacement with Intel 2147H NMOS STATIC RAM
- Capability of Battery Back Up Operation (L-version)



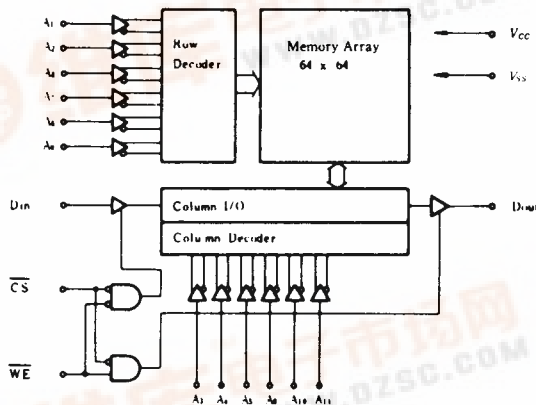
### PIN ARRANGEMENT



### ORDERING INFORMATION

Type No.	Access Time	Package
HM6147HP-35	35ns	300mil 18pin Plastic DIP
HM6147HP-45	45ns	
HM6147HP-55	55ns	
HM6147HLP-35	35ns	300mil 18pin Plastic DIP
HM6147HLP-45	45ns	
HM6147HLP-55	55ns	

### BLOCK DIAGRAM



### ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Rating	Unit
Voltage on Any Pin relative to $V_{SS}$	$V_T$	-0.5 <sup>1</sup> to +7.0	V
DC Output Current	$I_o$	20	mA
Power Dissipation	$P_T$	1.0	W
Operating Temperature	$T_{op}$	0 to +70	°C
Storage Temperature under bias	$T_{stg(bias)}$	-10 to +85	°C
Storage Temperature	$T_{stg}$	-55 to +125	°C

Note1 \*1 -3.5V for pulse width  $\leq$  20ns

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RECOMMENDED DC OPERATING CONDITIONS (0°C ≤ Ta ≤ 70°C)

Parameter	Symbol	min	typ	max	Unit
Supply Voltage	V <sub>CC</sub>	4.5	5.0	5.5	V
	V <sub>SS</sub>	0	0	0	V
Input High (logic 1) Voltage	V <sub>IH</sub>	2.0	3.0	6.0	V
Input Low (logic 0) Voltage	V <sub>IL</sub>	-0.5 <sup>*1</sup>	—	0.8	V

Note) \*1. -3.0V for pulse width ≤ 20ns

DC AND OPERATING CHARACTERISTICS (0°C ≤ Ta ≤ 70°C, V<sub>CC</sub> = 5V ± 10%, V<sub>SS</sub> = 0V)

Parameter	Symbol	Test Condition	min	typ <sup>*2</sup>	max	Unit
Input Leakage Current	I <sub>LI</sub>	V <sub>CC</sub> = 5.5V, V <sub>SS</sub> to V <sub>CC</sub>	—	—	10	μA
Output Leakage Current	I <sub>LO</sub>	$\overline{CS} = V_{IH}$ , V <sub>OH</sub> = V <sub>SS</sub> to V <sub>CC</sub>	—	—	10	μA
Operating Power Supply Current(1)	I <sub>CC</sub>	$\overline{CS} = V_{IL}$ , Output open	—	30	80	mA
Operating Power Supply Current(2)	I <sub>CC1</sub>	$\overline{CS} = V_{IL}$ , Minimum Cycle	—	40	80	mA
Standby Power Supply Current (1)	I <sub>SB</sub>	$\overline{CS} = V_{IH}$ , V <sub>CC</sub> = Min to Max	—	8	20	mA
			—	5 <sup>*3</sup>	15 <sup>*3</sup>	
Standby Power Supply Current (2)	I <sub>SB1</sub>	$\overline{CS} \geq V_{CC} - 0.2V$ , V <sub>IH</sub> ≥ 0.2V or V <sub>IH</sub> ≥ V <sub>CC</sub> - 0.2V	—	20	800	μA
			—	1 <sup>*3</sup>	100 <sup>*3</sup>	
Output Low Voltage	V <sub>OL</sub>	I <sub>OL</sub> = 8mA	—	—	0.40	V
Output High Voltage	V <sub>OH</sub>	I <sub>OH</sub> = -4mA	2.4	—	—	V

Notes) \*1. The operating ambient temperature range is guaranteed with transverse air flow exceeding 400 linear feet minute.

\*2. Typical limits are at V<sub>CC</sub> = 5.0V, Ta = 25°C and Specified loading.

\*3. This characteristics are guaranteed only for L-version.

CAPACITANCE (Ta = 25°C, f = 1.0MHz)

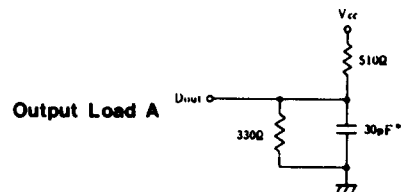
Item	Symbol	Conditions	max	Unit
Input Capacitance	C <sub>i</sub>	V <sub>i</sub> = 0V	5	pF
Output Capacitance	C <sub>o</sub>	V <sub>o</sub> = 0V	6	pF

Note) This parameter is sampled and not 100% tested.

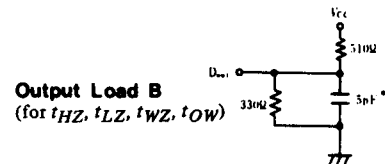
AC CHARACTERISTICS (Ta = 0 to +70°C, V<sub>CC</sub> = 5V ± 10%)

AC TEST CONDITIONS

- Input pulse levels: V<sub>SS</sub> to 3.0V
- Input rise and fall times: 5 ns
- Input timing reference levels: 1.5V
- Output load: See Figure
- Output timing reference levels: 1.5V (HM6147H-35)  
0.8 to 2.0V (HM6147H-45/55)



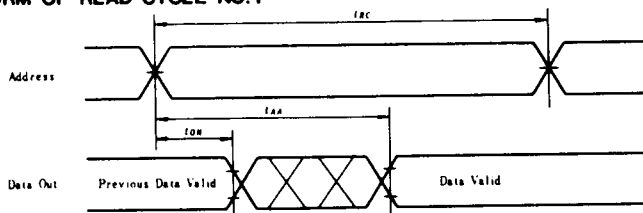
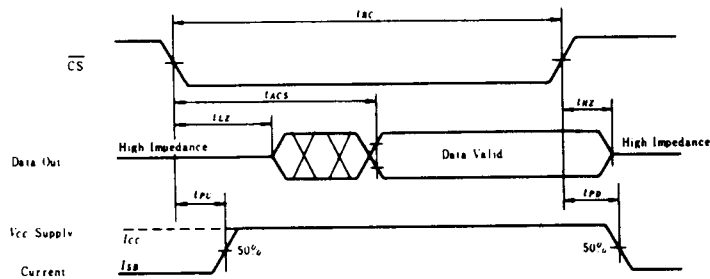
\* Including scope & jig capacitance



Output Load B  
(for t<sub>HZ</sub>, t<sub>LZ</sub>, t<sub>WZ</sub>, t<sub>OW</sub>)

## ● READ CYCLE

Parameter	Symbol	HM6147H-35		HM6147H-45		HM6147H-55		Unit	Notes
		min	max	min	max	min	max		
Read Cycle Time	$t_{RC}$	35	—	45	—	55	—	ns	(1)
Address Access Time	$t_{AA}$	—	35	—	45	—	55	ns	
Chip Select Access Time	$t_{ACS}$	—	35	—	45	—	55	ns	
Output Hold from Address Change	$t_{OH}$	5	—	5	—	5	—	ns	
Chip Selection to Output in Low Z	$t_{LZ}$	5	—	5	—	5	—	ns	(2), (3), (7)
Chip Deselection to Output in High Z	$t_{HZ}$	0	30	0	30	0	30	ns	(2), (3), (7)
Chip Selection to Power Up Time	$t_{PU}$	0	—	0	—	0	—	ns	
Chip Deselection to Power Down Time	$t_{PD}$	—	20	—	20	—	20	ns	

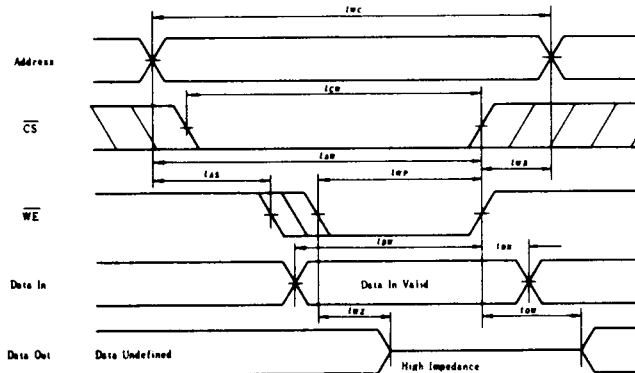
● TIMING WAVEFORM OF READ CYCLE NO.1 <sup>(4)(5)</sup>● TIMING WAVEFORM OF READ CYCLE NO.2 <sup>(4)(6)</sup>

- Notes:
1. All Read Cycle timings are referenced from last valid address to the first transitioning address.
  2. At any given temperature and voltage condition,  $t_{HZ}$  max. is less than  $t_{LZ}$  min. both for a given device and from device to device.
  3. Transition is measured  $\pm 500$ mV from steady state voltage with specified loading in Load B.
  4.  $\overline{WE}$  is high for READ Cycle.
  5. Device is continuously selected,  $\overline{CS}=V_{IL}$ .
  6. Addresses valid prior to or coincident with  $\overline{CS}$  transition low.
  7. This parameter is sampled and not 100% tested.

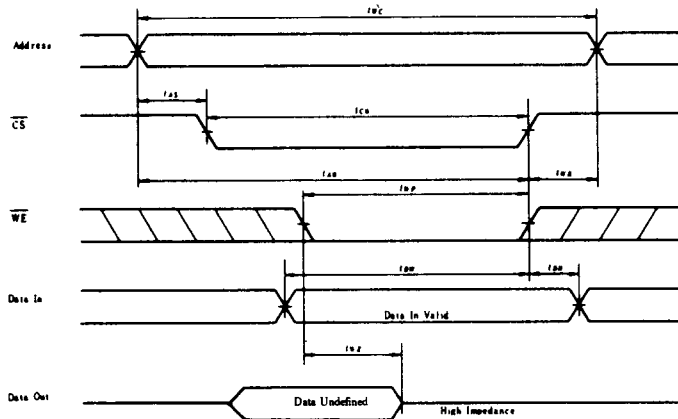
● WRITE CYCLE

Parameter	Symbol	HM6147H-35		HM6147H-45		HM6147H-55		Unit	Notes
		min	max	min	max	min	max		
Write Cycle Time	$t_{wc}$	35	—	45	—	55	—	ns	(2)
Chip Selection to End of Write	$t_{cw}$	35	—	45	—	45	—	ns	
Address Valid to End of Write	$t_{aw}$	35	—	45	—	45	—	ns	
Address Setup Time	$t_{as}$	0	—	0	—	0	—	ns	
Write Pulse Width	$t_{wp}$	20	—	25	—	30	—	ns	
Write Recovery Time	$t_{wr}$	0	—	0	—	0	—	ns	
Data Valid to End of Write	$t_{dw}$	20	—	25	—	25	—	ns	
Data Hold Time	$t_{dh}$	10	—	10	—	10	—	ns	
Write Enabled to Output in High Z	$t_{wz}$	0	20	0	25	0	30	ns	(3), (4)
Output Active from End of Write	$t_{ow}$	0	—	0	—	0	—	ns	(3), (4)

● TIMING WAVEFORM OF WRITE CYCLE ( $\overline{WE}$  Controlled)



● TIMING WAVEFORM OF WRITE CYCLE ( $\overline{CS}$  Controlled)



- Notes:
1. If  $\overline{CS}$  goes high simultaneously with  $\overline{WE}$  high, the output remains in a high impedance states.
  2. All Write Cycle timings are referenced from the last valid address to the first transitioning address.
  3. Transition is measured  $\pm 500mV$  from steady state voltage with specified loading in Load B.
  4. This parameter is sampled and not 100% tested.
  5.  $\overline{CS}$  or  $\overline{WE}$  is high for address transition.

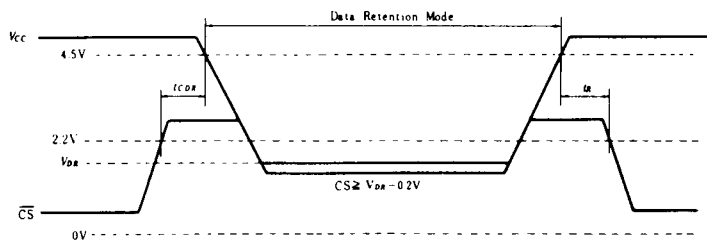
**LOW  $V_{CC}$  DATA RETENTION CHARACTERISTICS ( $T_a=0^\circ\text{C}$  to  $+70^\circ\text{C}$ )**

This characteristics are guaranteed only for L-version.

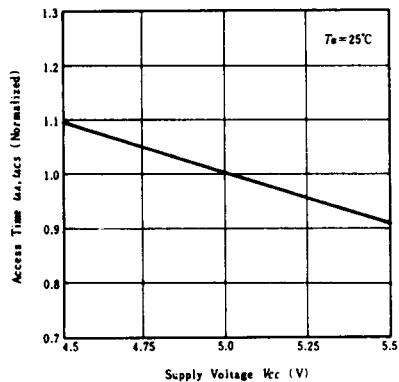
Item	Symbol	Test Condition	min	typ	max	Unit
$V_{CC}$ for Data Retention	$V_{DR}$	$\overline{CS} \geq V_{CC} - 0.2\text{V}$ $V_{IN} \geq V_{LC} - 0.2\text{V}$ or $V_{IN} \leq 0.2\text{V}$	2.0	—	—	V
Data Retention Current	$I_{CCDR}$	$V_{CC} = 3.0\text{V}$ , $\overline{CS} \geq 2.8\text{V}$ $V_{IN} \geq 2.8\text{V}$ or $V_{IN} \leq 0.2\text{V}$	—	—	50	$\mu\text{A}$
Chip Deselect to Data Retention Time	$t_{CDR}$	See Retention Waveform	0	—	—	ns
Operation Recovery Time	$t_R$		$t_{AC}^{*1}$	—	—	ns

Note) \*1.  $t_{AC}$  = Red Cycle Time.

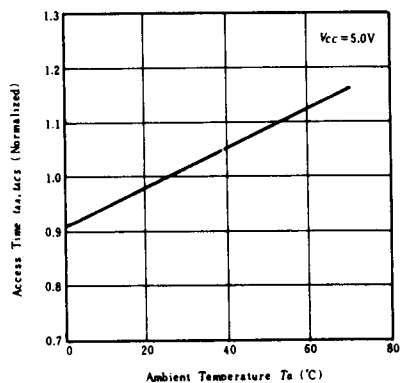
**LOW  $V_{CC}$  DATA RETENTION WAVEFORM**



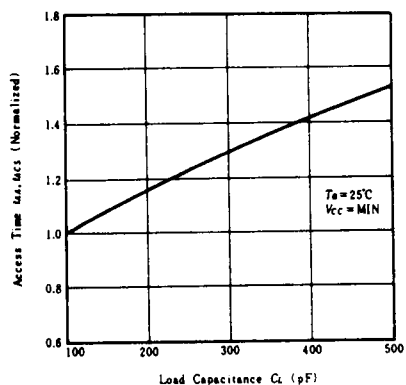
ACCESS TIME VS. SUPPLY VOLTAGE



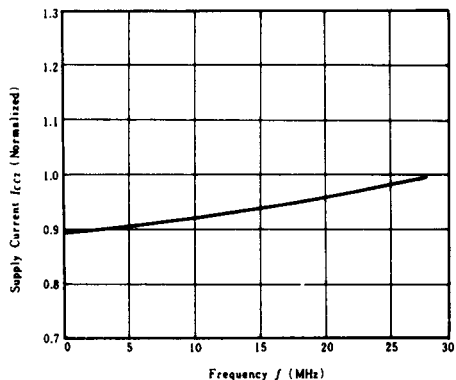
ACCESS TIME VS. AMBIENT TEMPERATURE



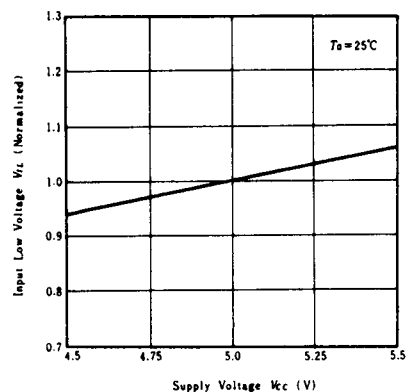
ACCESS TIME VS. LOAD CAPACITANCE



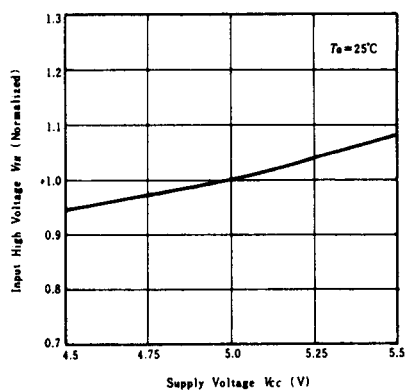
SUPPLY CURRENT VS. FREQUENCY



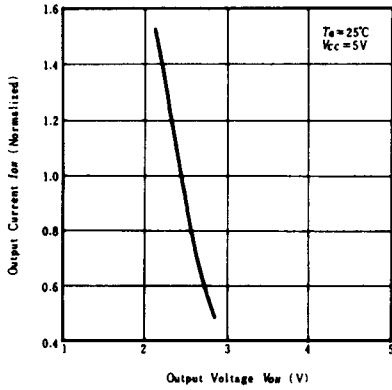
INPUT LOW VOLTAGE VS. SUPPLY VOLTAGE



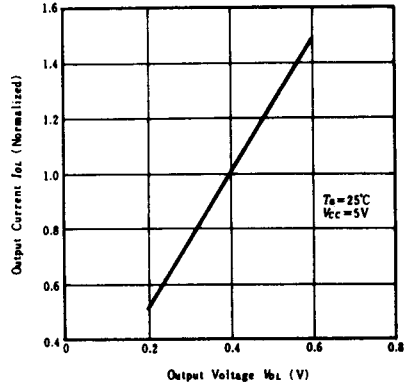
INPUT HIGH VOLTAGE VS. SUPPLY VOLTAGE



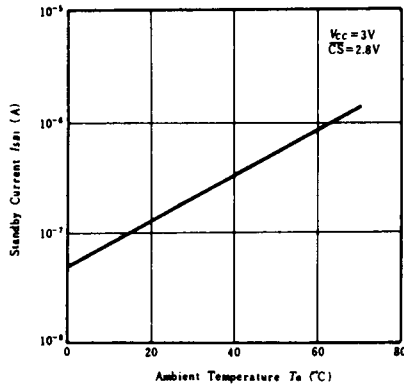
OUTPUT CURRENT VS. OUTPUT VOLTAGE



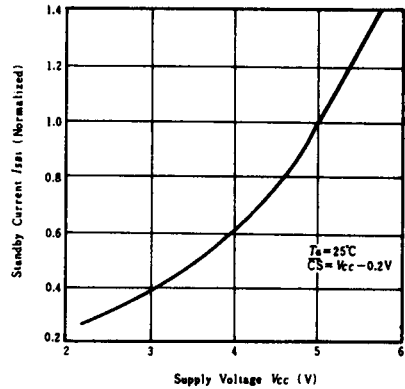
OUTPUT CURRENT VS. OUTPUT VOLTAGE



STANDBY CURRENT VS. AMBIENT TEMPERATURE



STANDBY CURRENT VS. SUPPLY VOLTAGE



STANDBY CURRENT VS. INPUT VOLTAGE

