

# HM6148HLP Series

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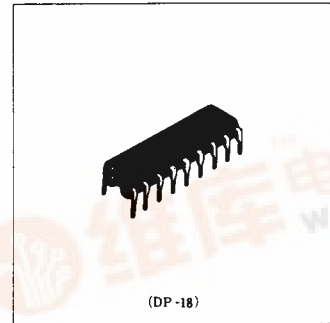
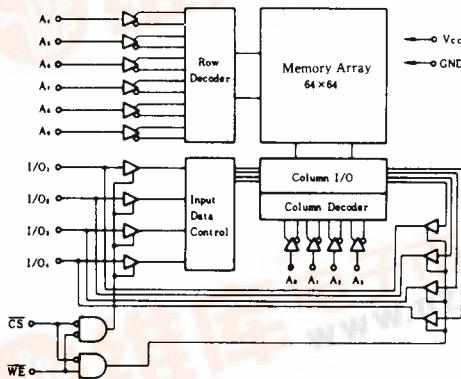
急出货

## 1024-word × 4-bit High Speed Static CMOS RAM

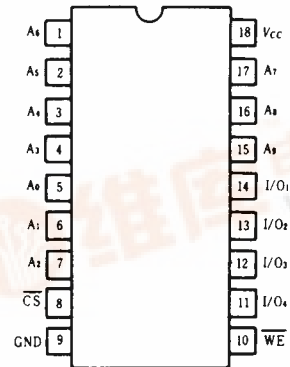
### FEATURES

- Low Power Standby and Low Power Operation; Standby: 5μW (typ.), Operation: 175mW (typ.)
- Fast Access Time: 45/55ns (max)
- Capability of Battery Back Up Operation
- Single 5V Supply
- Completely Static RAM: No Clock or Timing Strobe Required
- No Peak Power-On Current
- No Change of  $t_{ACS}$  with Short Deselected Time
- Equal Access and Cycle Time
- Directly TTL Compatible: All Inputs and Outputs
- Three State Output
- Pin-Out Compatible with Intel 2148H

### BLOCK DIAGRAM



### PIN ARRANGEMENT



(Top View)

### ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Ratings	Unit
Terminal Voltage*	$V_T$	-0.5 to +7.0	V
Power Dissipation	$P_T$	1.0	W
Operating Temperature	$T_{op}$	0 to +70	°C
Storage Temperature	$T_{stg}$	-55 to +125	°C
Storage Temperature**	$T_{1..}$	-10 to +85	°C

\* with respect to GND.  $V_{CC} \dots -3.5V$  (Pulse width = 20ns)

\*\* under bias.

### TRUTH TABLE

CS	WE	Mode	$V_{CC}$ Current	I/O Pin	Reference Cycle
H	X	Not selected	$I_{sa}, I_{sb1}$	High Z	
L	H	Read	$I_{cc}$	Dout	Read Cycle 1, 2
L	L	Write	$I_{cc}$	Din	Write Cycle 1, 2



■ RECOMMENDED DC OPERATING CONDITIONS ( $T_a=0$  to  $+70^\circ\text{C}$ )

Item	Symbol	min	typ	max	Unit
Supply Voltage	$V_{CC}$	4.5	5.0	5.5	V
	GND	0	0	0	V
Input Voltage	$V_{IH}$	2.2	—	6.0	V
	$V_{IL}$	-0.5*	—	0.8	V

\* -3.0V (Pulse width 20ns)

■ DC AND OPERATING CHARACTERISTICS ( $T_a=0$  to  $+70^\circ\text{C}$ ,  $V_{CC}=5V \pm 10\%$ ,  $GND=0V$ )

Parameter	Symbol	Test Conditions	min	typ*	max	Unit
Input Leakage Current	$ I_{LI} $	$V_{CC}=\text{max}$ , $V_{in}=\text{GND to } V_{CC}$	—	—	2.0	$\mu\text{A}$
Output Leakage Current	$ I_{LO} $	$\overline{\text{CS}}=V_{IH}$ , $V_{I/O}=\text{GND to } V_{CC}$	—	—	2.0	$\mu\text{A}$
Operating Power Supply Current (1)	$I_{CC}$	$\overline{\text{CS}}=V_{IL}$ , $I_{I/O}=0\text{mA}$	—	35	80	mA
Operating Power Supply Current (2)	$I_{CC1}$	min. cycle, $\overline{\text{CS}}=V_{IL}$ , $I_{I/O}=0\text{mA}$	—	50	100	mA
Standby Power Supply Current (1)	$I_{SB}$	$\overline{\text{CS}}=V_{IH}$	—	5	20	mA
Standby Power Supply Current (2)	$I_{SB1}$	$\overline{\text{CS}} \geq V_{CC}-0.2\text{V}$ , $V_{IN} \leq 0.2\text{V}$ or $V_{IN} \geq V_{CC}-0.2\text{V}$	—	1	50	$\mu\text{A}$
Output Low Voltage	$V_{OL}$	$I_{OL}=8\text{mA}$	—	—	0.4	V
Output High Voltage	$V_{OH}$	$I_{OH}=-4.0\text{mA}$	2.4	—	—	V

\* Typical limits are at  $V_{CC}=5.0\text{V}$ ,  $T_a=+25^\circ\text{C}$  and specified loading.

■ CAPACITANCE ( $T_a=25^\circ\text{C}$ ,  $f=1\text{MHz}$ )

Item	Symbol	Test Conditions	typ	max	Unit
Input Capacitance	$C_{in}$	$V_{in}=0\text{V}$	—	5	pF
Input/Output Capacitance	$C_{I/O}$	$V_{I/O}=0\text{V}$	—	7	pF

Note) This parameter is sampled and not 100% tested.

■ AC CHARACTERISTICS ( $V_{CC}=5V \pm 10\%$ ,  $T_a=0$  to  $+70^\circ\text{C}$ )

● RISE/FALL TIME

Item	Symbol	min	typ	max	Unit
Input Rise Time	$t_r$	—	5	100	ns
Input Fall Time	$t_f$	—	5	100	ns

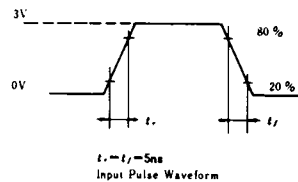
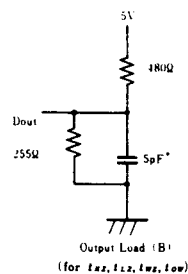
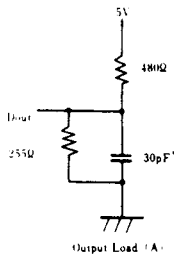
● AC TEST CONDITIONS

Input pulse levels: GND to 3.0V

Input rise and fall times: 5ns

Input and Output timing reference levels: 1.5V

Output load: See Figure



\* Including scope & jig.

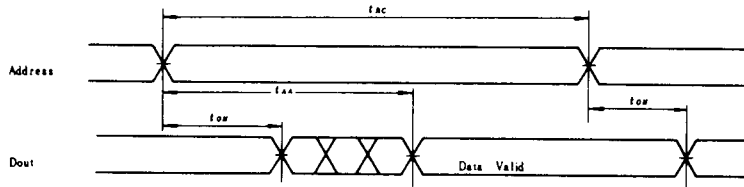
■ AC CHARACTERISTICS ( $T_a=0$  to  $+70^\circ\text{C}$ ,  $V_{cc}=5\text{V}\pm 10\%$ , unless otherwise noted.)

● READ CYCLE

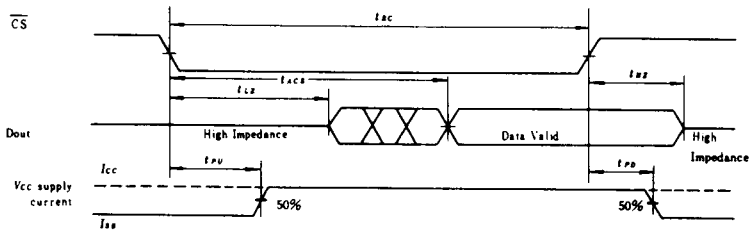
Item	Symbol	HM6148HLP-45		HM6148HLP-55		Unit
		min	max	min	max	
Read Cycle Time	$t_{RC}$	45	—	55	—	ns
Address Access Time	$t_{AA}$	—	45	—	55	ns
Chip Select Access Time	$t_{ACS}$	—	45	—	55	ns
Output Hold from Address Change	$t_{OH}$	5	—	5	—	ns
Chip Selection to Output in Low Z	$t_{LZ}^*$	10	—	10	—	ns
Chip Deselection to Output in High Z	$t_{HZ}^*$	0	20	0	20	ns
Chip Selection to Power Up Time	$t_{PU}$	0	—	0	—	ns
Chip Deselection to Power Down Time	$t_{PD}$	—	30	—	30	ns

\* Transition is measured  $\pm 500\text{mV}$  from steady state voltage with Load(B). This parameter is sampled and not 100% tested.  
At any temperature and voltage condition  $t_{LZ}$  max is less than  $t_{LZ}$  min.

● TIMING WAVEFORM OF READ CYCLE NO.1 <sup>(1)(2)</sup>



● TIMING WAVEFORM OF READ CYCLE NO.2 <sup>(1)(3)</sup>



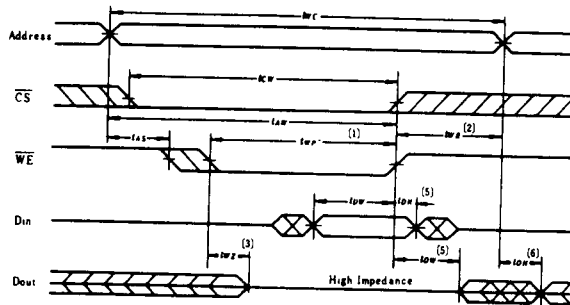
- Notes) 1.  $\overline{WE}$  is High for Read Cycle.  
2. Device is continuously selected,  $\overline{CS} = V_{IL}$ .  
3. Address Valid prior to or coincident with  $\overline{CS}$  transition Low.

● WRITE CYCLE

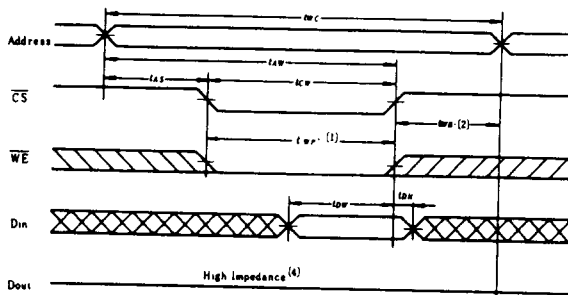
Item	Symbol	HM6148HLP-45		HM6148HLP-55		Unit
		min	max	min	max	
Write Cycle Time	$t_{wc}$	45	—	55	—	ns
Chip Selection to End of Write	$t_{cw}$	40	—	50	—	ns
Address Valid to End of Write	$t_{aw}$	40	—	50	—	ns
Address Setup Time	$t_{as}$	0	—	0	—	ns
Write Pulse Width	$t_{wp}$	35	—	40	—	ns
Write Recovery Time	$t_{wr}$	5	—	5	—	ns
Data Valid to End of Write	$t_{dw}$	20	—	20	—	ns
Data Hold Time	$t_{dh}$	0	—	0	—	ns
Write Enabled to Output in High Z*	$t_{wz}$	0	15	0	20	ns
Output Active from End of Write*	$t_{ow}$	0	—	0	—	ns

\* Transition is measured  $\pm 500$ mV from steady state voltage with Load B.  
This parameter is sampled and not 100% tested.

● TIMING WAVEFORM OF WRITE CYCLE NO.1 ( $\overline{WE}$  Controlled)



● TIMING WAVEFORM OF WRITE CYCLE NO.2 ( $\overline{CS}$  Controlled)



Notes of Timing Waveform of Write :

1. A write occurs during the overlap of a low  $\overline{CS}$  and a low  $\overline{WE}$ . ( $t_{wp}$ )
2.  $t_{aw}$  is measured from the earlier of  $\overline{CS}$  or  $\overline{WE}$  going high to the end of write cycle.
3. During this period, I/O pins are in the output state so that the input signals of opposite phase to the outputs must not be applied.
4. If the  $\overline{CS}$  low transition occurs simultaneously with the  $\overline{WE}$  low transition or after the  $\overline{WE}$  transition, the output buffers remain in a high impedance state.
5. If  $\overline{CS}$  is low during this period, I/O pins are in the output state. Then the data input signals of opposite phase to the outputs must not be applied to them.
6.  $t_{ow}$  is the same phase of write data of this write cycle.

■ LOW  $V_{CC}$  DATA RETENTION CHARACTERISTICS ( $0^{\circ}\text{C} \leq T_a \leq 70^{\circ}\text{C}$ )

Parameter	Symbol	Test Conditions	min	typ	max	Unit
$V_{CC}$ for Data Retention	$V_{DR}$	$\overline{CS} \geq V_{CC} - 0.2\text{V}$ $V_{i1} \geq V_{CC} - 0.2\text{V}$ or $0\text{V} \leq V_{i1} \leq 0.2\text{V}$	2.0	—	—	V
Data Retention Current	$I_{CCDR}$		—	—	30* 20**	$\mu\text{A}$
Chip Deselect to Data Retention Time	$t_{CDR}$		0	—	—	ns
Operation Recovery Time	$t_R$		$t_{AC(1)}$	—	—	ns

Note) 1.  $t_{AC}$ —Read Cycle Time.

- \*  $V_{CC} = 3.0\text{V}$
- \*\*  $V_{CC} = 2.0\text{V}$

● LOW  $V_{CC}$  DATA RETENTION WAVEFORM

