HMC322

GaAs MMIC SP8T NON-REFLECTIVE SWITCH, DC - 10.0 GHz

Typical Applications

The HMC322 is ideal for:

- Telecom Infrastructure
- Microwave Radio & VSAT
- Military & Space
- Test Instrumentation

Features

Broadband Performance: DC - 10.0 GHz

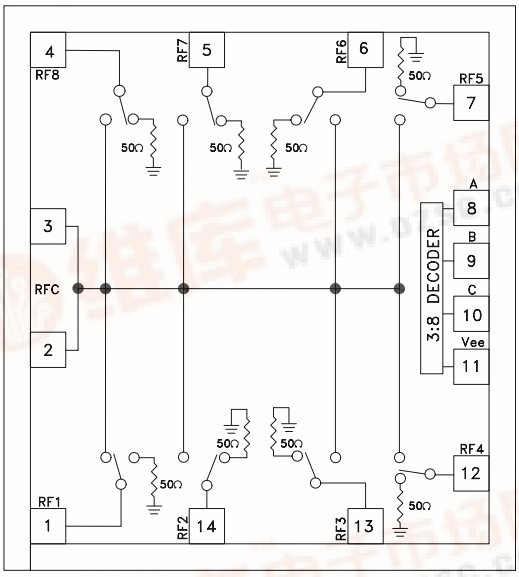
High Isolation: >38 dB@ 4 GHz

Low Insertion Loss: 2.0 dB@ 4 GHz

Integrated 3:8 TTL Decoder

Small Size: 1.45 mm x 1.6 mm x 0.10 mm

Functional Diagram



General Description

The HMC322 is a broadband non-reflective GaAs MESFET SP8T switch chip. Covering DC to 10.0 GHz, this switch offers high isolation and low insertion loss and extends the frequency coverage of Hittite's SP8T switch product line. This switch also includes an on board binary decoder circuit which reduces the required logic control lines to three. The switch operates using a negative control voltage of 0/-5V, and requires a fixed bias of -5V. All data is tested with the chip in a 50 Ohm test fixture connected via 0.025 mm (1 mil) diameter wire bonds of 0.5 mm (20 mils) length.

Electrical Specifications, T_A = +25° C, With 0/-5V Control, Vee= -5V, 50 Ohm System

Parameter		Frequency	Min.	Typ.	Max.	Units
Insertion Loss		DC - 2.0 GHz DC - 4.0 GHz DC - 6.0 GHz DC - 8.0 GHz DC - 10.0 GHz		1.9 2.0 2.1 2.2 2.4	2.3 2.4 2.5 2.6 2.8	dB dB dB dB dB
Isolation (RFC to RF1 - 8)		DC - 2.0 GHz DC - 4.0 GHz DC - 6.0 GHz DC - 8.0 GHz DC - 10.0 GHz	40 32 27 20 18	46 38 32 26 24		dB dB dB dB dB
Return Loss	"On State"	DC - 10.0 GHz		14		dB
Return Loss	"Off State"	DC - 10.0 GHz		11		dB
Input Power for 1 dB Compression		0.5 - 10.0 GHz	19	23		dBm
Input Third Order Intercept (Two-Tone Input Power = +7 dBm Each Tone)		0.5 - 10.0 GHz	34	38		dBm
Switching Characteristics tRISE, tFALL (10/90% RF) tON, tOFF (50% CTL to 10/90% RF)		DC - 10.0 GHz		 50 150		 ns ns

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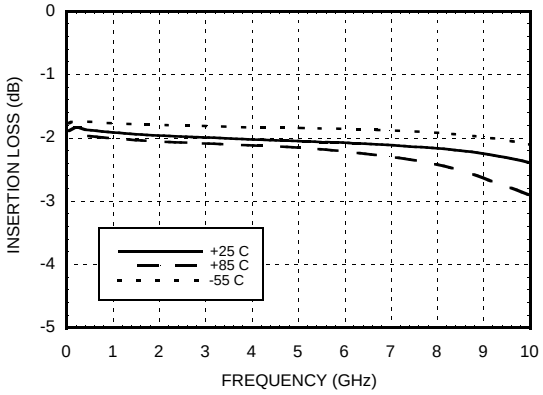
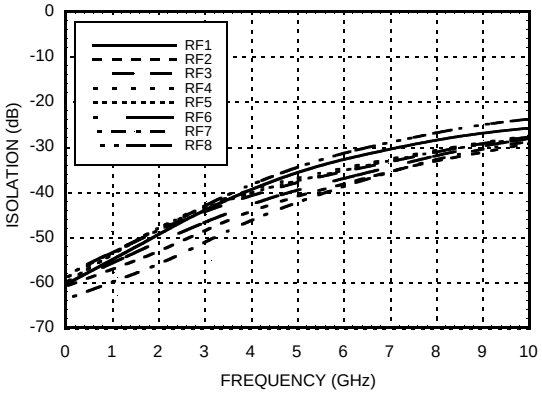
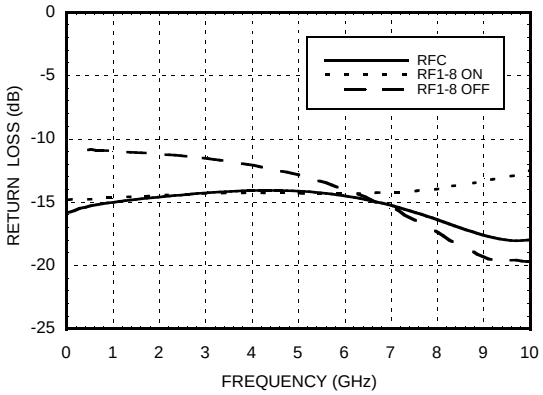
Insertion Loss vs. Temperature



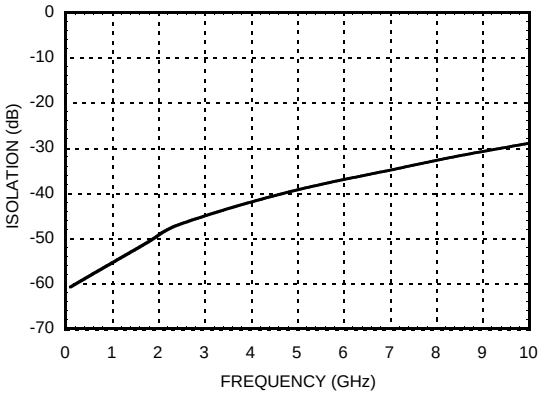
Isolation Between RFC and Output Ports



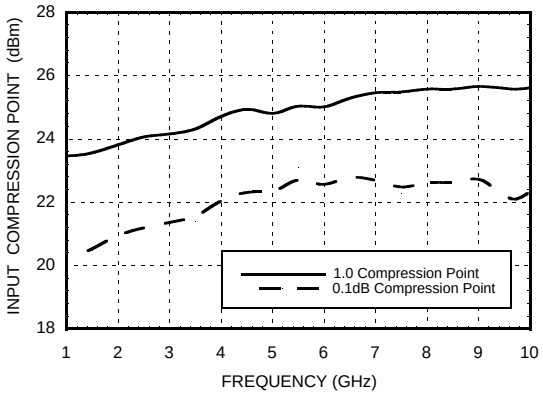
Return Loss



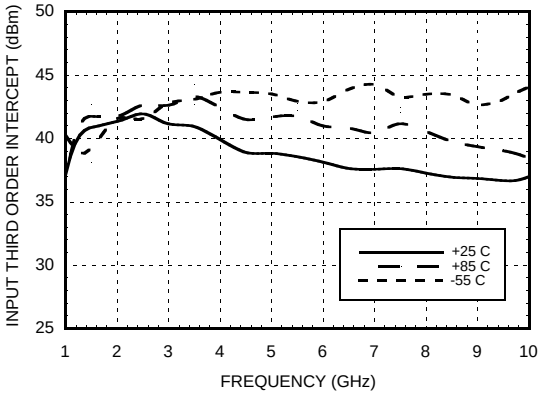
Isolation Between Output Ports



0.1 and 1 dB Input Compression Point



Input Third Order Intercept Point



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Absolute Maximum Ratings

Bias Voltage Range (Vee)	-7.0 Vdc
Control Voltage Range (A, B, & C)	Vee -0.5V to +1.0 Vdc
Storage Temperature	-65 to +150 °C
Operating Temperature	-40 to +85 °C
RF Input Power, 0.5 - 10 GHz	+26 dBm

Bias Voltage & Current

Vee Range = -5.0 Vdc ± 10%		
Vee (Vdc)	Iee (Typ.) (mA)	Iee (Max.) (mA)
-5.0	5.0	9.0

Control Voltages

State	Bias Condition
Low	-3V to 0 Vdc @ 25 uA Typical
High	-5 to -4.2 Vdc @ 5 uA Typical

Truth Table

Control Input			Signal Path State
A	B	C	RFCOM to:
High	High	High	RF1
Low	High	High	RF2
High	Low	High	RF3
Low	Low	High	RF4
High	High	Low	RF5
Low	High	Low	RF6
High	Low	Low	RF7
Low	Low	Low	RF8

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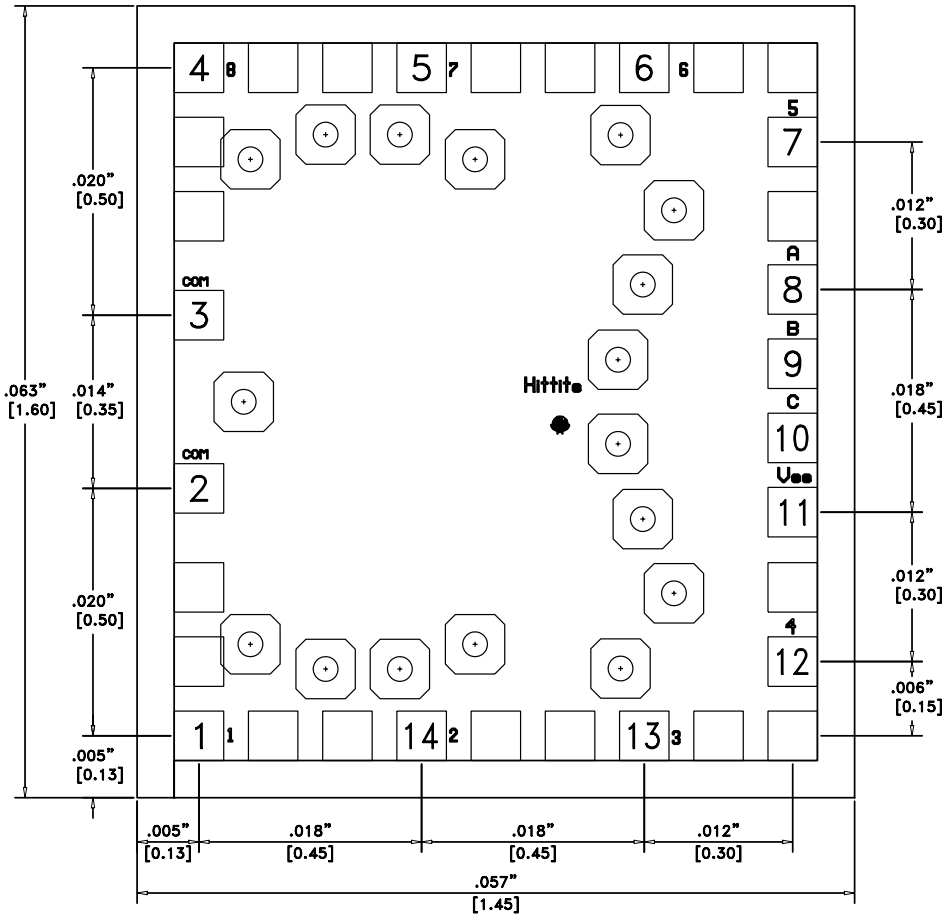
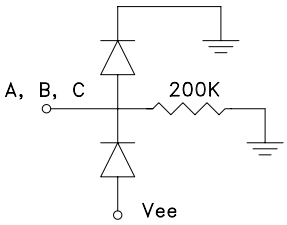
Outline Drawing



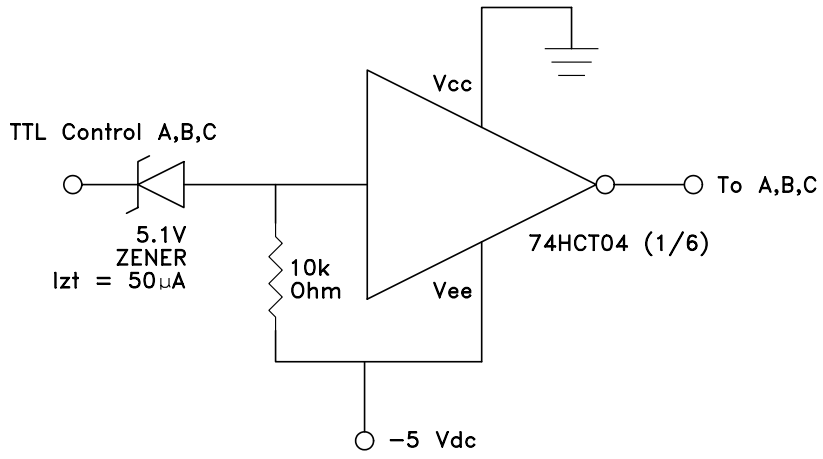
NOTES:

1. DIMENSIONS IN INCHES [MILLIMETERS].
2. DIE THICKNESS IS 0.004".
3. TYPICAL BOND PAD IS 0.004" SQUARE.
4. TYPICAL BOND PAD SPACING IS 0.006" CENTER TO CENTER.
5. BOND PAD METALLIZATION: GOLD.
6. BACKSIDE METALLIZATION: GOLD.
7. BACKSIDE METAL IS GROUND.
8. NO CONNECTION REQUIRED FOR UNLABELED GROUND BOND PADS.

Pad Descriptions

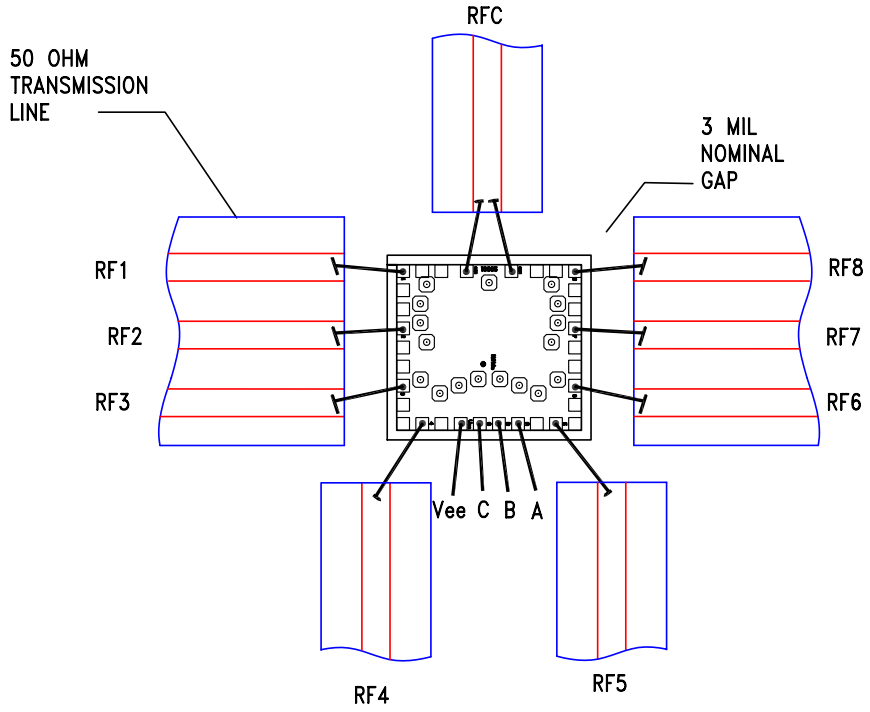
Pad Number	Function	Description	Interface Schematic
1 - 7, 12 - 14	RF1, RFC, RF8 - RF2	These pads are DC coupled and matched to 50 Ohms. Blocking capacitors are required if RF line potential is not equal to 0V.	
8	A	See truth table and control voltage table.	
9	B	See truth table and control voltage table.	
10	C	See truth table and control voltage table.	
11	Vee	Supply Voltage = -5Vdc ± 10%	
Die Bottom	GND	Die bottom must be connected to RF / DC ground.	

TTL Interface Circuit *(Required for Each Control Input A, B and C)*



Note:
Control inputs A, B, and C can be driven directly with TTL logic with -5 Volts applied to the HCT logic gates Vee pin and to the Vee pad of the RF Switch.

Assembly Diagram



Handling Precautions

Follow these precautions to avoid permanent damage.

Cleanliness: Handle the chips in a clean environment. DO NOT attempt to clean the chip using liquid cleaning systems.
Static Sensitivity: Follow ESD precautions to protect against > ± 250V ESD strikes.
Transients: Suppress instrument and bias supply transients while bias is applied. Use shielded signal and bias cables to minimize inductive pick-up.
General Handling: Handle the chip along the edges with a vacuum collet or with a sharp pair of bent tweezers. The surface of the chip has fragile air bridges and should not be touched with vacuum collet, tweezers, or fingers.

Mounting

The chip is back-metallized and can be die mounted with electrically conductive epoxy. The mounting surface should be clean and flat.

Epoxy Die Attach: Apply a minimum amount of epoxy to the mounting surface so that a thin epoxy fillet is observed around the perimeter of the chip once it is placed into position. Cure epoxy per the manufacturer's schedule.

Wire Bonding

Ball or wedge bond with 0.025mm (1 mil) diameter pure gold wire. Thermosonic wirebonding with a nominal stage temperature of 150 deg. C and a ball bonding force of 40 to 50 grams or wedge bonding force of 18 to 22 grams is recommended. Use the minimum level of ultrasonic energy to achieve reliable wirebonds. Wirebonds should be started on the chip and terminated on the package or substrate. All bonds should be as short as possible <0.31mm (12 mils).