HMC364

GaAs HBT MMIC DIVIDE-BY-2, DC - 13.0 GHz

Typical Applications

Prescaler for DC to Ku Band PLL Applications:

- Satellite Communication Systems
- Fiber Optic
- Pt-Pt and Pt-MPt Radios
- VSAT

Features

Ultra Low SSB Phase Noise: -145 dBc/Hz

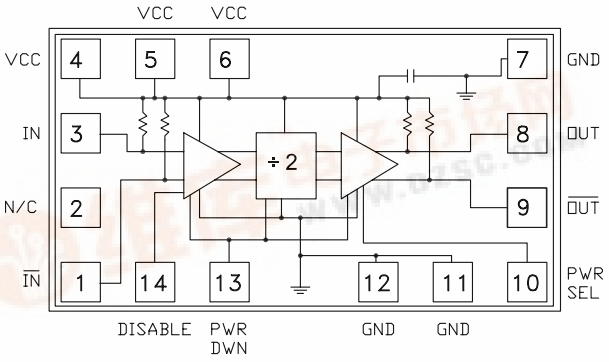
Wide Bandwidth

Output Power: 4 dBm

Single DC Supply: +5V

Small Size: 0.686 mm x 1.143 mm

Functional Diagram



General Description

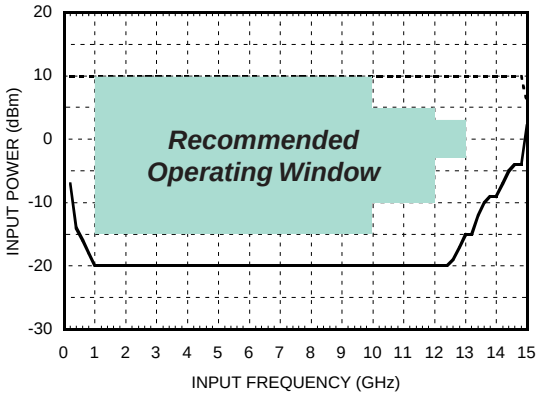
The HMC364 is a low noise Divide-by-2 Static Divider with InGaP GaAs HBT technology that has a small size of 0.686 mm x 1.143 mm. This device operates from DC (with a square wave input) to 13 GHz input frequency with a single +5.0V DC supply. The low additive SSB phase noise of -145 dBc/Hz at 100 kHz offset helps the user maintain good system noise performance.

Electrical Specifications, T_A = +25° C, 50 Ohm System, Vcc= 5V

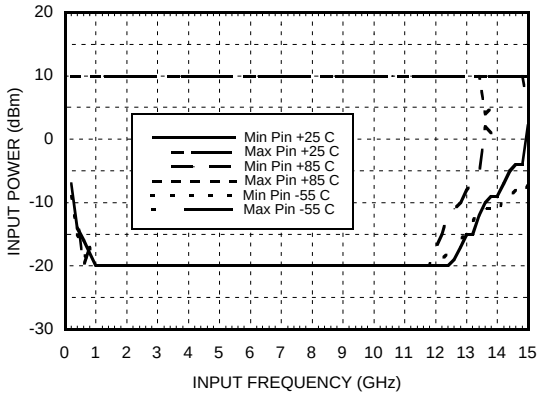
Parameter	Conditions	Min.	Typ.	Max.	Units
Maximum Input Frequency		13	14		GHz
Minimum Input Frequency	Sine Wave Input. [1]		0.2	0.5	GHz
Input Power Range	Fin = 1 to 10 GHz	-15	>-20	+10	dBm
	Fin = 10 to 12 GHz	-10	>-15	+5	dBm
	Fin = 12 to 13 GHz	-4	>-8	+2	dBm
Output Power [2]	Fin = 6 GHz	1	4		dBm
	Fin = 9 GHz	-2			dBm
	Fin = 11 GHz	-5			dBm
	Fin = 13 GHz	-9			dBm
Reverse Leakage	Both RF Outputs Terminated		40		dB
SSB Phase Noise (100 kHz offset)	Pin = 0 dBm, Fin = 6 GHz		-145		dBc/Hz
Output Transition Time	Pin = 0 dBm, Fout = 882 MHz		100		ps
Supply Current (Icc) [2]			105		mA

1. Divider will operate down to DC for square-wave input signal.
2. When operating in high power mode (pin 10 connected to ground).

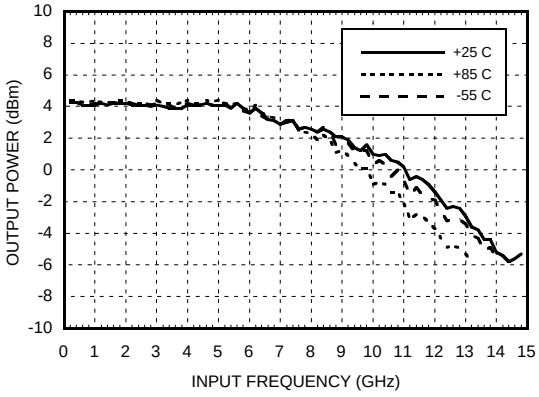
Input Sensitivity Window, T= 25 °C



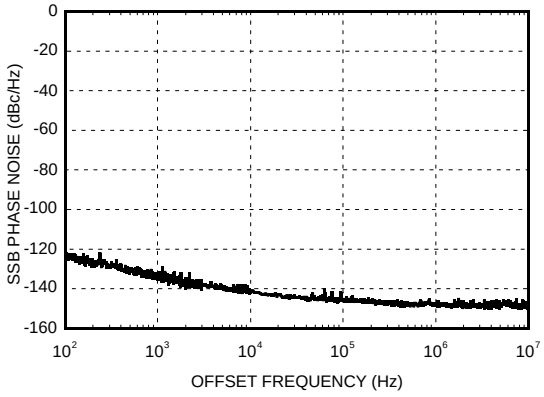
Input Sensitivity Window vs. Temperature



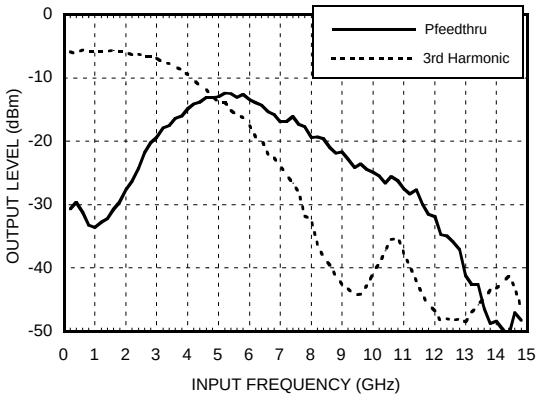
Output Power vs. Temperature



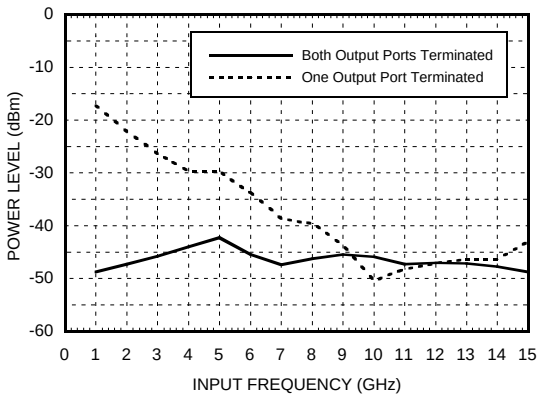
SSB Phase Noise Performance, Pin= 0 dBm, T= 25 °C



Output Harmonic Content, Pin= 0 dBm, T= 25 °C



Reverse Leakage, Pin= 0 dBm, T= 25 °C



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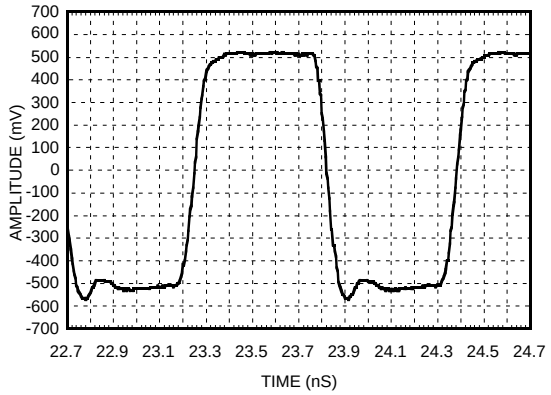
Output Voltage Waveform, Pin= 0 dBm, Fout= 882 MHz, T= 25 °C



Absolute Maximum Ratings

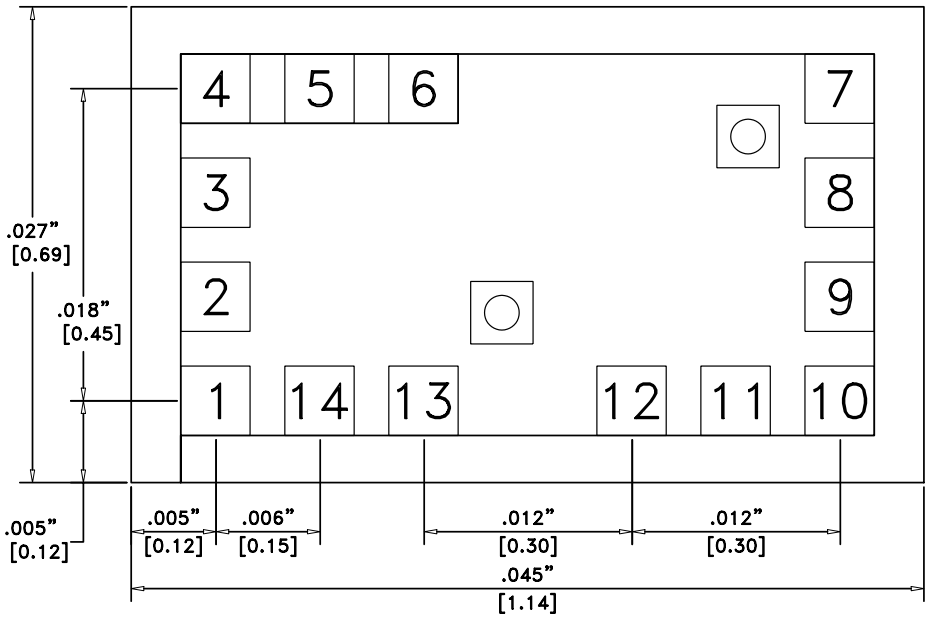
RF Input (Vcc = +5V)	+13
Vcc	+5.5V
VLogic	Vcc -1.6V to Vcc -1.2V
Storage Temperature	-65 to +150 °C
Operating Temperature	-55 to +85 °C

Typical Supply Current vs. Vcc

Vcc (V)	Icc (mA)
4.75	93
5.0	105
5.25	115

Note: Divider will operate over full voltage range shown above

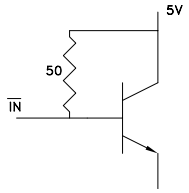
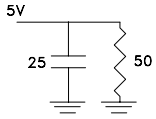
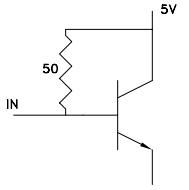
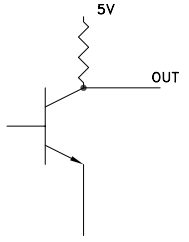
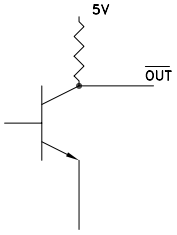
Outline Drawing



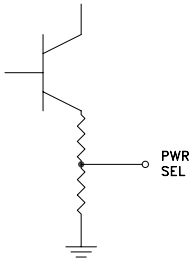
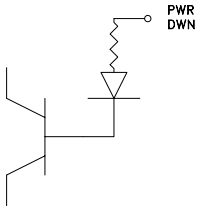
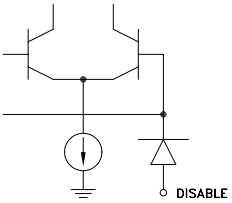
NOTES:

1. ALL DIMENSIONS IN INCHES (MILLIMETERS)
2. ALL TOLERANCES ARE ±0.001 (0.025)
3. DIE THICKNESS IS 0.004 (0.100) BACKSIDE IS GROUND
4. BOND PADS ARE 0.004 (0.100) SQUARE
5. BOND PAD SPACING, CTR-CTR: 0.006 (0.150)
6. BACKSIDE METALLIZATION: GOLD
7. BOND PAD METALLIZATION: GOLD

Pad Description

Pad Number	Function	Description	Interface Schematic
1	$\overline{IN}$	RF Input 180° out of phase with pad 3 for differential operation. AC ground for single ended operation.	
2	N/C	Not Connected	
4, 5, 6	VCC	Supply Voltage 5V ±0.25V can be applied to pad 4, 5, or 6.	
3	IN	RF Input must be DC blocked.	
7, 11, 12	GND	Ground: These pads are grounded.	
8	OUT	Divided Output	
9	$\overline{OUT}$	Divided output 180° out of phase with pad 8.	

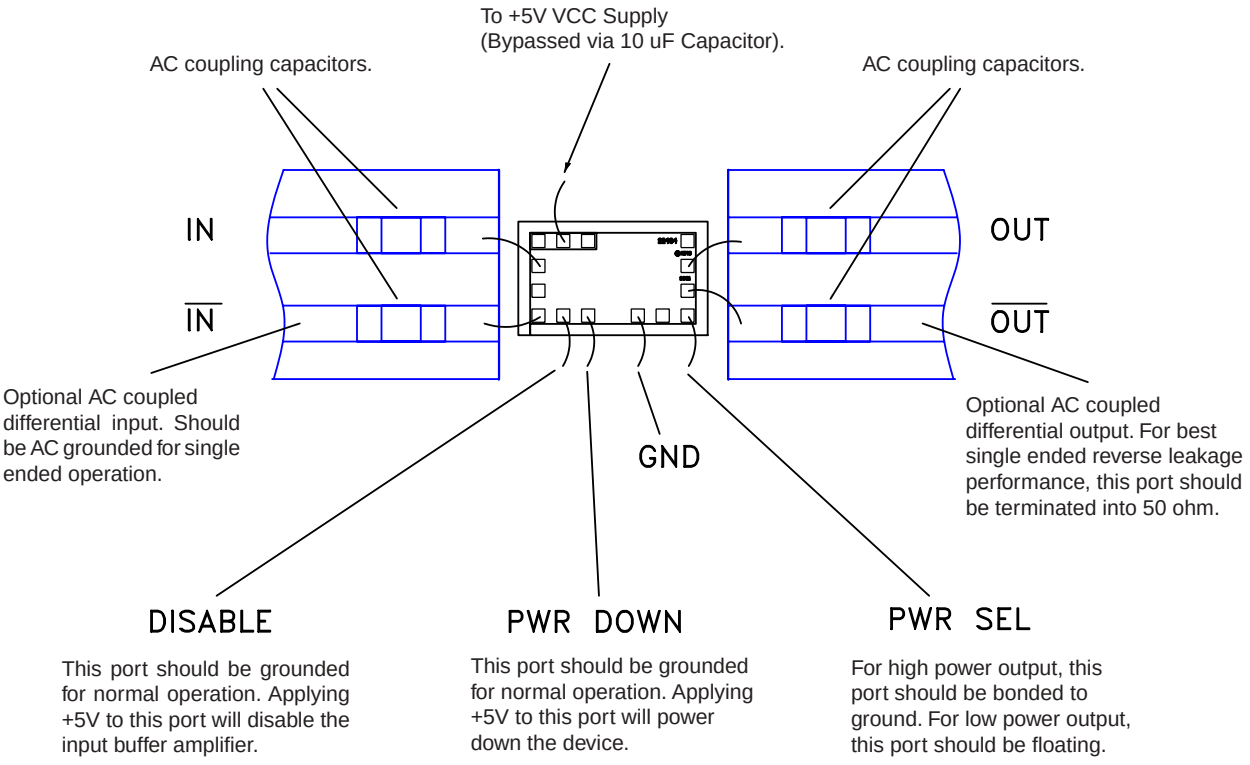
Pad Description *(continued)*

Pad Number	Function	Description	Interface Schematic
10	PWR SEL	In the low power mode, the power select pin is left floating. By grounding this pin, the output power is increased by approximately 6 dB.	
13	PWR DWN	The power down pin is grounded for normal operation. Applying 5 volts to this pin will power down this device.	
14	DISABLE	The disable pin is grounded for normal operation. Applying 5 volts to this pin will disable the input buffer amplifier.	

Truth Table

Function	Pin	5V	GND	Float
DISABLE	14	Output Off	Output On	X
PWR DWN	13	Power Down	Power Up	X
PWR SEL	10	x	High Power Output	Low Power Output
X = State not permitted.				

Assembly Diagram



Handling Precautions

Follow these precautions to avoid permanent damage.

Cleanliness: Handle the chips in a clean environment. DO NOT attempt to clean the chip using liquid cleaning systems.
Static Sensitivity: Follow ESD precautions to protect against > ± 250V ESD strikes.
Transients: Suppress instrument and bias supply transients while bias is applied. Use shielded signal and bias cables to minimize inductive pick-up.
General Handling: Handle the chip along the edges with a vacuum collet or with a sharp pair of bent tweezers. The surface of the chip has fragile air bridges and should not be touched with vacuum collet, tweezers, or fingers.

Mounting

The chip is back-metallized and can be die mounted with AuSn eutectic preforms or with electrically conductive epoxy. The mounting surface should be clean and flat.

Eutectic Die Attach: A 80/20 gold tin preform is recommended with a work surface temperature of 255 °C and a tool temperature of 265 °C. When hot 90/10 nitrogen/hydrogen gas is applied, tool tip temperature should be 290 °C. DO NOT expose the chip to a temperature greater than 320 °C for more than 20 seconds. No more than 3 seconds of scrubbing should be required for attachment.
Epoxy Die Attach: Apply a minimum amount of epoxy to the mounting surface so that a thin epoxy fillet is observed around the perimeter of the chip once it is placed into position. Cure epoxy per the manufacturer's schedule.

Wire Bonding

Ball or wedge bond with 0.025 mm (1 mil) diameter pure gold wire. Thermosonic wirebonding with a nominal stage temperature of 150 °C and a ball bonding force of 40 to 50 grams or wedge bonding force of 18 to 22 grams is recommended. Use the minimum level of ultrasonic energy to achieve reliable wirebonds. Wirebonds should be started on the chip and terminated on the package or substrate. All bonds should be as short as possible <0.31 mm (12 mils).