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HMC372LP3

GaAs PHEMT MMIC LOW NOISE AMPLIFIER, 700 - 1000 MHz

Typical Applications

The HMC372LP3 is ideal for basestation receivers:

- GSM, GPRS & EDGE
- CDMA & W-CDMA
- Private Land Mobile Radio

Features

Noise Figure: <1.0 dB

+34 dBm Output IP3

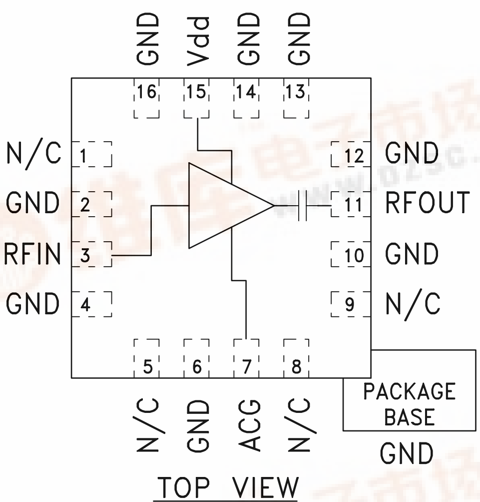
Gain: 15 dB

Very Stable Gain vs. Supply & Temperature

Single Supply: +5.0 V @ 100 mA

50 Ohm Matched Output

Functional Diagram



General Description

The HMC372LP3 is a GaAs PHEMT MMIC Low Noise Amplifier that is ideal for GSM & CDMA cellular basestation front-end receivers operating between 700 and 1000 MHz. The amplifier has been optimized to provide 1.0 dB noise figure, 15 dB gain and +34 dBm output IP3 from a single supply of +5.0V @ 100 mA. Input and output return losses are 25 and 14 dB respectively with the LNA requiring only four external components to optimize the RF Input match, RF ground and DC bias. The HMC372LP3 shares the same package and pinout with the HMC356LP3 high IP3 LNA. A low cost, leadless 3x3 mm (LP3) SMT QFN package houses the low noise amplifier.

Electrical Specifications, $T_A = +25°$ C, Vs = +5V

Parameter	Min.	Typ.	Max.	Min.	Typ.	Max.	Units
Frequency Range		810 - 960			700 - 1000		MHz
Gain	12.5	14.5		11.5	14.5		dB
Gain Variation Over Temperature		0.008	0.015		0.008	0.015	dB / °C
Noise Figure		1.0	1.3		1.0	1.3	dB
Input Return Loss		25			25		dB
Output Return Loss		14			12		dB
Reverse Isolation		20			22		dB
Output Power for 1dB Compression (P1dB)	18	21		17	20		dBm
Saturated Output Power (Psat)		23.5			22.5		dBm
Output Third Order Intercept (IP3) (-20 dBm Input Power per tone, 1 MHz tone spacing)		34		30	33		dBm
Supply Current (Idd)		100			100		mA

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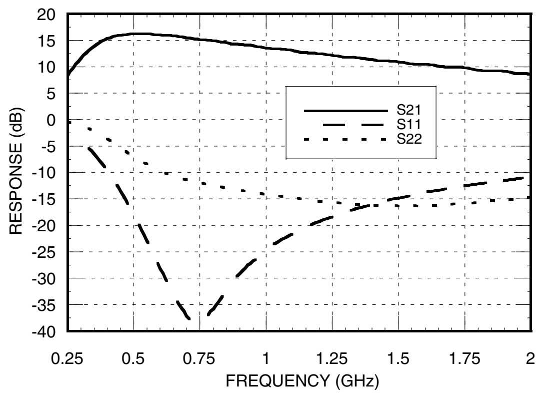
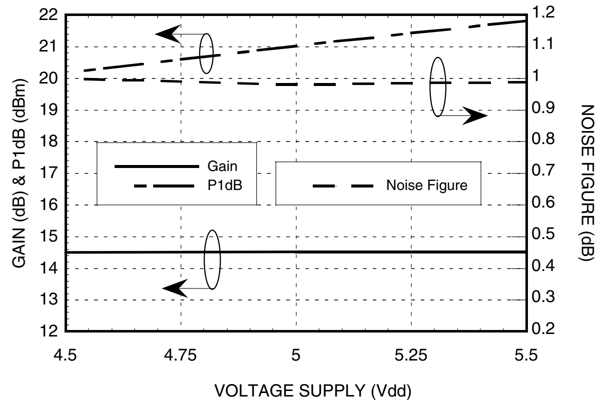
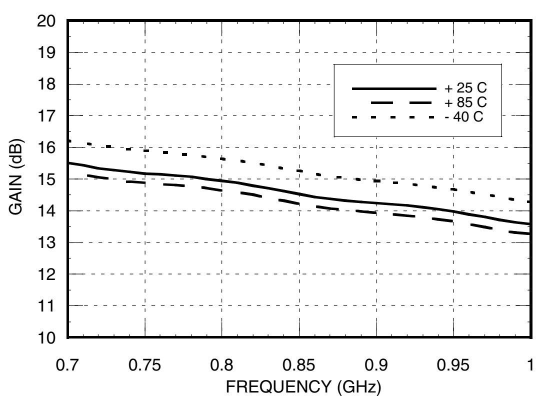
Broadband Gain & Return Loss



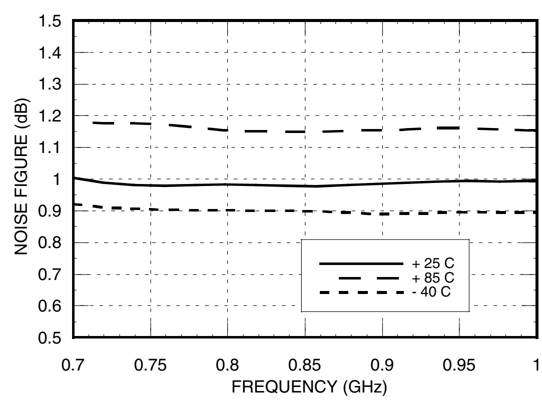
Gain, Noise Figure & Power vs. Supply Voltage @ 850MHz



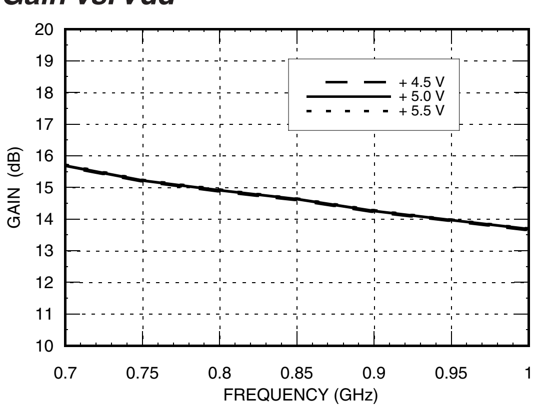
Gain vs. Temperature



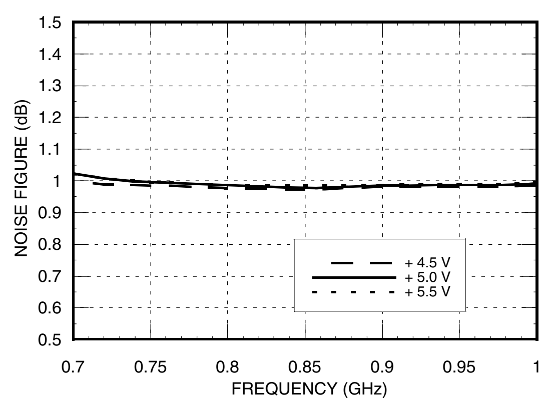
Noise Figure vs. Temperature



Gain vs. Vdd



Noise Figure vs. Vdd



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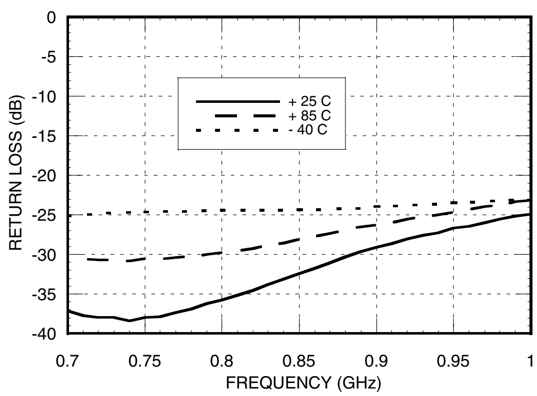
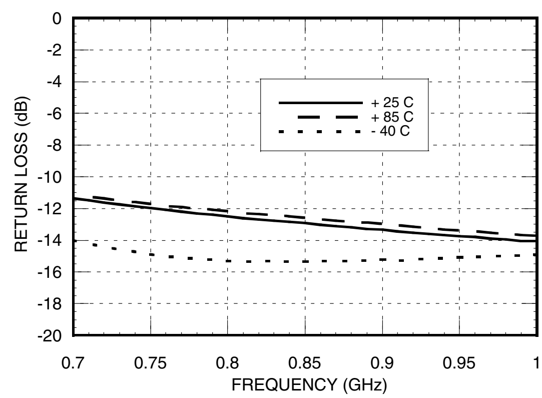
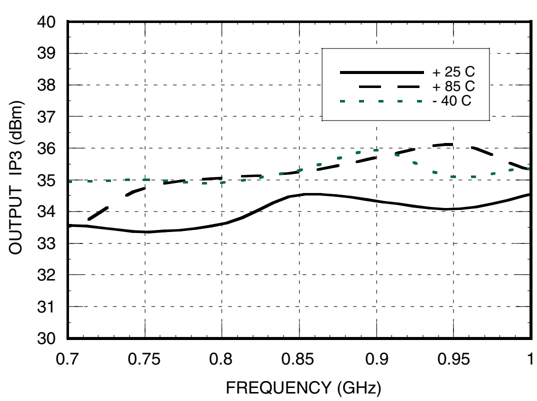
Input Return Loss vs. Temperature



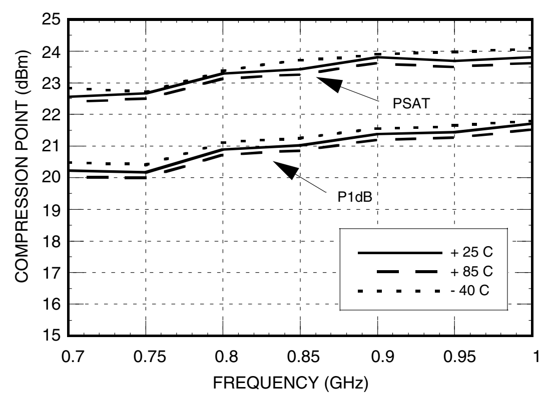
Output Return Loss vs. Temperature



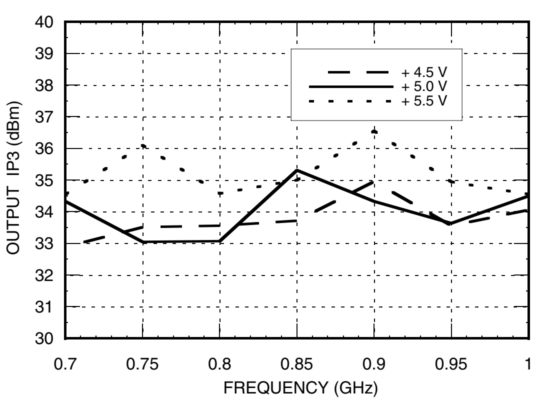
Output IP3 vs. Temperature



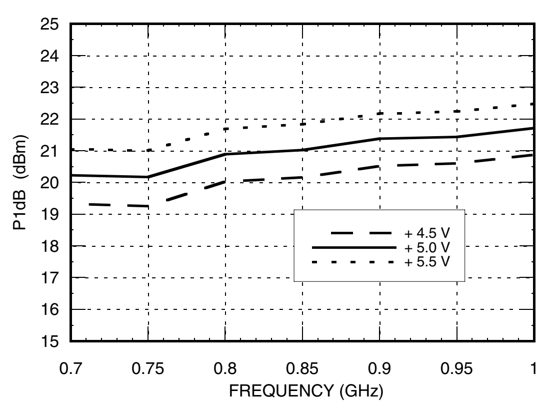
P1dB & Psat vs. Temperature



Output IP3 vs. Vdd



P1dB vs. Vdd



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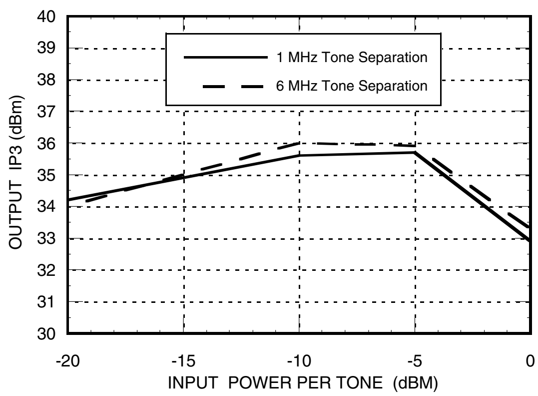
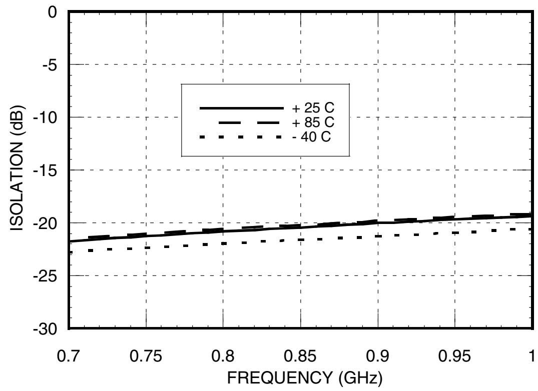
Output IP3 vs. Input Power @ 950 MHz



Reverse Isolation vs. Temperature



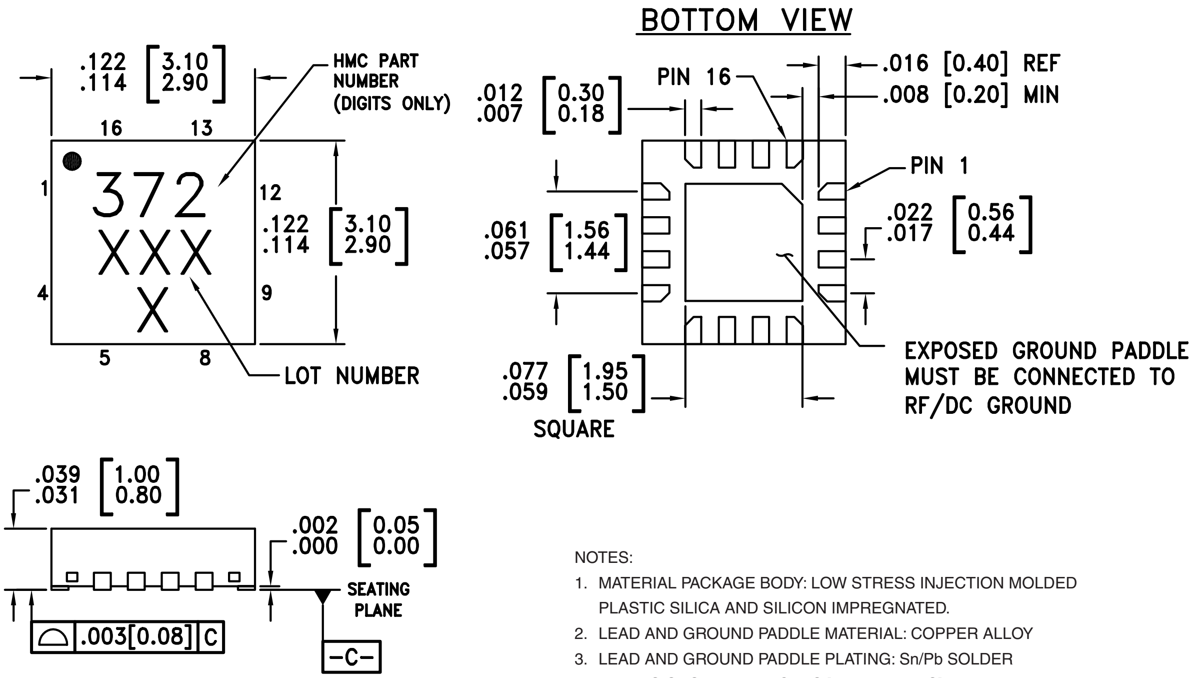
Absolute Maximum Ratings

Drain Bias Voltage (Vdd)	+8.0 Vdc
RF Input Power (RFin)(Vs = +5.0 Vdc)	+15 dBm
Channel Temperature	150 °C
Continuous Pdiss (T = 85 °C) (derate 15.6 mW/°C above 85 °C)	1.015 W
Thermal Resistance (channel to ground paddle)	64.1 °C/W
Storage Temperature	-65 to +150 °C
Operating Temperature	-40 to +85 °C

Typical Supply Current vs. Vdd

Vdd (Vdc)	Idd (mA)
+4.5	98
+5.0	100
+5.5	102

Outline Drawing



NOTES:

1. MATERIAL PACKAGE BODY: LOW STRESS INJECTION MOLDED PLASTIC SILICA AND SILICON IMPREGNATED.
2. LEAD AND GROUND PADDLE MATERIAL: COPPER ALLOY
3. LEAD AND GROUND PADDLE PLATING: Sn/Pb SOLDER
4. DIMENSIONS ARE IN INCHES [MILLIMETERS].
5. LEAD SPACING TOLERANCE IS NON-CUMULATIVE
6. PAD BURR LENGTH SHALL BE 0.15mm MAXIMUM. PAD BURR HEIGHT SHALL BE 0.05mm MAXIMUM.
7. PACKAGE WARP SHALL NOT EXCEED 0.05mm.
8. ALL GROUND LEADS AND GROUND PADDLE MUST BE SOLDERED TO PCB RF GROUND.
9. REFER TO HITTITE APPLICATION NOTE FOR SUGGESTED PCB LAND PATTERN

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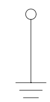
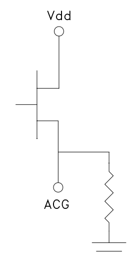
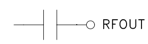
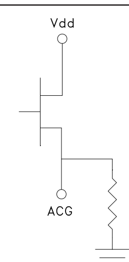
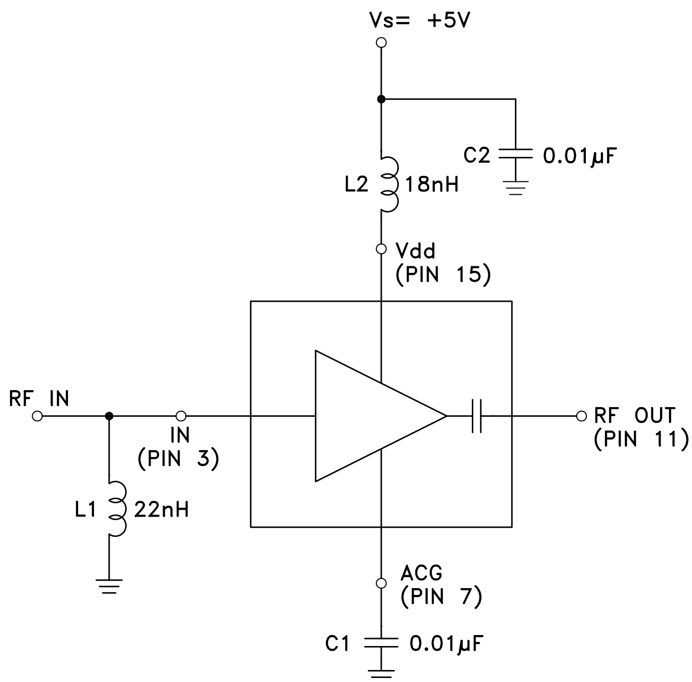
Pin Descriptions

Pin Number	Function	Description	Interface Schematic
1, 5, 8, 9	N/C	No connection necessary. These pins may be connected to RF/DC ground.	
2, 4, 6, 10, 12, 13, 14, 16	GND	These pins must be connected to RF/DC ground.	
3	RF IN	This pin is matched to 50 Ohms with a 22 nH inductor to ground. See Application Circuit.	
7	ACG	AC Ground - An external capacitor of 0.01µF to ground is required for low frequency bypassing. See Application Circuit for further details.	
11	RF OUT	This pin is AC coupled and matched to 50 Ohms.	
15	Vdd	Power supply voltage. Choke inductor and bypass capacitor are required. See application circuit.	

Application Circuit



Note 1: Choose value of capacitor C1 for low frequency bypassing. A 0.01 µF ±10% capacitor is recommended.
Note 2: L1, L2 and C1 should be located as close to the pins as possible.

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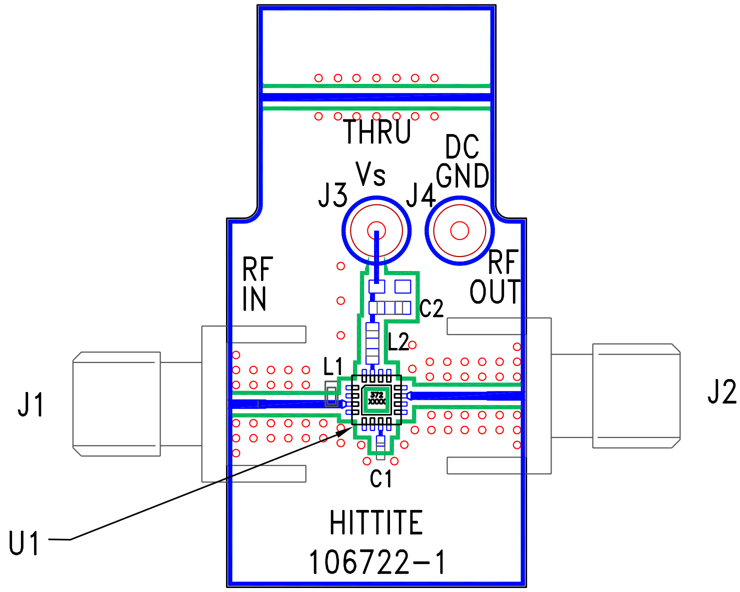
Evaluation PCB



List of Material

Item	Description
J1 - J2	PC Mount SMA RF Connector
J3 - J4	DC Pin
C1	10000 pF Capacitor, 0402 Pkg.
C2	10000 pF Capacitor, 0060 Pkg.
L1	22nH Inductor, 0402 Pkg.
L2	18nH Inductor, 0603 Pkg.
U1	HMC372LP3 Amplifier
PCB*	106722 Eval Board
* Circuit Board Material: Rogers 4350	

The circuit board used in the final application should use RF circuit design techniques. Signal lines should have 50 ohm impedance while the package ground leads and exposed paddle should be connected directly to the ground plane similar to that shown. A sufficient number of VIA holes should be used to connect the top and bottom ground planes. The evaluation circuit board shown is available from Hittite upon request.