Hittite MICROWAVE CORPORATION

v04.1102

HMC394LP4

GaAs HBT PROGRAMMABLE 5-BIT COUNTER, DC - 2.2 GHz

Typical Applications

Programmable divider for offset synthesizer and variable divide by N applications:

- Satellite Communication Systems
- Pt-Pt and Pt-MPt Radios
- LMDS
- SONET

Features

SSB Phase Noise: -153 dBc/Hz @ 100 kHz

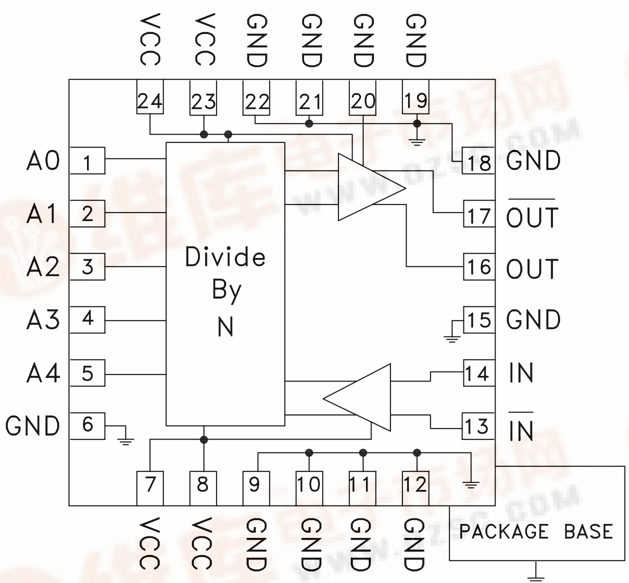
Selectable Division from 2 to 32

Parallel 5-Bit Control

Wide Input Power Range: -20 to +10 dBm

4mm x 4mm Leadless SMT Package

Functional Diagram



General Description

The HMC394LP4 is a low noise GaAs HBT programmable 5-bit counter in a 4mm x 4mm leadless surface mount package. This device allows continuous division from N= 2 to 32 at input frequencies up to 2.2 GHz. The output voltage swing is 800 mV with a duty cycle inversely proportional to N. The low additive SSB phase noise of -153 dBc/Hz at 100 KHz offset makes this counter an excellent choice for low noise synthesizer applications.

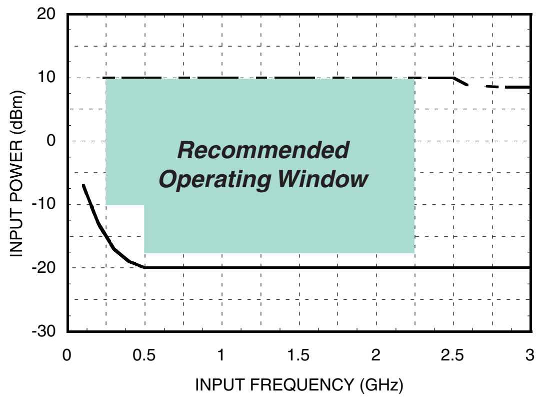
Electrical Specifications, T_A = +25° C, 50 Ohm System, Vcc= 5V

Parameter	Conditions	Min.	Typ.	Max.	Units
Maximum Input Frequency		2.2			GHz
Minimum Input Frequency	Sine Wave Input [1]			0.1	GHz
Input Power Range	Fin = 0.1 to 2.2 GHz	-15	>-20	+10	dBm
Output Power	Divide-by-2		4		dBm
SSB Phase Noise	Fin = 1 GHz, N = 4		-153		dBc/Hz
Output Transition Time			100		ps
Supply Current (Icc)			194		mA

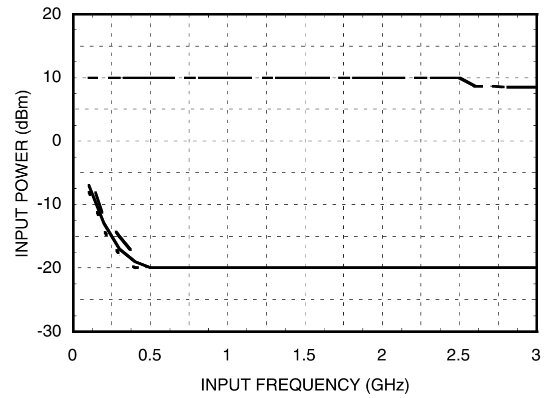
1. Divider will operate down to DC for square-wave input signal.

GaAs HBT PROGRAMMABLE 5-BIT COUNTER, DC - 2.2 GHz

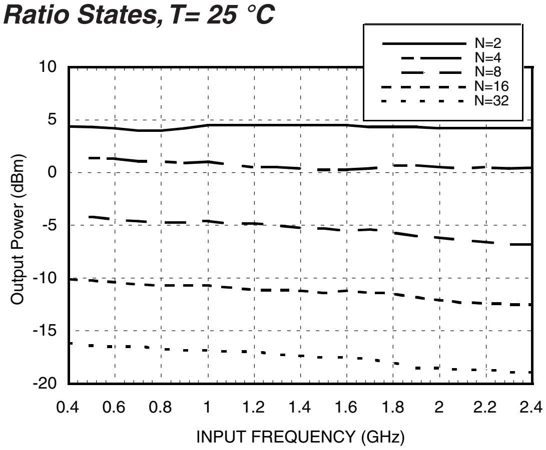
Input Sensitivity Window, 5 major Divide Ratio States, T= 25 °C



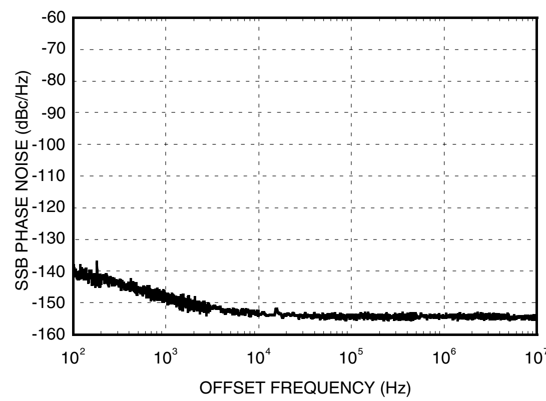
Input Sensitivity Window vs. Temperature, N= 16, T= -40 °C to +85 °C



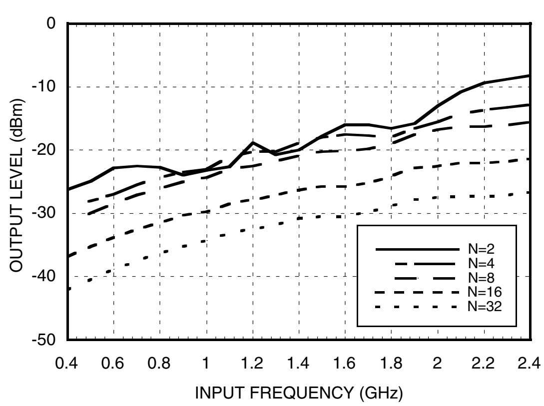
Output Power, 5 Major Divide Ratio States, T= 25 °C



SSB Phase Noise Performance, Fin= 1 GHz, N= 4, T= 25 °C



Fundamental Feedthru Power, Pin= 0 dBm, T= 25 °C



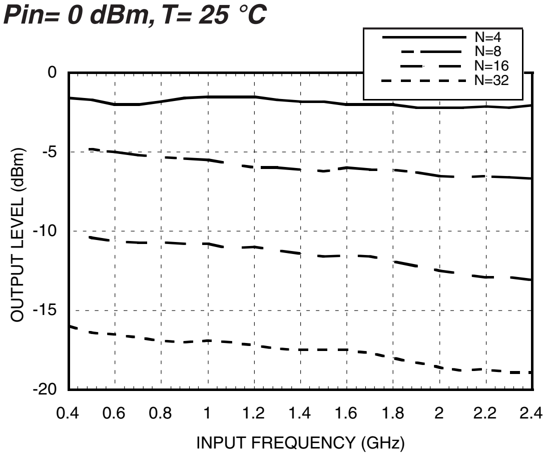
Typical Supply Current vs. Vcc

Vcc (V)	Icc (mA)
4.75	176
5.0	194
5.25	210

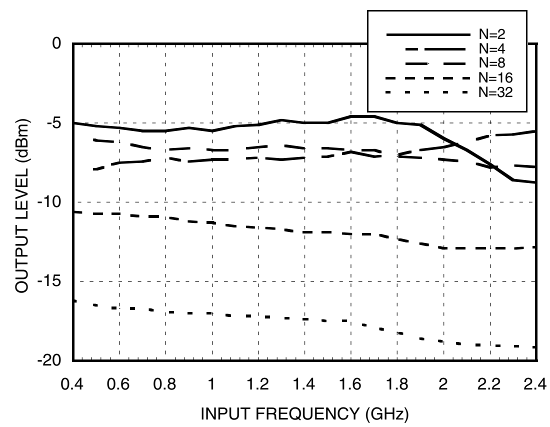
Note: Divider will operate over full voltage range shown above.

GaAs HBT PROGRAMMABLE 5-BIT COUNTER, DC - 2.2 GHz

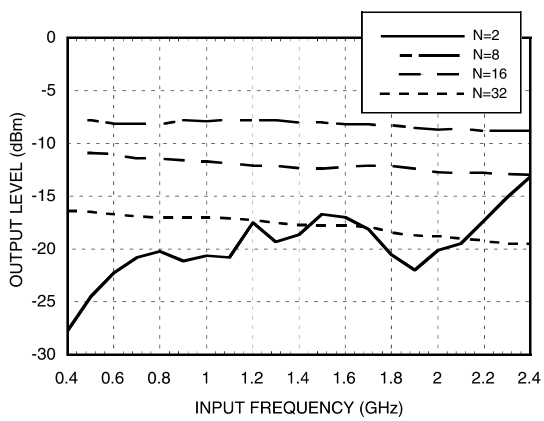
2nd Harmonic, Pin= 0 dBm, T= 25 °C



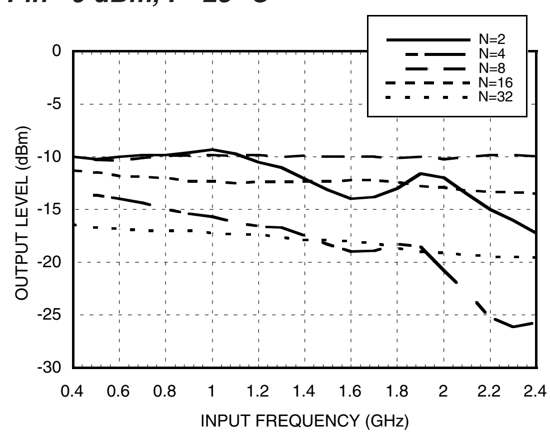
3rd Harmonic, Pin= 0 dBm, T= 25 °C



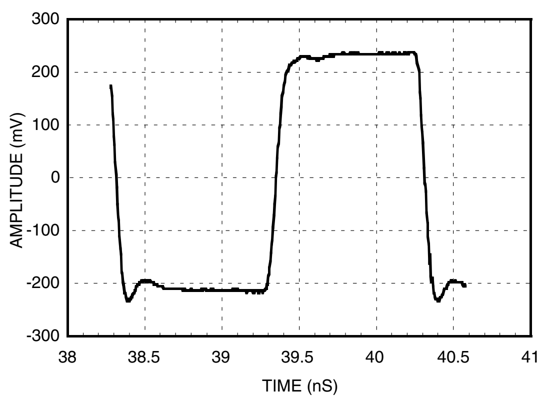
4th Harmonic, Pin= 0 dBm, T= 25 °C



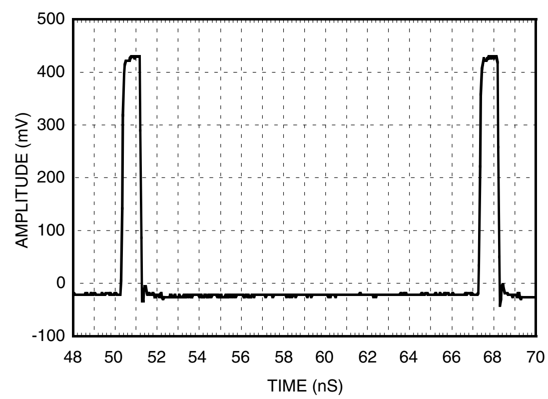
5th Harmonic, Pin= 0 dBm, T= 25 °C



Output Voltage Wavform, Fin= 1 GHz, N= 2, Pin= 0 dBm, T= 25 °C



Output Voltage Wavform, Fin= 1 GHz, N= 17, Pin= 0 dBm, T= 25 °C

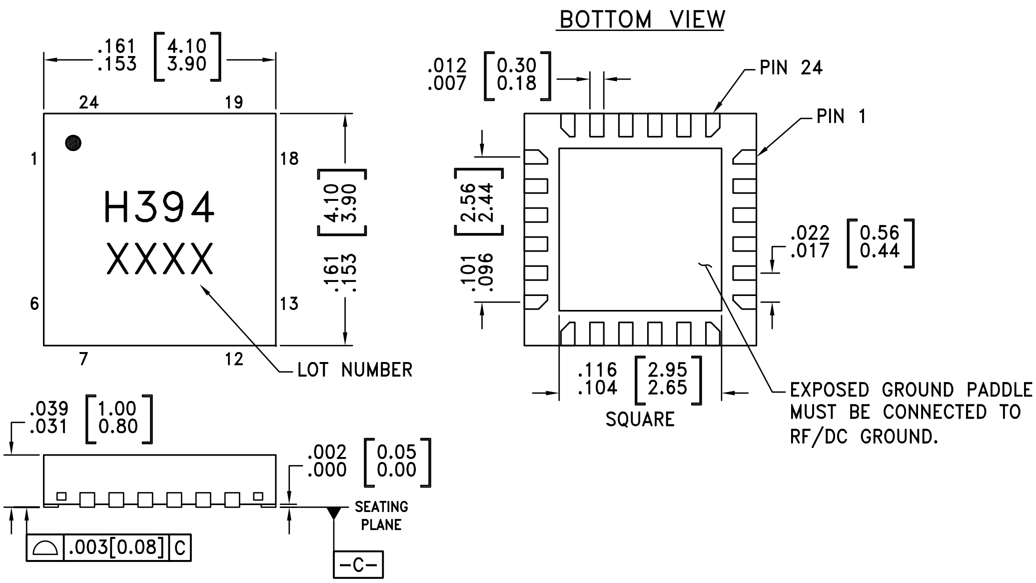


GaAs HBT PROGRAMMABLE 5-BIT COUNTER, DC - 2.2 GHz

Absolute Maximum Ratings

RF Input (Vcc = +5V)	+13 dBm
Vcc	+5.5V
VLogic	-1.6 to -1.2 Vcc
Maximum Channel Temperature	135 °C
Continuous Pdiss (T = 85 °C) (derate 55 mW/°C above 85 °C)	1.155 W
Storage Temperature	-65 to +150 °C
Operating Temperature	-55 to +85 °C

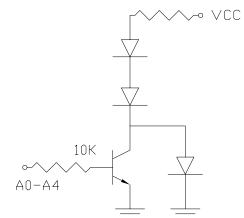
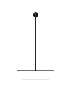
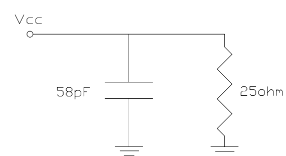
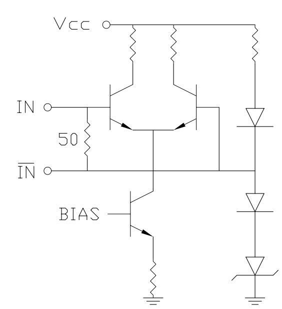
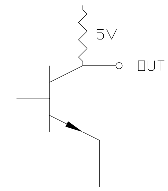
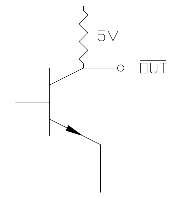
Outline Drawing



NOTES:
1. MATERIAL PACKAGE BODY: LOW STRESS INJECTION MOLDED PLASTIC SILICA AND SILICON IMPREGNATED.
2. LEAD AND GROUND PADDLE MATERIAL: COPPER ALLOY
3. LEAD AND GROUND PADDLE PLATING: Sn/Pb SOLDER
4. DIMENSIONS ARE IN INCHES [MILLIMETERS].
5. LEAD SPACING TOLERANCE IS NON-CUMULATIVE
6. PAD BURR LENGTH SHALL BE 0.15mm MAXIMUM. PAD BURR HEIGHT SHALL BE 0.05mm MAXIMUM.
7. PACKAGE WARP SHALL NOT EXCEED 0.05mm.
8. ALL GROUND LEADS AND GROUND PADDLE MUST BE SOLDERED TO PCB RF GROUND.

GaAs HBT PROGRAMMABLE 5-BIT COUNTER, DC - 2.2 GHz

Pin Description

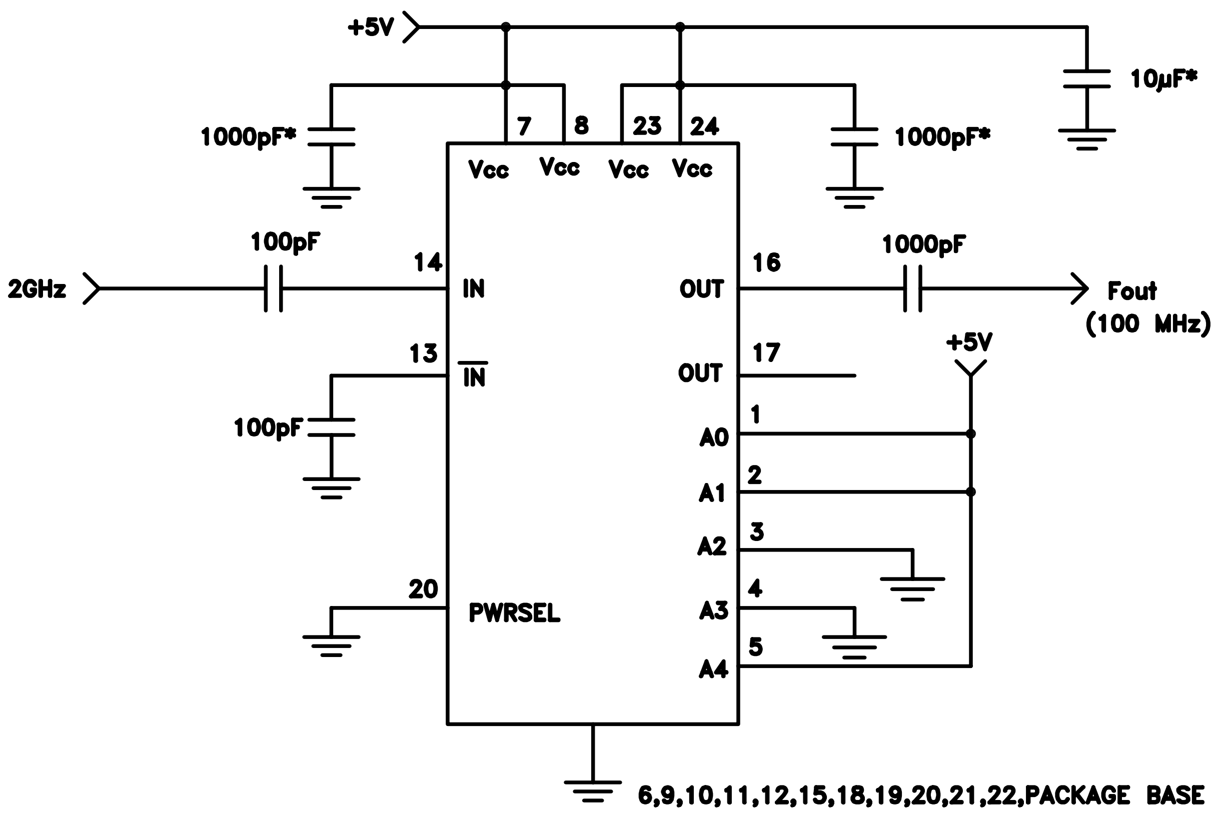
Pin Number	Function	Description	Interface Schematic
1 - 5	AO - A4	CMOS compatible control input bit 0 (LSB) - 4.	
6, 9, 10, 11, 12, 15, 18, 19, 20, 21, 22	GND	Ground: Backside of package has exposed metal ground slug which must be connected to ground.	
7, 8, 23, 24	VCC	Supply voltage 5V ± 0.25V must be applied to all four pins.	
13	$\overline{\text{IN}}$	RF input 180° out of phase with pin 14 must be AC ground.	
14	IN	RF input must be DC blocked.	
16	OUT	Divided output pulse.	
17	$\overline{\text{OUT}}$	Divided output pulse 180° out of phase with pin 16.	

GaAs HBT PROGRAMMABLE 5-BIT COUNTER, DC - 2.2 GHz

HMC394LP4 Programming Truth Table

Function	(LSB) A0	A1	A2	A3	A4
Output Low	0	0	0	0	0
/ 2	1	0	0	0	0
/ 3	0	1	0	0	0
/ 4	1	1	0	0	0
-	-	-	-	-	-
/ 32	1	1	1	1	1
Note: A0 through A4 are CMOS compatible logic control inputs.					

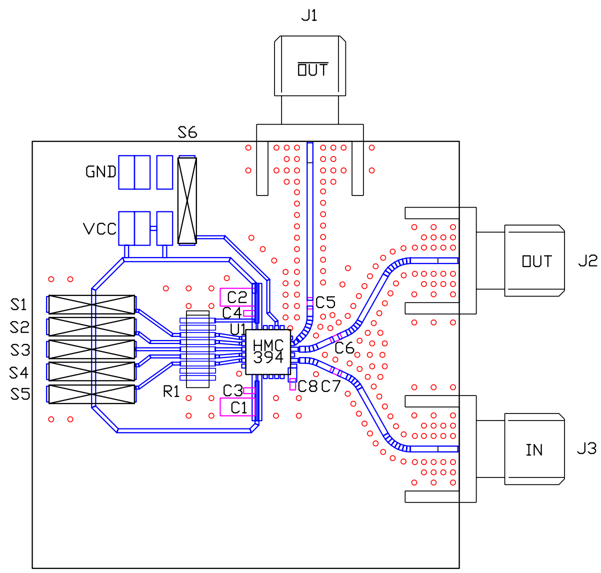
Application Circuit, (2 GHz - Divide-by-20)



* Note: Mount bypass capacitors as close to pins as possible.

GaAs HBT PROGRAMMABLE 5-BIT COUNTER, DC - 2.2 GHz

Evaluation PCB



The circuit board used in the final application should use RF circuit design techniques. Signal lines should have 50 ohm impedance while the package ground leads and backside ground slug should be connected directly to the ground plane similar to that shown. A sufficient number of via holes should be used to connect the top and bottom ground planes. The evaluation circuit board shown is available from Hittite upon request.

Note: C1 and C3 bypass capacitors are not necessary if power supply trace is short.

HMC394LP4 Evaluation PCB Truth Table

Note: The evaluation PCB for the HMC394LP4 contains 10K Ohm pull up resistors for each of the five control inputs A0 through A4. Programming the 31 distinct division ratios consists of installing or removing jumpers S1 through S5, as shown below.

Function	S1	S2	S3	S4	S5
Output Low	0	0	0	0	0
/ 2	1	0	0	0	0
/ 3	0	1	0	0	0
/ 4	1	1	0	0	0
-	-	-	-	-	-
/ 32	1	1	1	1	1
Note: 0 = Jumper Installed. 1 = Jumper Not Installed. Install jumper S6 for high power mode.					

Evaluation Circuit Board Layout Design Details

Item	Description
J1 - J3	PC Mount SMA RF Connector
C1 - C2*	1.0 µF Tantalum Capacitor
C3 - C4*	.01 µF Capacitor, 0603 Pkg.
C5 - C8	1000 pF Capacitor, 0603 Pkg.
R1*	Resistor SIP 10 K ohm
S1 - S6	Jumper (shunt) 2mm
U1	HMC394LP4 5-Bit Counter
PCB	104435 Eval Board
* Optional components.	

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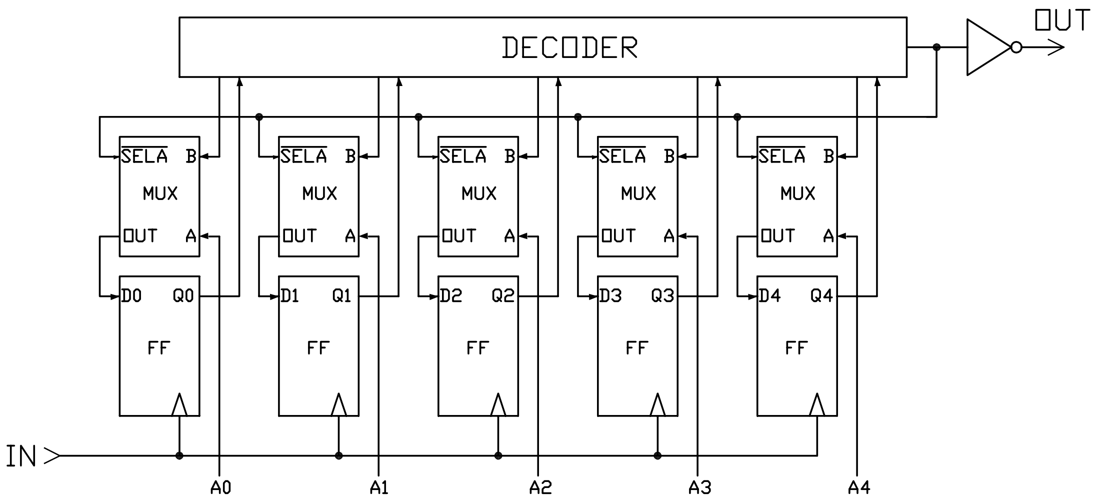
Applications Information

Simplified Block Diagram



Asynchronous Programming

The 5-Bit programmable counter counts-down from the programmed value of the data bits to zero and issues an output pulse at the end of each cycle. Settling time of the programmable 5-Bit counter is defined as the maximum time required for the counter to change the division ratio N to a new value after the data bits have settled. The worst case settling time occurs if the data bits A0 thru A4 are changing during the load cycle. Under this condition, the data bits may potentially be erroneous when they are clocked in and in the worst case could be all 1's, requiring 32 clock cycles until the correct data is re-loaded into the flip flops. The worst case asynchronous settling time can be calculated as follows:

$$T_{SETTLING\ MAX} = 32/f_{IN} \text{ (For Asynchronous Programming)}$$

As an example, if the input frequency is 1 GHz, the maximum settling time is 32 nS

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Synchronous Programming

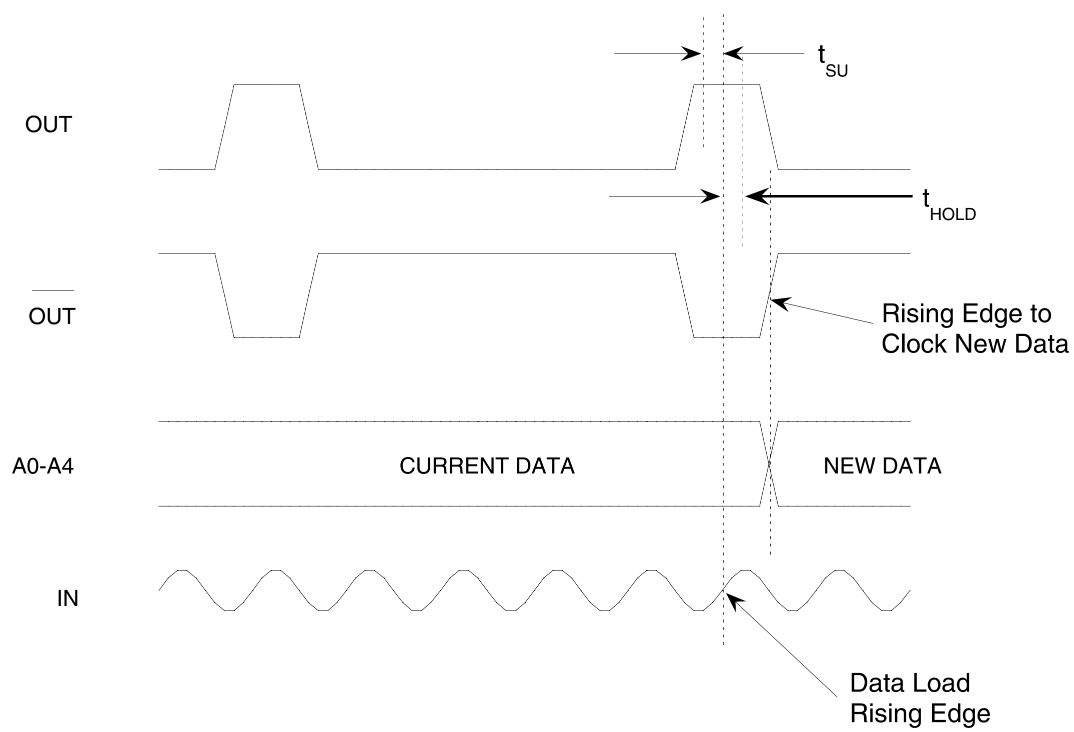
For applications which can not tolerate a momentary undefined division ratio, which normally occurs while changing the data bits (A0-A4) at random, synchronous programming can be used. Data is loaded into the counter on every rising edge of the clock which occurs while the output (OUT) is "HIGH". The typical minimum setup and hold times are shown in the table below as a function of frequency. For precision applications, the rising edge of the complementary output may be used to latch the new data bits (A0-A4), so that all bits are settled before the next load cycle.

$$T_{SETTLING\ MAX} = N/f_{IN} \text{ (For Synchronous Programming)}$$

Where N is the desired division ratio, and f_{IN} = Input Frequency (Hz)

Parameter	0.5 GHz	1 GHz	2 GHz
t_{SETUP}	200 ps	200 ps	200 ps
t_{HOLD}	700 ps	300 ps	120 ps

Programmable Divider Timing Requirements for Synchronous Programming



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CMOS/TTL Input Characteristics

Maximum Input Logic “0” Voltage ($V_{IL\ MAXIMUM}$) = 1.1V @ 10 uA.

Minimum Input Logic “1” Voltage ($V_{IH\ MINIMUM}$) = 1.8V @ 500 uA.

Input IV characteristics for the logic inputs (A0-A4) are shown below: