

v00.0202

HMC425LP3

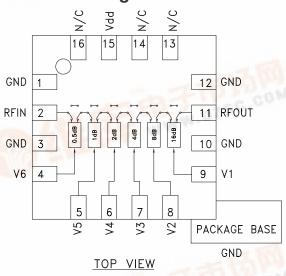
0.5 dB LSB GaAs MMIC 6-BIT DIGITAL POSITIVE CONTROL ATTENUATOR, 2.4 - 8.0 GHz

Typical Applications

The HMC425LP3 is ideal for:

- WLAN & Point-to-Multi-Point
- Fiber Optics & Broadband Telecom
- Microwave Radio & VSAT
- Military

Functional Diagram



Features

0.5 dB LSB Steps to 31.5 dB
Single Control Line Per Bit
+/- 0.5 dB Typical Bit Error
Single +5V Supply
3 mm x 3 mm x 1 mm SMT Package

General Description

The HMC425LP3 is a broadband 6-bit GaAs IC digital attenuator in a low cost leadless surface mount package. Covering 2.4 to 8.0 GHz, the insertion loss is less then 3.8 dB typical. The attenuator bit values are 0.5 (LSB), 1, 2, 4, 8, and 16 dB for a total attenuation of 31.5 dB. Attenuation accuracy is excellent at \pm 0.5 dB typical step error with an IIP3 of +40 dBm. Six control voltage inputs, toggled between 0 and +3 to +5V, are used to select each attenuation state. A single Vdd bias of +3 to +5V is required.

Electrical Specifications,

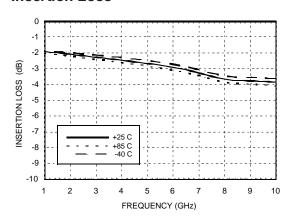
 $T_A = +25^{\circ}$ C, With Vdd = +5V & Vctl = 0/+5V (Unless Otherwise Noted)

Parameter	Frequency (GHz)	Min.	Тур.	Max.	Units
Insertion Loss	2.4 - 6.0 GHz 6.0 - 8.0 GHz	TE.	3.0 3.8	3.5 4.3	dB dB
Attenuation Range	2.4 - 8.0 GHz		31.5		dB
Return Loss (RF1 & RF2, All Atten. States)	2.4 - 8.0 GHz	11	15		dB
Attenuation Accuracy: (Referenced to Insertion Loss) All States	2.4 - 8.0 GHz	± 0.5 + 5% of Atten. Setting Max.		dB	
Input Power for 0.1 dB Compression Vdd = 5V Vdd = 3V	2.4 - 8.0 GHz		22 19		dBm dBm
Input Third Order Intercept Point REF - 16.0 dB States (Two-Tone Input Power= 0 dBm Each Tone) 16.5 - 31.5 dB States	2.4 - 8.0 GHz		45 35		dBm dBm
Switching Characteristics	2.4 - 8.0 GHz				
tRISE, tFALL (10/90% RF) tON: tOFF (50% CTL to 10/90% RF)			160 180		ns ns

MICROWAVE CORPORATION

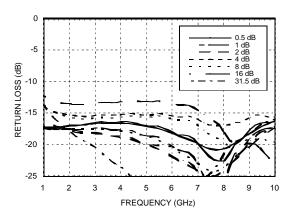
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Insertion Loss



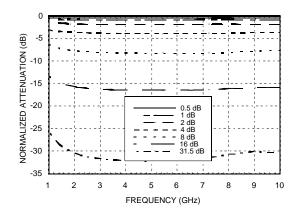
Return Loss RF1, RF2

(Only Major States are Shown)

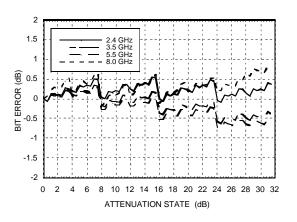


Normalized Attenuation

(Only Major States are Shown)

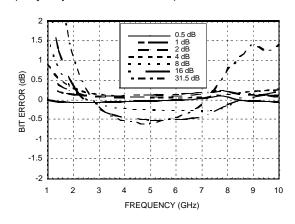


Bit Error vs. Attenuation State



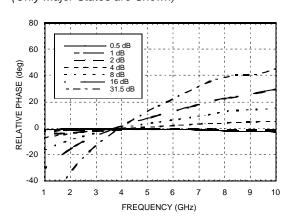
Bit Error vs. Frequency

(Only Major States are Shown)



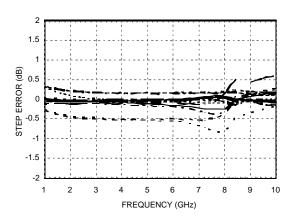
Relative Phase vs. Frequency

(Only Major States are Shown)





Worst Case Step Error Between Successive Attenuation States



Truth Table

Control Voltage Input				Attenuation			
V1 16 dB	V2 8 dB	V3 4 dB	V4 2 dB	V5 1 dB	V6 0.5 dB	State RF1 - RF2	
High	High	High	High	High	High	Reference I.L.	
High	High	High	High	High	Low	0.5 dB	
High	High	High	High	Low	High	1 dB	
High	High	High	Low	High	High	2 dB	
High	High	Low	High	High	High	4 dB	
High	Low	High	High	High	High	8 dB	
Low	High	High	High	High	High	16 dB	
Low	Low	Low	Low	Low	Low	31.5 dB	

Any combination of the above states will provide an attenuation approximately equal to $\,$ the sum of the bits selected.

Bias Voltage & Current

Vdd Range = 3.0 to +5.0 Vdc		
Vdd (VDC)	ldd (Typ.) (μΑ)	
+3.0	10	
+5.0	30	

Control Voltage

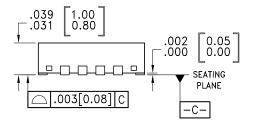
State	Bias Condition
Low	0 to 0.2V @ 10 uA Typ.
High	Vdd ± 0.2V @ 5 uA Typ.
Note: Vdd = +3V to +5V	



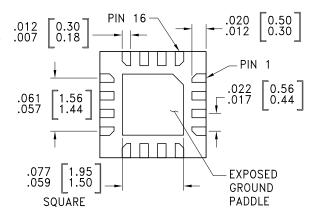
Absolute Maximum Ratings

Control Voltage (V1 to V6)	Vdd +0.5 Vdc
Bias Voltage (Vdd)	+7.0 Vdc
Staorage Temperature	-65 to +150 °C
Operating Temperature	-40 to +85 °C
RF Input Power (2.4 - 8.0 GHz)	+30 dBm

Outline Drawing



BOTTOM VIEW



NOTES:

- MATERIAL PACKAGE BODY: LOW STRESS INJECTION MOLDED PLASTIC SILICA AND SILICON IMPREGNATED.
- 2. LEAD AND GROUND PADDLE MATERIAL: COPPER ALLOY
- 3. LEAD AND GROUND PADDLE PLATING: Sn/Pb SOLDER
- 4. DIMENSIONS ARE IN INCHES [MILLIMETERS].
- 5. LEAD SPACING TOLERANCE IS NON-CUMULATIVE
- PAD BURR LENGTH SHALL BE 0.15mm MAXIMUM.
 PAD BURR HEIGHT SHALL BE 0.05mm MAXIMUM.
- 7. PACKAGE WARP SHALL NOT EXCEED 0.05mm.
- 8. ALL GROUND LEADS AND GROUND PADDLE MUST BE SOLDERED TO PCB RF GROUND.

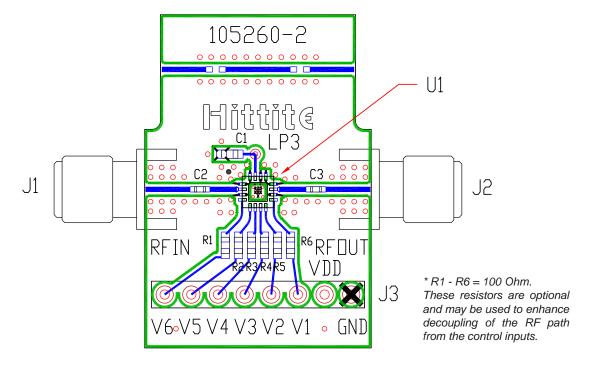


Pin Descriptions

Pin Number	Function	Description	Interface Schematic	
1, 3, 10, 12	GND	Package bottom has an exposed metal paddle that must also be connected to RF Ground.	0	
2, 11	RFIN, RFOUT	This pin is DC coupled and matched to 50 Ohm. Blocking capacitors are required.		
4, 5, 6, 7, 8, 9	V1 - V6	See truth table and control voltage table.	500 	
13, 14, 16	N/C	This pin should be connected to PCB RF ground to maximize performance.		
15	Vdd	Supply Voltage.		



Evaluation PCB



The circuit board used in the final application should use RF circuit design techniques. Signal lines should have 50 ohm impedance while the package ground leads and exposed paddle should be connected directly to the ground plane similar to that shown. A sufficient number of via holes should be used to connect the top and bottom ground planes. The evaluation circuit board shown is available from Hittite upon request.

List of Material

Item	Description	
J1 - J2	PC Mount SMA Connector	
J3	8 Pin DC Connector	
C1	0.01 μF Capacitor, 0603 Pkg.	
C2, C3	100 pF Capacitor, 0402 Pkg.	
R1 - R6	100 Ohm Resistor, 0603 Pkg.	
U1	HMC425LP3 Digital Attenuator	
PCB*	105260 Evaluation PCB	
* Circuit Board Material: Rogers 4350		