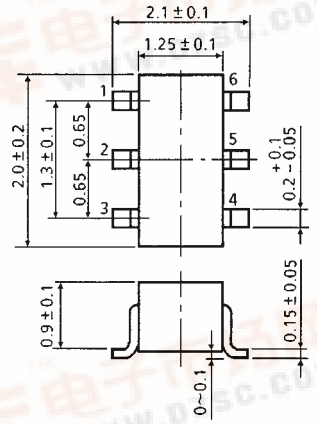
TOSHIBA Field Effect Transistor Silicon N Channel MOS Type

HN1K04FU

High Speed Switching Applications
Analog Switch Applications

- High input impedance and extremely low drive current.
- V_{th} is low and it is possible to drive directly at low-voltage CMOS.
  : V_{th} = 0.8 to 2.5 V
- Switching speed is fast.
- Suitable for high-density mounting because of a compact package.

Unit: mm



1. SOURCE 1
2. GATE 1
3. DRAIN 2
4. SOURCE 2
5. GATE 2
6. DRAIN 1

US6

JEDEC	—
JEITA	—
TOSHIBA	2-2J1C

Weight: 6.8 mg

Maximum Ratings (Ta = 25°C) (Q1, Q2 common)

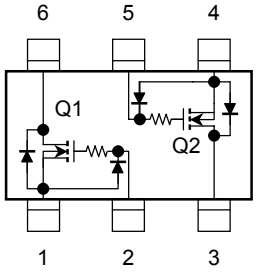
Characteristics	Symbol	Rating	Unit
Drain-source voltage	V_{DS}	50	V
Gate-source voltage	V_{GSS}	10	V
DC drain current	I_D	50	mA
Drain power dissipation	P_D (Note)	200	mW
Channel temperature	T_{ch}	150	°C
Storage temperature range	T_{stg}	−55 to 150	°C

Note: TOTAL rating

Electrical Characteristics (Ta = 25°C) (Q1, Q2 common)

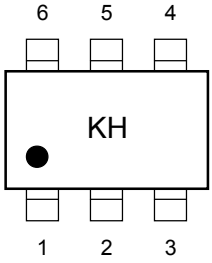
Characteristic	Symbol	Test Condition	Min	Typ.	Max	Unit
Gate leakage current	I_{GSS}	V_{GS} = 10 V, V_{DS} = 0 V	—	—	1	μA
Drain-source breakdown voltage	$V_{(BR)\ DSS}$	I_D = 100 μA, V_{GS} = 0 V	50	—	—	V
Drain cut-off current	I_{DSS}	V_{DS} = 50V, V_{GS} = 0 V	—	—	1	μA
Gate threshold voltage	V_{th}	V_{DS} = 5V, I_D = 0.1 mA	0.8	—	2.5	V
Forward transfer admittance	$\|Y_{fs}\|$	V_{DS} = 5V, I_D = 10 mA	20	—	—	mS
Drain-source ON resistance	$R_{DS\ (ON)}$	I_D = 10 mA, V_{GS} = 4.0 V	—	20	50	Ω
Input capacitance	C_{iss}	V_{DS} = 5 V, V_{GS}=0 V, f = 1 MHz	—	6.3	—	pF
Reverse transfer capacitance	C_{rss}	V_{DS} = 5 V, V_{GS}=0 V, f = 1 MHz	—	1.3	—	pF
Output capacitance	C_{oss}	V_{DS} = 5 V, V_{GS}=0 V, f = 1 MHz	—	5.7	—	pF
Switching time	t_{on}	V_{DD} = 5 V, I_D = 10 mA, V_{GS} = 0 to 4.0 V	—	0.11	—	μs
	t_{off}	V_{DD} = 5 V, I_D = 10 mA, V_{GS} = 0 to 4.0 V	—	0.15	—	

Equivalent Circuit (top view)



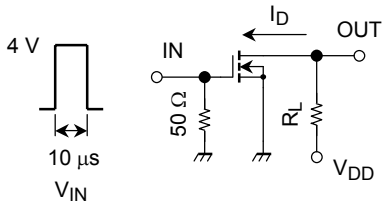
(Q1, Q2 common)

Marking



Switching Time Test Circuit

(a) Test circuit



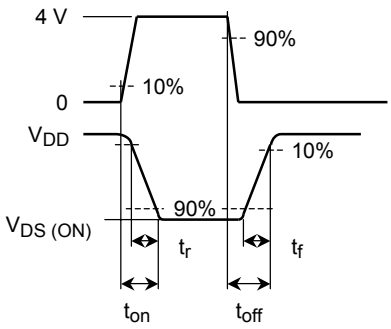
V_{DD} = 5 V
D.U. ≦ 1%
V_{IN}: t_r, t_f < 5 ns
(Z_{out} = 50 Ω)
Common Source
Ta = 25°C

(b) V_{IN}

V_{GS}

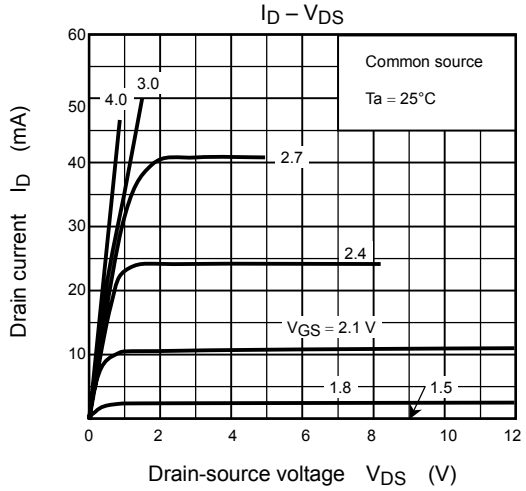
(c) V_{OUT}

V_{DS}

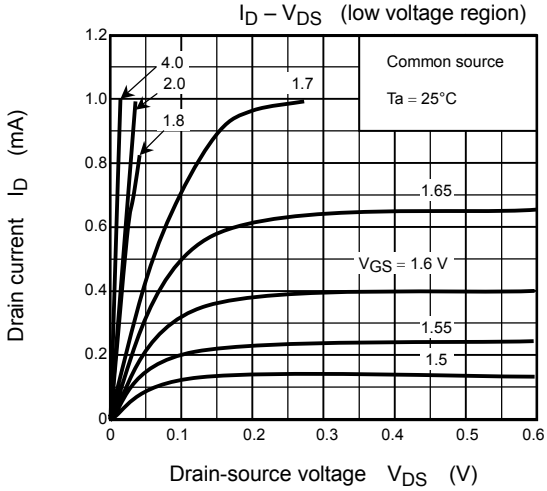


(Q1, Q2 common)

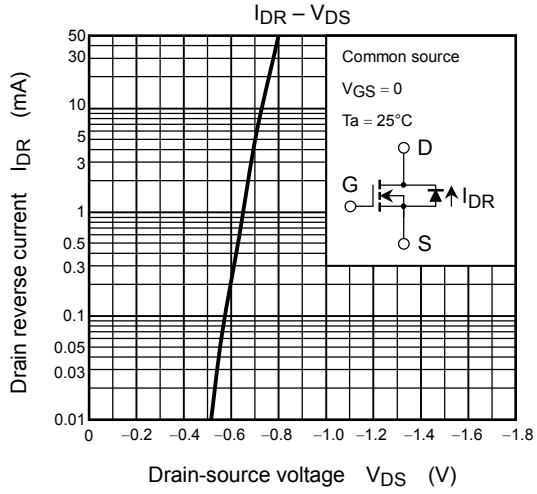
$I_D - V_{DS}$



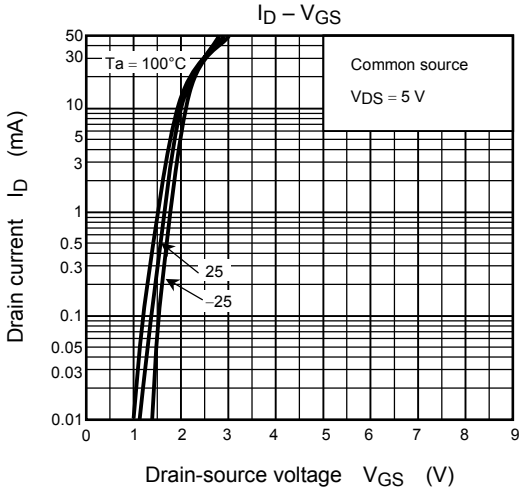
$I_D - V_{DS}$ (low voltage region)



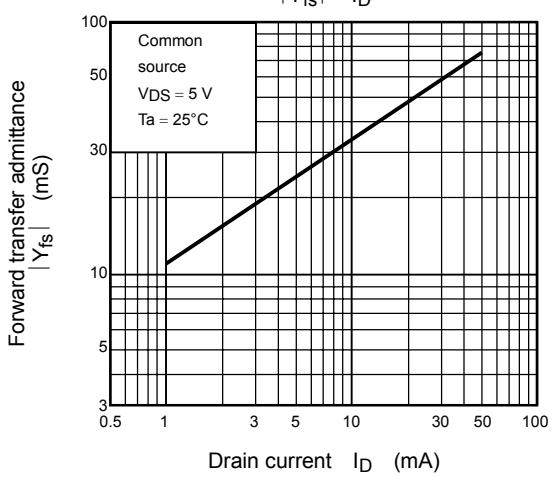
$I_{DR} - V_{DS}$



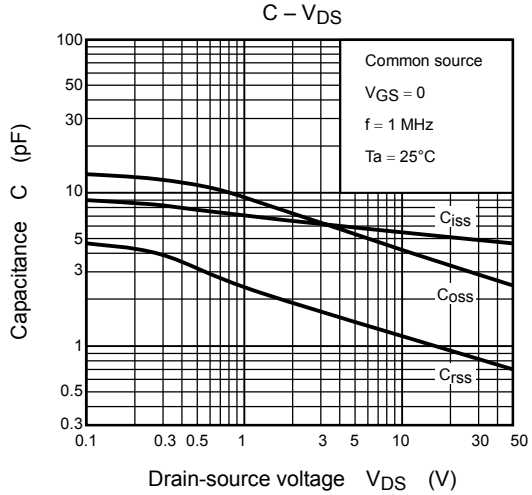
$I_D - V_{GS}$



$|Y_{fs}| - I_D$

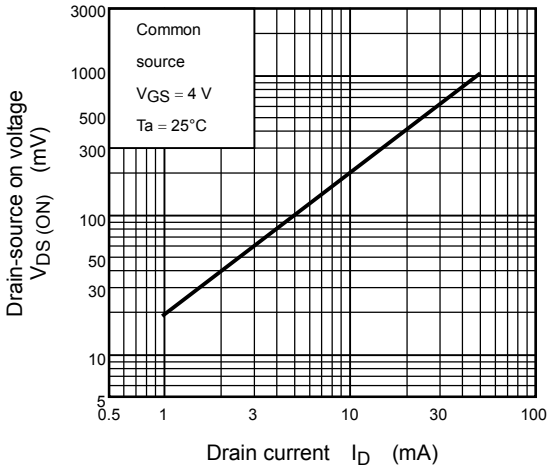


$C - V_{DS}$

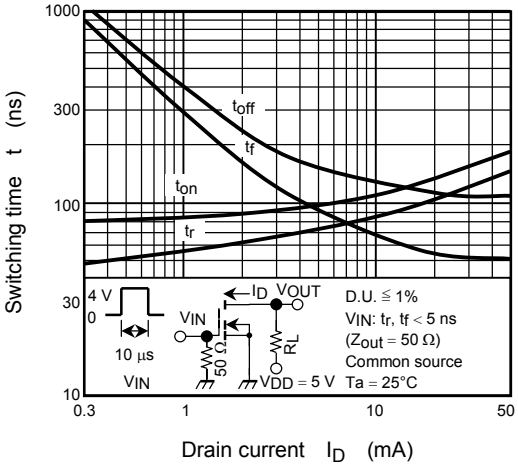


(Q1, Q2 common)

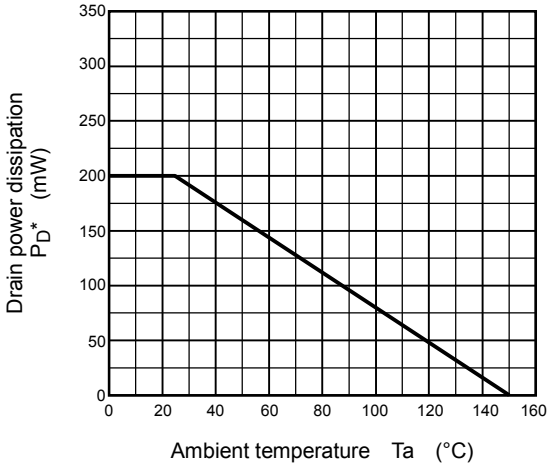
$V_{DS\ (ON)} - I_D$



$t - I_D$



$P_D^* - Ta$



*: TOTAL rating

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