

ADE-203-311A (Z)

HN27C4000G Series

524288-Word × 8-Bit/262144-Word × 16-Bit
CMOS UV Erasable and Programmable ROM

HITACHI

Rev. 1
Nov. 10, 1994

The Hitachi HN27C4000 is a 4-Mbit UV erasable and electrically programmable ROM that is organized either as 524288-word × 8 bit or as 262144-word × 16 bit, featuring extra-high speed burst mode that gives two times faster 4-word or 8-byte serial access than normal. And also high speed and fast programming are served as well as the existing Hitachi 4M device HN27C4096 and HN27C4001. Fabricated on advanced fine process and high speed circuitry technique, HN27C4000 makes high speed access time and low power dissipation in either active or stand-by mode. Therefore, it is suitable for all systems featuring high speed microprocessor such as the 80386, 80486, 68030, 68040 and so on.

Features

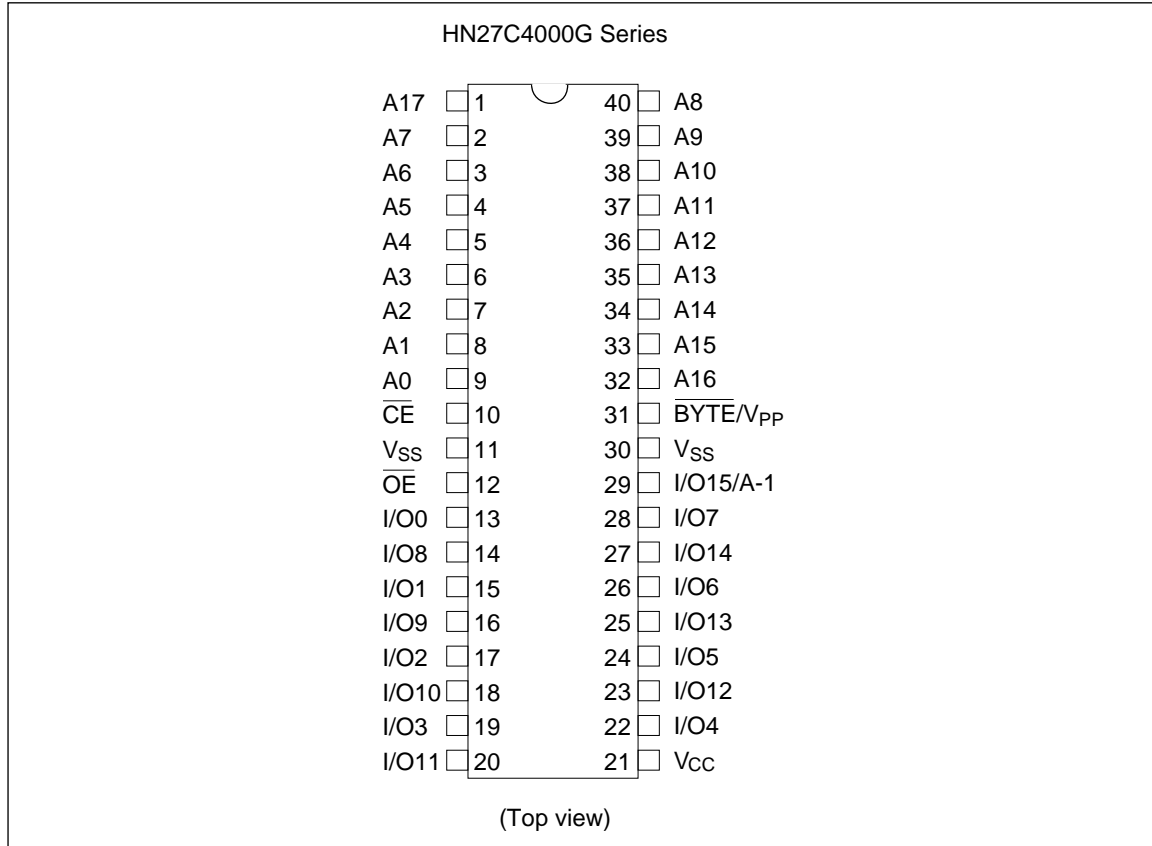
- Organization: 524288-word × 8-bit/262144-word × 16-bit (BYTE/V_{PP} enables selection byte-wide or word-wide)
- High speed: Access time 100 ns/120 ns/150 ns (max)
Burst access time 50 ns/60 ns/60 ns (max)
- Low power dissipation:
Standby mode; 5 μW (typ),
Active mode; 150 mW/MHz (typ)
- Fast high reliability page programming, fast high-reliability programming and option programming: Program voltage; +12.5 V DC
Program time; 3.5 sec (min)
(Theoretical in Page programming)
- Inputs and outputs TTL compatible during both read and program modes
- Pin arrangement: 40-pin EIAJ standard pin compatible with HN62414/HN62434
- Device identifier mode: Manufacturer code and device code



Hitachi

HN27C4000G Series

Pin Arrangement



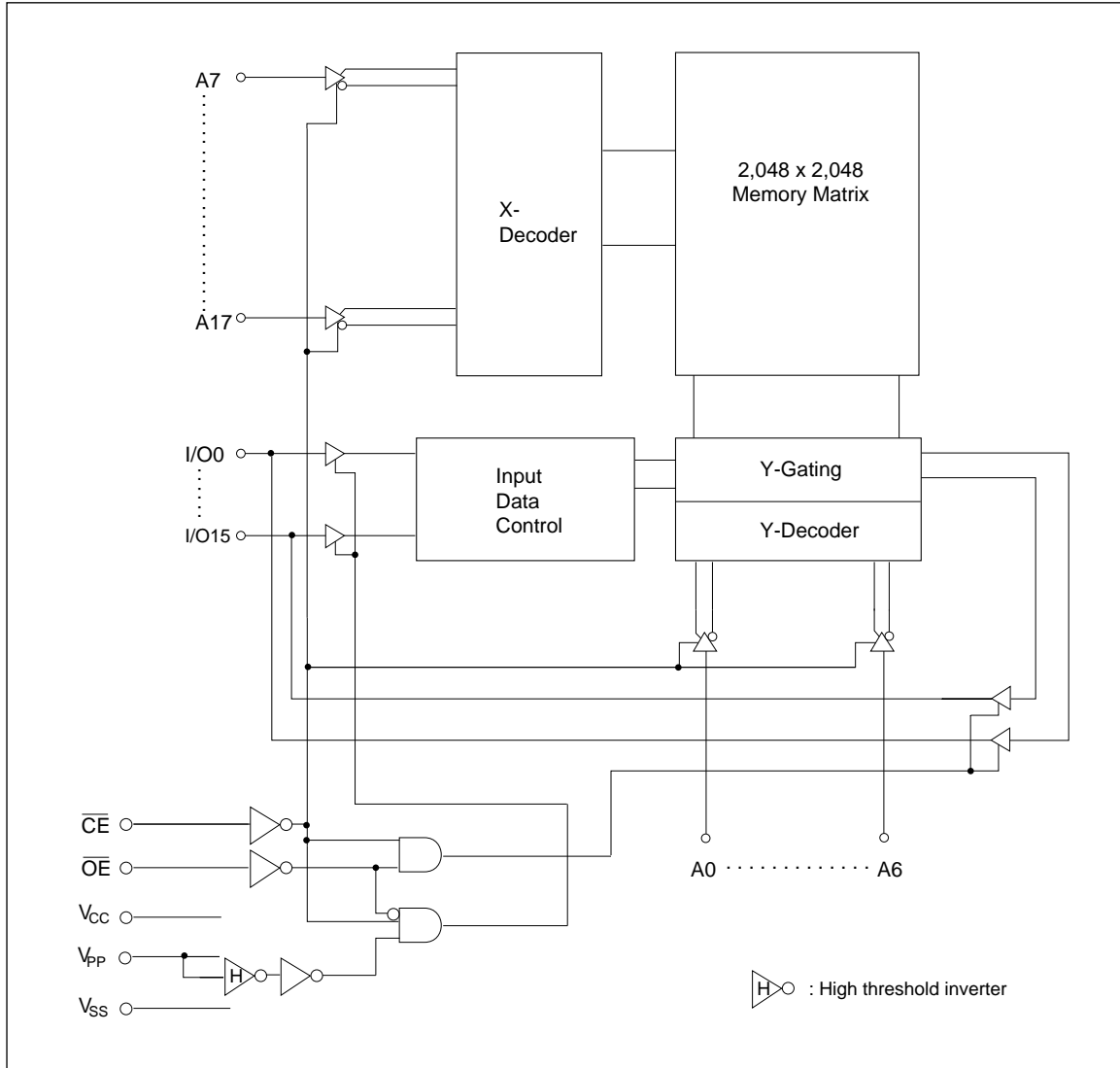
Ordering Information

Type No.	Access time	Package
HN27C4000G-10	100 ns	600-mil
HN27C4000G-12	120 ns	40-pin cerdip
HN27C4000G-15	150 ns	(DG-40A)

Pin Description

Pin name	Function
A0 – A17	Address
I/O0 – I/O14	Input/output
I/O15/A-1	Input/output/address
\overline{CE}	Chip enable
\overline{OE}	Output enable
V _{CC}	Power supply
BYTE/V _{PP}	Byte/word selection/ Programming power supply
V _{SS}	Ground

Block Diagram



Mode Selection

	Pin	\overline{CE}	\overline{OE}	A9	\overline{BYTE}/V_{PP}	V_{CC}	I/O0 – I/O7, I/O8 – I/O14, I/O15/A-1
Mode	DG-40A	(10)	(12)	(39)	(31)	(21)	(13 – 20, 22 – 28, 29)
Read (X16 bit)		V_{IL}	V_{IL}	X	V_{IH}	V_{CC}	Dout Dout Dout
Read (X8 bit)		V_{IL}	V_{IL}	X	V_{IL}	V_{CC}	Dout High-Z V_{IH}/V_{IL}
Output disable (X16 bit)		V_{IL}	V_{IH}	X	V_{IH}	V_{CC}	High-Z High-Z High-Z
Output disable (X8 bit)		V_{IL}	V_{IH}	X	V_{IL}	V_{CC}	High-Z High-Z V_{IH}/V_{IL}

HN27C4000G Series

Mode Selection (cont)

	Pin	\overline{CE}	\overline{OE}	A9	\overline{BYTE}/V_{PP}	V_{CC}	I/O0 – I/O7, I/O8 – I/O14, I/O15/A-1		
Mode	DG-40A	(10)	(12)	(39)	(31)	(21)	(13 – 20, 22 – 28, 29)		
Standby		V_{IH}	X	X	$V_{SS} - V_{CC}$	V_{CC}	High-Z	High-Z	High-Z
Page prog.	Page program set	V_{IH}	V_H^{*2}	X	V_{PP}	V_{CC}	High-Z	High-Z	High-Z
	Page data latch	V_{IL}	V_H^{*2}	X	V_{PP}	V_{CC}	Din	Din	Din
	Page program	V_{IL}	V_{IH}	X	V_{PP}	V_{CC}	High-Z	High-Z	High-Z
	Page program verify	V_{IH}	V_{IL}	X	V_{PP}	V_{CC}	Dout	Dout	Dout
	Page program reset	V_{IH}	V_{IH}	X	V_{CC}	V_{CC}	High-Z	High-Z	High-Z
Word prog.	Program	V_{IL}	V_{IH}	X	V_{PP}	V_{CC}	Din	Din	Din
	Program verify	V_{IH}	V_{IL}	X	V_{PP}	V_{CC}	Dout	Dout	Dout
	Optional verify	V_{IL}	V_{IL}	X	V_{PP}	V_{CC}	Dout	Dout	Dout
	Program inhibit	V_{IH}	V_{IH}	X	V_{PP}	V_{CC}	High-Z	High-Z	High-Z
Identifier		V_{IL}	V_{IL}	V_H^{*2}	$V_{SS} - V_{CC}$	V_{CC}	Code	Code	Code

- Notes: 1. X: Don't care.
2. V_H : 12.0 V \pm 0.5 V

Absolute Maximum Ratings

Item	Symbol	Value	Unit
All input and output voltages ^{*1}	V_{in}, V_{out}	-0.6 ^{*2} to +7.0	V
Voltage on pin A9 and \overline{OE}	V_{ID}	-0.6 ^{*2} to +13.0	V
V_{PP} voltage ^{*1}	V_{PP}	-0.6 to +13.5	V
V_{CC} voltage ^{*1}	V_{CC}	-0.6 to +7.0	V
Operating temperature range	T_{opr}	0 to +70	°C
Storage temperature range ^{*3}	T_{stg}	-65 to +125	°C
Storage temperature under bias	T_{bias}	-20 to +80	°C

- Notes: 1. Relative to V_{SS} .
2. V_{in}, V_{out}, V_{ID} min = -2.0 V for pulse width \leq 20 ns
3. Storage temperature range of device before programming.

HN27C4000G Series

Capacitance (Ta = 25°C, f = 1 MHz)

Item	Symbol	Min	Typ	Max	Unit	Test conditions	Notes
Input capacitance	Cin	—	—	12	pF	Vin = 0 V	Except $\overline{\text{BYTE}}/V_{PP}$
Output capacitance	Cout	—	—	20	pF	Vout = 0 V	

Read Operation

DC Characteristics (VCC = 5 V ± 10%, VPP = VSS to VCC, Ta = 0 to +70°C)

Item	Symbol	Min	Typ	Max	Unit	Test conditions
Input leakage current	ILI	—	—	2	μA	Vin = 5.5 V
Output leakage current	ILO	—	—	2	μA	Vout = 5.5 V/0.45 V
VPP current	I _{PP1}	—	1	20	μA	V _{PP} = 5.5 V
Standby VCC current	ISB1	—	—	1	mA	$\overline{\text{CE}} = V_{IH}$
	ISB2	—	1	20	μA	$\overline{\text{CE}} = V_{CC} \pm 0.3 \text{ V}$
Operating VCC current	I _{CC1}	—	—	35	mA	I _{out} = 0 mA, f = 1 MHz
	I _{CC2}	—	—	120	mA	I _{out} = 0 mA, f = 10 MHz
Input voltage	V _{IL}	-0.3 ^{*1}	—	0.8	V	
	V _{IH}	2.2	—	V _{CC} + 1 ^{*2}	V	
Output voltage	V _{OL}	—	—	0.45	V	I _{OL} = 2.1 mA
	V _{OH}	2.4	—	—	V	I _{OH} = -400 μA

Notes: 1. V_{IL} min = -1.0 V for pulse width ≤ 50 ns

V_{IL} min = -2.0 V for pulse width ≤ 20 ns

2. V_{IH} max = V_{CC} + 1.5 V for pulse width ≤ 20 ns

If V_{IH} is over the specified maximum value, read operation cannot be guaranteed.

HN27C4000G Series

AC Characteristics ($V_{CC} = 5\text{ V} \pm 10\%$, $V_{PP} = V_{SS}$ to V_{CC} , $T_a = 0$ to $+70^\circ\text{C}$)

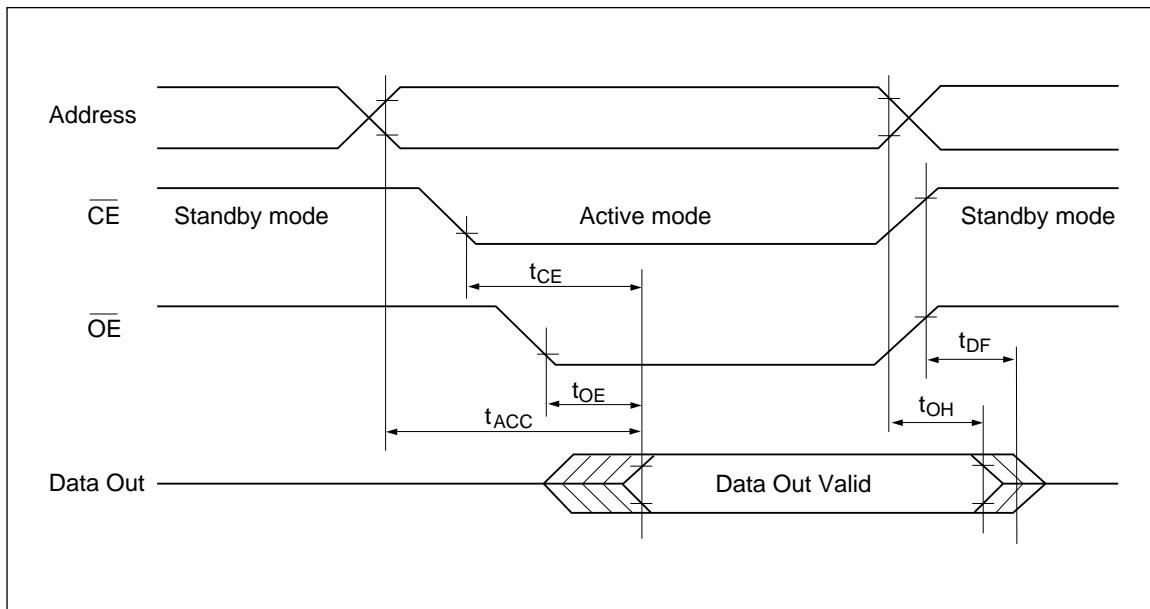
Test Conditions

- Input pulse levels: 0.45 to 2.4 V
- Input rise and fall times: ≤ 10 ns
- Output load: 1 TTL gate +100 pF
- Reference levels for measuring timing: 0.8 V, 2.0 V

Item	Symbol	HN27C4000 -10		HN27C4000 -12		HN27C4000 -15		Unit	Test conditions
		Min	Max	Min	Max	Min	Max		
Address to output delay	t_{ACC}	—	100	—	120	—	150	ns	$\overline{CE} = \overline{OE} = V_{IL}$
\overline{CE} to output delay	t_{CE}	—	100	—	120	—	150	ns	$\overline{OE} = V_{IL}$
\overline{OE} to output delay	t_{OE}	—	60	—	60	—	70	ns	$\overline{CE} = V_{IL}$
Burst address to output delay	t_{BAC}	—	50	—	60	—	60	ns	$\overline{CE} = V_{IL}$
\overline{OE} high to output float **1	t_{DF}	0	35	0	40	0	50	ns	$\overline{CE} = V_{IL}$
Address to output hold	t_{OH}	5	—	5	—	5	—	ns	$\overline{CE} = \overline{OE} = V_{IL}$

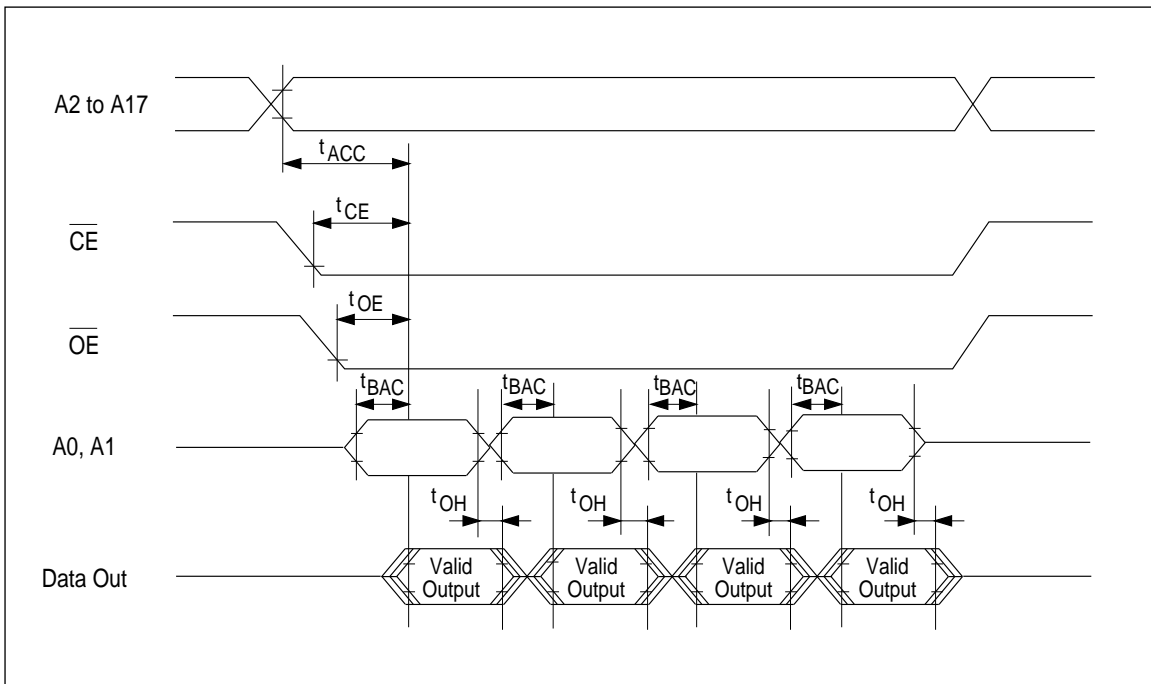
Note: 1. t_{DF} is defined as the time at which the output achieves the open circuit condition and data is no longer driven.

Read Timing Waveform



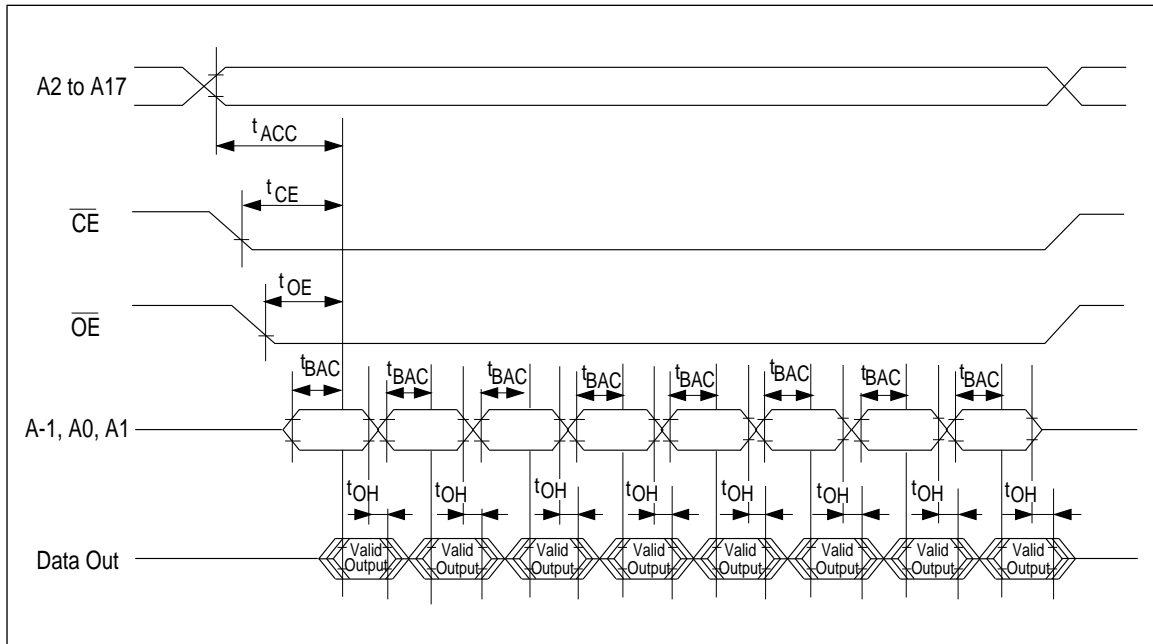
Read Timing Waveform (Burst access mode)

In Burst Access mode, fast read-out of 4 word data is selected by address A0, A1. (Valid only for Read × 16 mode)



HN27C4000G Series

In Burst Access mode, fast read-out of 8 byte data is selected by address A-1, A0, A1. (Valid only for Read \times 8 mode)



Fast High-Reliability Page Programming

This device can be applied the high performance page programming algorithm shown in the following flowchart. This algorithm allows to obtain faster programming time without any voltage stress to the device nor deterioration in reliability of programmed data.

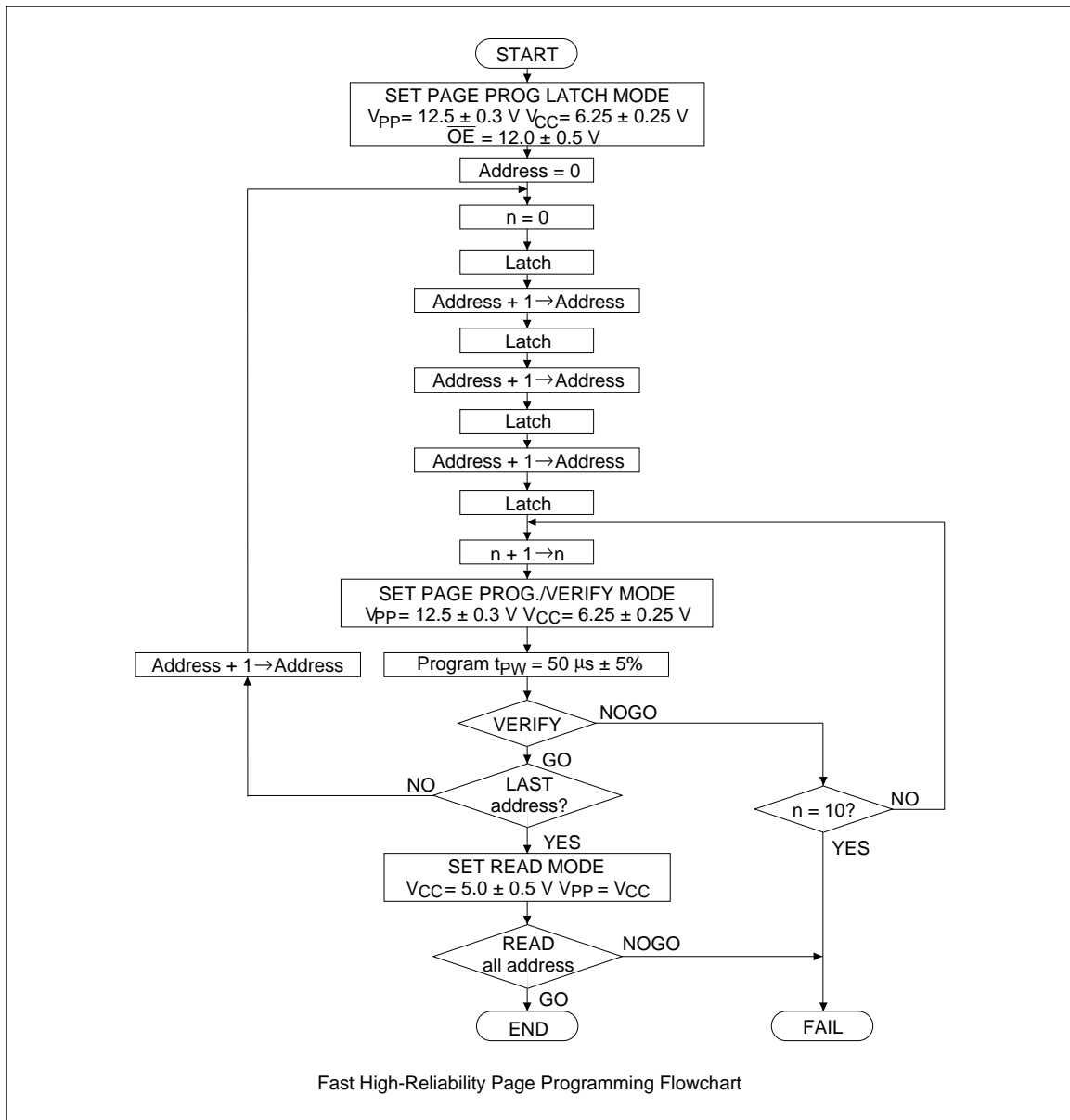
Page Program Set

Apply 12 V to \overline{OE} pin after applying 12.5 V to V_{PP} to set a page program mode.

The device operates in a page program mode until reset.

Page Program Reset

Set V_{PP} to V_{CC} level or less to reset a page program mode.



HN27C4000G Series

DC Characteristics ($V_{CC} = 6.25 \text{ V} \pm 0.25 \text{ V}$, $V_{PP} = 12.5 \text{ V} \pm 0.3 \text{ V}$, $T_a = 25^\circ\text{C} \pm 5^\circ\text{C}$)

Item	Symbol	Min	Typ	Max	Unit	Test conditions
Input leakage current	I_{LI}	—	—	2	μA	$V_{in} = 6.5 \text{ V}/0.45 \text{ V}$
Output voltage during verify	V_{OL}	—	—	0.45	V	$I_{OL} = 2.1 \text{ mA}$
	V_{OH}	2.4	—	—	V	$I_{OH} = -400 \mu\text{A}$
Operating V_{CC} current	I_{CC}	—	—	50	mA	
Input voltage	V_{IL}	-0.1^{*5}	—	0.8	V	
	V_{IH}	2.2	—	$V_{CC} + 0.5^{*6}$	V	
	V_H	11.5	12.0	12.5	V	
V_{PP} supply current	I_{PP}	—	—	70	mA	$\overline{CE} = V_{IL}$

- Notes:
1. V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP} .
 2. V_{PP} must not exceed 13 V including overshoot.
 3. An influence may be had upon device reliability if the device is installed or removed while $V_{PP} = 12.5 \text{ V}$.
 4. Do not alter V_{PP} either V_{IL} to 12.5 V or 12.5 V to V_{IL} when $\overline{CE} = \text{low}$.
 5. $V_{IL} \text{ min} = -0.6 \text{ V}$ for pulse width $\leq 20 \text{ ns}$.
 6. If V_{IH} is over the specified maximum value, programming operation cannot be guaranteed.

HN27C4000G Series

AC Characteristics ($V_{CC} = 6.25 \text{ V} \pm 0.25 \text{ V}$, $V_{PP} = 12.5 \text{ V} \pm 0.3 \text{ V}$, $T_a = 25^\circ\text{C} \pm 5^\circ\text{C}$)

Test Conditions

- Input pulse levels: 0.45 to 2.4 V
- Input rise and fall times: $\leq 20 \text{ ns}$
- Reference levels for measuring timing: Inputs; 0.8 V, 2.0 V,
Outputs; 0.8 V, 2.0 V

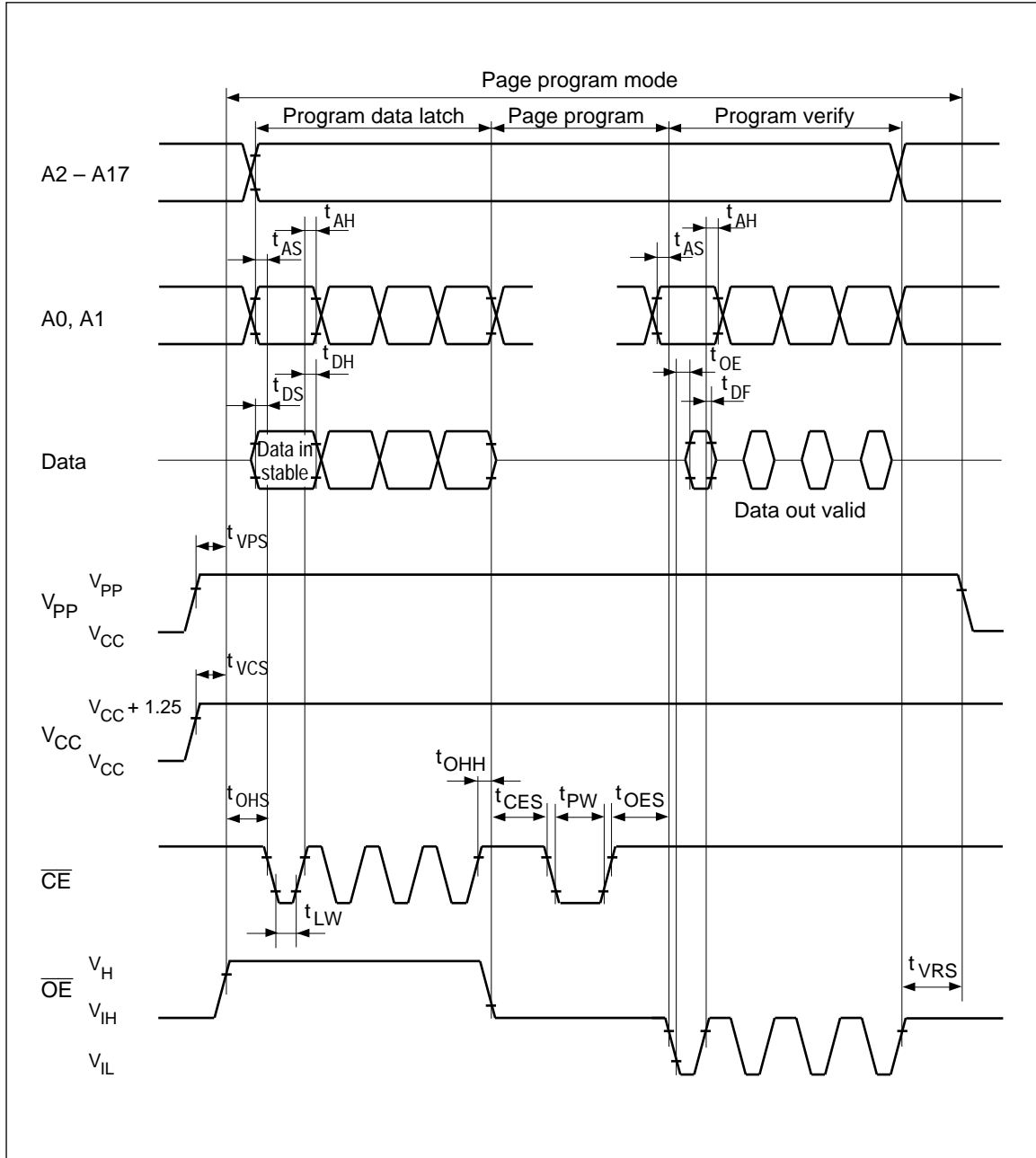
Item	Symbol	Min	Typ	Max	Unit	Test conditions
Address setup time	t_{AS}	2	—	—	μs	
\overline{OE} setup time	t_{OES}	2	—	—	μs	
Data setup time	t_{DS}	2	—	—	μs	
Address hold time	t_{AH}	0	—	—	μs	
Data hold time	t_{DH}	2	—	—	μs	
\overline{OE} high to output float delay	t_{DF}^{*1}	0	—	130	ns	
V_{PP} setup time	t_{VPS}	2	—	—	μs	
V_{CC} setup time	t_{VCS}	2	—	—	μs	
\overline{CE} initial programming pulse width	t_{PW}	47.5	50.0	52.5	μs	
\overline{CE} setup time	t_{CES}	2	—	—	μs	
Data valid from \overline{OE}	t_{OE}	0	—	150	ns	
\overline{CE} pulse width during data latch	t_{LW}	1	—	—	μs	
$\overline{OE} = V_H$ setup time	t_{OHS}	2	—	—	μs	
$\overline{OE} = V_H$ hold time	t_{OHH}	2	—	—	μs	
V_{PP} hold time ^{*2}	t_{VRS}	1	—	—	μs	

Notes: 1. t_{DF} is defined as the time at which the output achieves the open circuit condition and data is no longer driven.

2. Page program mode will be reset when V_{PP} is set to V_{CC} or less.

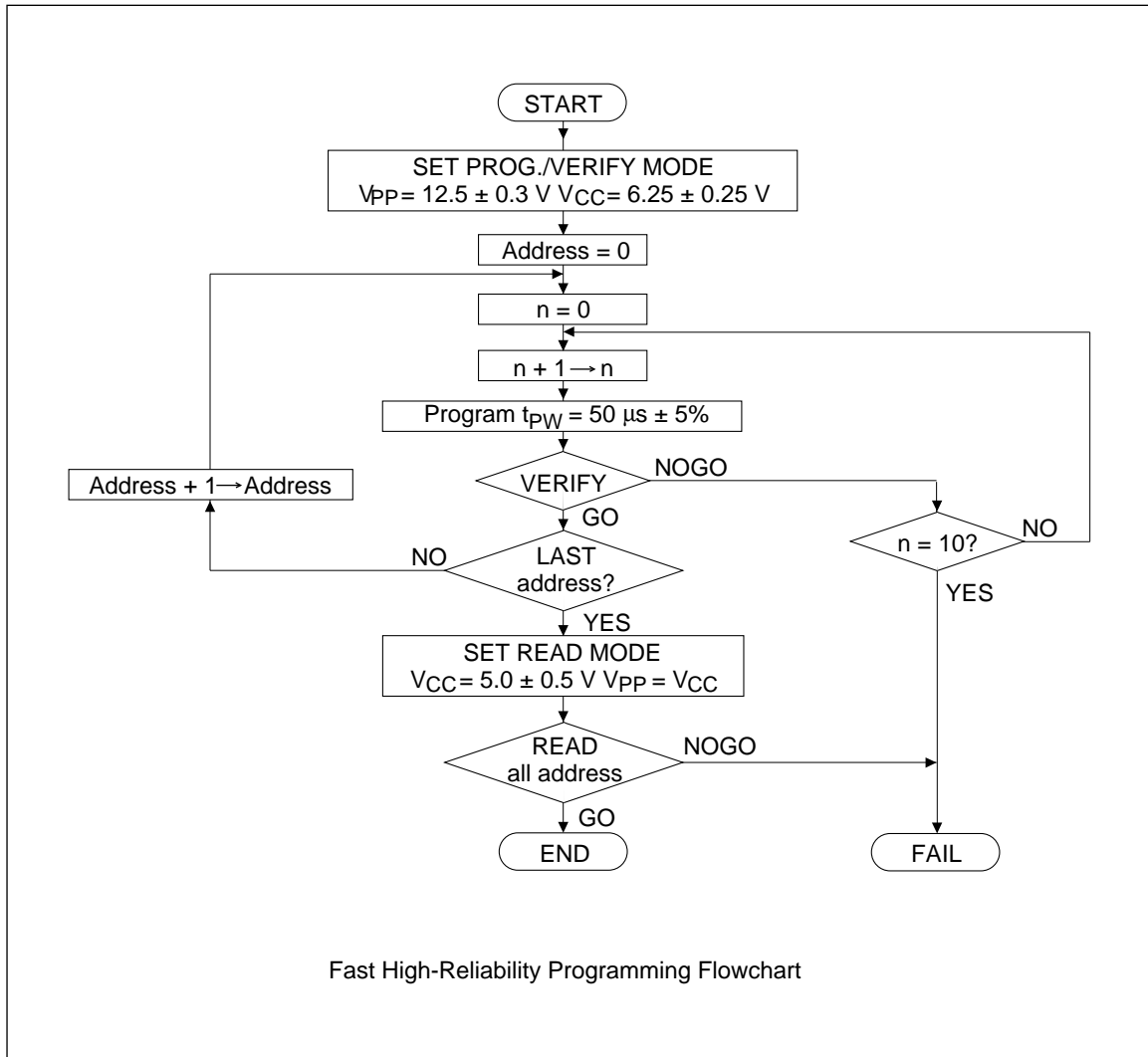
HN27C4000G Series

Fast High-Reliability Page Programming Timing Waveform



Fast High-Reliability Programming

This device can be applied the fast high-reliability programming algorithm shown in the following flowchart. This algorithm allows to obtain faster programming time without any voltage stress to the device nor deterioration in reliability of programmed data.



HN27C4000G Series

DC Characteristics ($V_{CC} = 6.25 \text{ V} \pm 0.25 \text{ V}$, $V_{PP} = 12.5 \text{ V} \pm 0.3 \text{ V}$, $T_a = 25^\circ\text{C} \pm 5^\circ\text{C}$)

Item	Symbol	Min	Typ	Max	Unit	Test conditions
Input leakage current	I_{LI}	—	—	2	μA	$V_{in} = 6.5 \text{ V}/0.45 \text{ V}$
V_{PP} supply current	I_{PP}	—	—	40	mA	$\overline{CE} = V_{IL}$
Operating V_{CC} current	I_{CC}	—	—	50	mA	
Input voltage	V_{IL}	-0.1^{*5}	—	0.8	V	
	V_{IH}	2.2	—	$V_{CC} + 0.5^{*6}$	V	
Output voltage	V_{OL}	—	—	0.45	V	$I_{OL} = 2.1 \text{ mA}$
	V_{OH}	2.4	—	—	V	$I_{OH} = -400 \mu\text{A}$

- Notes: 1. V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP} .
 2. V_{PP} must not exceed 13 V including overshoot.
 3. An influence may be had upon device reliability if the device is installed or removed while $V_{PP} = 12.5 \text{ V}$.
 4. Do not alter V_{PP} either V_{IL} to 12.5 V or 12.5 V to V_{IL} when $\overline{CE} = \text{low}$.
 5. V_{IL} min = -0.6 V for pulse width $\leq 20 \text{ ns}$.
 6. If V_{IH} is over the specified maximum value, programming operation cannot be guaranteed.

AC Characteristics ($V_{CC} = 6.25 \text{ V} \pm 0.25 \text{ V}$, $V_{PP} = 12.5 \text{ V} \pm 0.3 \text{ V}$, $T_a = 25^\circ\text{C} \pm 5^\circ\text{C}$)

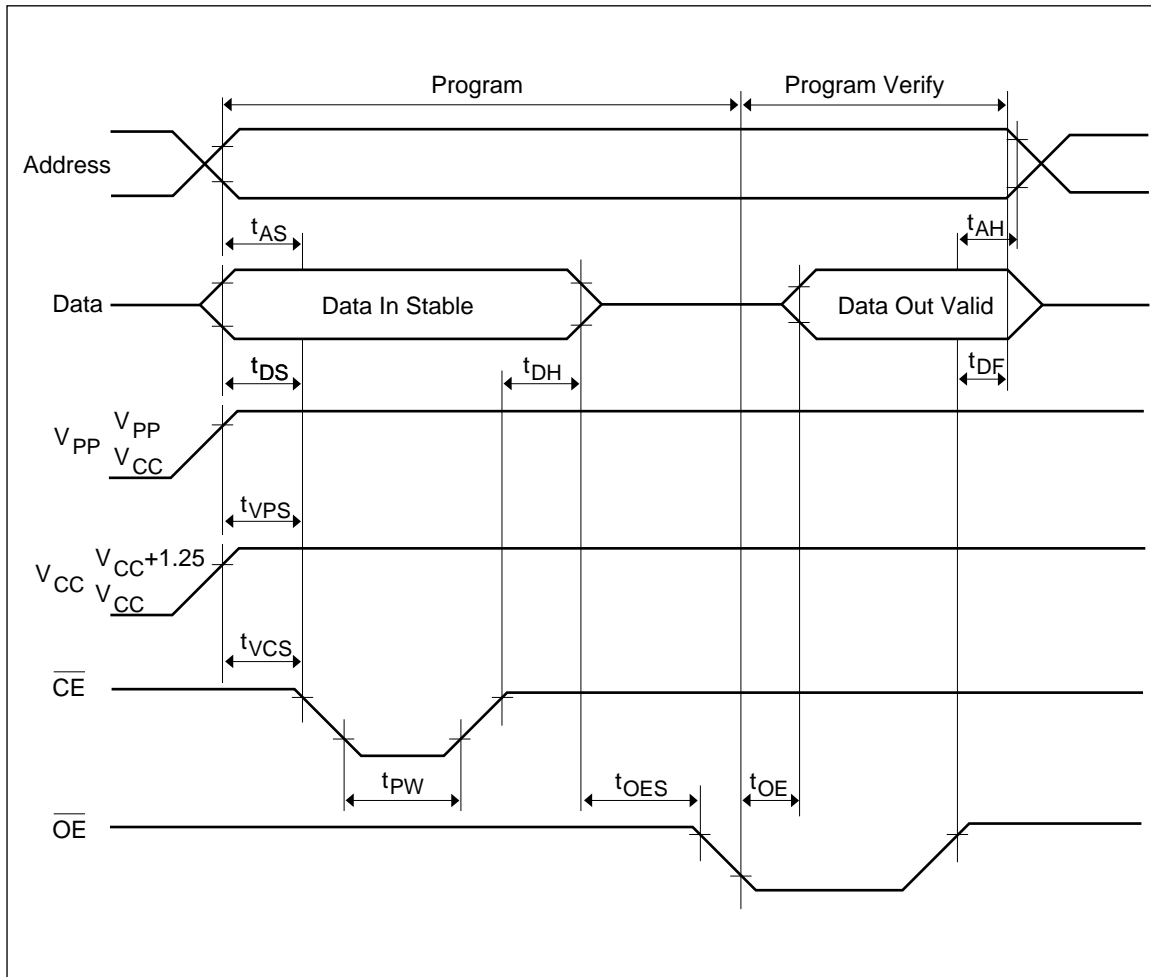
Test Conditions

- Input pulse levels: 0.45 to 2.4 V
- Input rise and fall times: $\leq 20 \text{ ns}$
- Reference levels for measuring timings: 0.8 V, 2.0 V

Item	Symbol	Min	Typ	Max	Unit	Test conditions
Address setup time	t_{AS}	2	—	—	μs	
\overline{OE} setup time	t_{OES}	2	—	—	μs	
Data setup time	t_{DS}	2	—	—	μs	
Address hold time	t_{AH}	0	—	—	μs	
Data hold time	t_{DH}	2	—	—	μs	
\overline{OE} to output float delay	t_{DF}^{*1}	0	—	130	ns	
V_{PP} setup time	t_{VPS}	2	—	—	μs	
V_{CC} setup time	t_{VCS}	2	—	—	μs	
\overline{CE} initial programming pulse width	t_{PW}	47.5	50.0	52.5	μs	
Data valid from \overline{OE}	t_{OE}	0	—	150	ns	

- Note: 1. t_{DF} is defined as the time at which the output achieves the open circuit condition and data is no longer driven.

Fast High-Reliability Programming Timing Waveform



Optional Page Programming

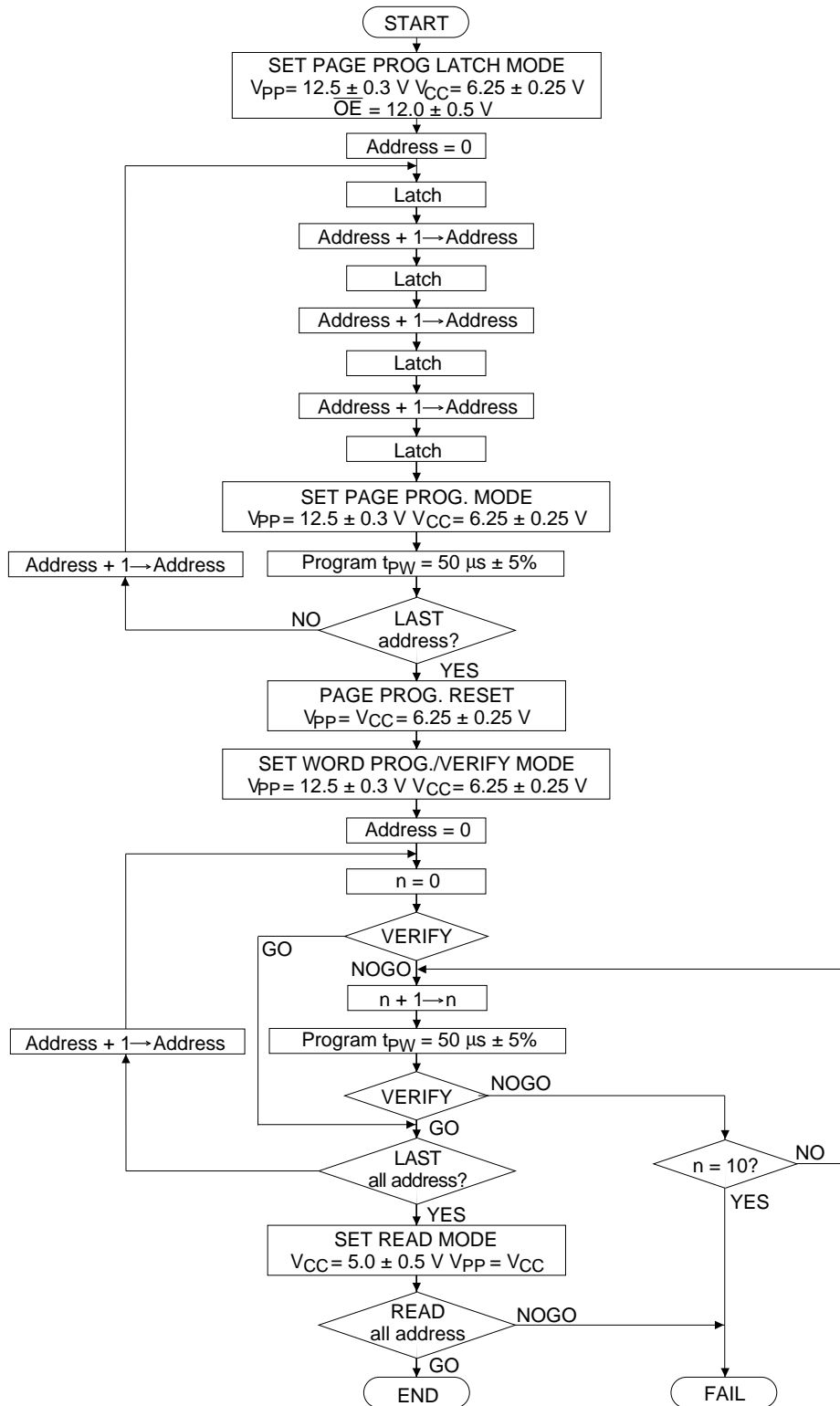
This device can be applied the optional page programming algorithm shown in the following flowchart. This algorithm allows to obtain faster programming time without any voltage stress to the device nor deterioration in reliability of programmed data.

This programming algorithm is the combination of page programming and word verify. It can avoid

the increase of programming verify time when a programmer with slow machine cycle is used, and shorten the total programming time.

Regarding the timing specifications for page programming and word verify, please refer to the specifications for fast high-reliability page programming and fast high-reliability programming.

HN27C4000G Series



Optional Page Programming Flowchart

HN27C4000G Series

DC Characteristics ($V_{CC} = 6.25 \text{ V} \pm 0.25 \text{ V}$, $V_{PP} = 12.5 \text{ V} \pm 0.3 \text{ V}$, $T_a = 25^\circ\text{C} \pm 5^\circ\text{C}$)

Item	Symbol	Min	Typ	Max	Unit	Test conditions
Input leakage current	I_{LI}	—	—	2	μA	$V_{in} = 6.5 \text{ V}/0.45 \text{ V}$
Output voltage during verify	V_{OL}	—	—	0.45	V	$I_{OL} = 2.1 \text{ mA}$
	V_{OH}	2.4	—	—	V	$I_{OH} = -400 \mu\text{A}$
Operating V_{CC} current	I_{CC}	—	—	50	mA	
Input voltage	V_{IL}	-0.1^{*5}	—	0.8	V	
	V_{IH}	2.2	—	$V_{CC} + 0.5^{*6}$	V	
	V_H	11.5	12.0	12.5	V	
V_{PP} supply current	I_{PP}	—	—	70	mA	$\overline{CE} = V_{IL}$

- Notes:
- V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP} .
 - V_{PP} must not exceed 13 V including overshoot.
 - An influence may be had upon device reliability if the device is installed or removed while $V_{PP} = 12.5 \text{ V}$.
 - Do not alter V_{PP} either V_{IL} to 12.5 V or 12.5 V to V_{IL} when $\overline{CE} = \text{low}$.
 - V_{IL} min = -0.6 V for pulse width $\leq 20 \text{ ns}$.
 - If V_{IH} is over the specified maximum value, programming operation cannot be guaranteed.

HN27C4000G Series

AC Characteristics ($V_{CC} = 6.25 \text{ V} \pm 0.25 \text{ V}$, $V_{PP} = 12.5 \text{ V} \pm 0.3 \text{ V}$, $T_a = 25^\circ\text{C} \pm 5^\circ\text{C}$)

Test Conditions

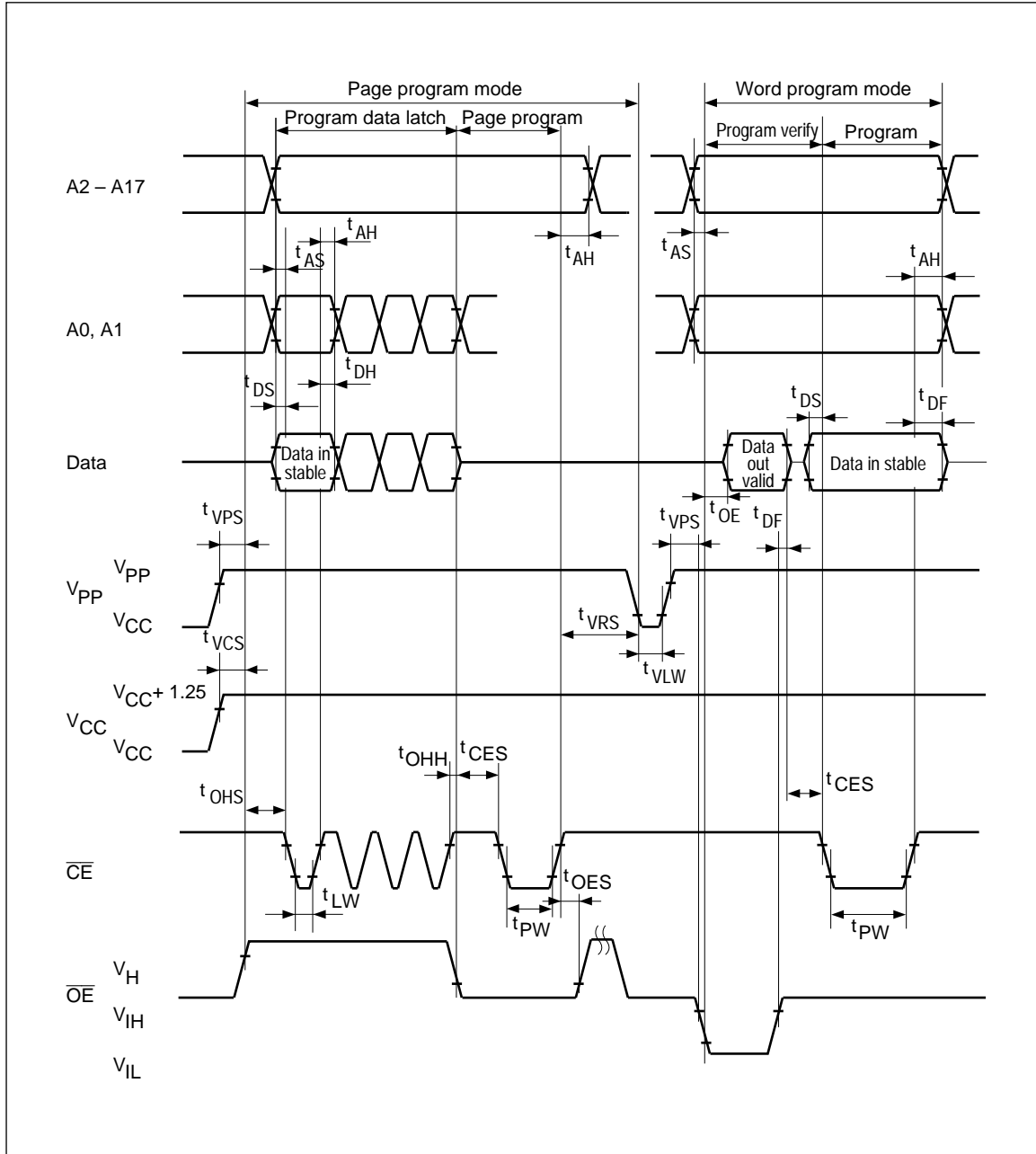
- Input pulse levels: 0.45 to 2.4 V
- Input rise and fall times: $\leq 20 \text{ ns}$
- Reference levels for measuring timings: Inputs; 0.8 V, 2.0 V
Outputs; 0.8 V, 2.0 V

Item	Symbol	Min	Typ	Max	Unit	Test conditions
Address setup time	t_{AS}	2	—	—	μs	
\overline{OE} setup time	t_{OES}	2	—	—	μs	
Data setup time	t_{DS}	2	—	—	μs	
Address hold time	t_{AH}	0	—	—	μs	
Data hold time	t_{DH}	2	—	—	μs	
\overline{OE} high to output float delay	t_{DF}^{*1}	0	—	130	ns	
V_{PP} setup time	t_{VPS}	2	—	—	μs	
V_{CC} setup time	t_{VCS}	2	—	—	μs	
\overline{CE} initial programming pulse width	t_{PW}	47.5	50.0	52.5	μs	
\overline{CE} setup time	t_{CES}	2	—	—	μs	
Data valid from \overline{OE}	t_{OE}	0	—	150	ns	
\overline{CE} pulse width during data latch	t_{LW}	1	—	—	μs	
$\overline{OE} = V_H$ setup time	t_{OHS}	2	—	—	μs	
$\overline{OE} = V_H$ hold time	t_{OHH}	2	—	—	μs	
Page programming reset time ^{*2}	t_{VLW}	1	—	—	μs	
V_{PP} hold time ^{*2}	t_{VRS}	1	—	—	μs	

Notes: 1. t_{DF} is defined as the time at which the output achieves the open circuit condition and data is no longer driven.

2. Page program mode will be reset when V_{PP} is set to V_{CC} or less.

Option Page Programming Timing Waveform



HN27C4000G Series

Erase

Erasure of this device is performed by exposure to ultraviolet light of 2537 Å and all the output data are changed to “1” after this erasure procedure. The minimum integrated dose (i.e. UV intensity X exposure time) for erasure is 15 W•sec/cm².

Mode Description

Device Identifier Mode

The device identifier mode allows the reading out of binary codes that identify manufacturer and type of device, from outputs of EPROM. By this mode, the device will be automatically matched its own corresponding programming algorithm, using programming equipment.

HN27C4000G Identifier Code

Identifier	A0	I/O8 – I/O15	I/O7	I/O6	I/O5	I/O4	I/O3	I/O2	I/O1	I/O0	Hex Data
Manufacturer code	DG-40 (9) V _{IL}	— X	(28) 0	(26) 0	(24) 0	(22) 0	(19) 0	(17) 1	(15) 1	(13) 1	07
Device code	V _{IH}	X	1	0	1	0	0	0	0	1	A1

- Notes:
1. V_{CC} = 5.0 V ± 10%
 2. A9 = 12.0 V ± 0.5 V
 3. \overline{CE} , \overline{OE} = V_{IL}
 4. A1 – A8, A10 – A17: Don't care.
 5. X: Don't care.