FAIRCHILD SEMICONDUCTOR®

Data Sheet December 2001

10A, 30V, 0.0135 Ohm, Single N-Channel, Logic Level Power MOSFET

This power MOSFET is manufactured using an innovative process. This advanced process technology achieves the lowest possible on-resistance per silicon area, resulting in outstanding performance. This device is capable of withstanding high energy in the avalanche mode and the diode exhibits very low reverse recovery time and stored charge. It was designed for use in applications where power efficiency is important, such as switching regulators, switching converters, motor drivers, relay drivers, low-voltage bus switches, and power management in portable and battery-operated products.

Ordering Information

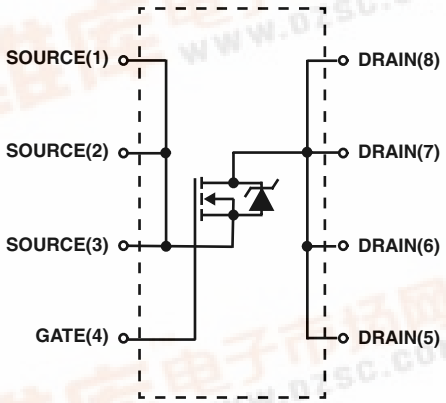
PART NUMBER	PACKAGE	BRAND
HP4410DY	SO-8	P4410DY

NOTE: When ordering, use the entire part number. Add the suffix T to obtain the variant in tape and reel, e.g., HP4410DYT.

Features

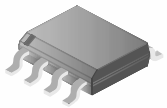
- Logic Level Gate Drive
- 10A, 30V
- $r_{DS(ON)}$ = 0.0135Ω at I_D = 10A, V_{GS} = 10V
- $r_{DS(ON)}$ = 0.020Ω at I_D = 8A, V_{GS} = 4.5V
- Related Literature
  - TB334, “Guidelines for Soldering Surface Mount Components to PC Boards”

Symbol



Packaging

SO-8



Absolute Maximum Ratings $T_A = 25^oC$, Unless Otherwise Specified

		HP4410DY	UNITS
Drain to Source Voltage (Note 1)	V_{DSS}	30	V
Drain to Gate Voltage (R_{GS} = 20kΩ) (Note 1)	V_{DGR}	30	V
Gate to Source Voltage	V_{GS}	±16	V
Drain Current			
Continuous	I_D	10	A
Pulsed Drain Current (10μs Pulse Width)	I_{DM}	50	A
Power Dissipation	P_D	2.5	W
Derate Above 25°C		0.02	W/°C
Operating and Storage Temperature	T_J, T_{STG}	-55 to 150	°C
Maximum Temperature for Soldering			
Leads at 0.063in (1.6mm) from Case for 10s	T_L	300	°C
Package Body for 10s, See Techbrief 334	T_{pkg}	260	°C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

1. $T_A = 25^oC$ to 125^oC.

Electrical Specifications $T_A = 25^oC$, Unless Otherwise Specified

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Drain to Source Breakdown Voltage	BV_{DSS}	I_D = 250μA, V_{GS} = 0V	30	-	-	V
Gate to Source Threshold Voltage	$V_{GS(TH)}$	V_{GS} = V_{DS}, I_D = 250μA (Figure 9)	1	-	-	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 30V, V_{GS} = 0V	-	-	1	μA
		V_{DS} = 30V, V_{GS} = 0V, $T_A = 55^oC$	-	-	25	μA
Gate to Source Leakage Current	I_{GSS}	V_{GS} = ±16V	-	-	100	nA
Drain to Source On Resistance	$r_{DS(ON)}$	I_D = 8A, V_{GS} = 4.5V (Figures 6, 8)	-	0.015	0.020	Ω
		I_D = 10A, V_{GS} = 10V (Figures 6, 8)	-	0.011	0.0135	Ω
Turn-On Delay Time	$t_{d(ON)}$	V_{DD} = 25V, $I_D \cong$ 1A, R_L = 25Ω, V_{GEN} = 10V, R_{GS} = 6Ω	-	15	30	ns
Rise Time	t_r		-	9	20	ns
Turn-Off Delay Time	$t_{d(OFF)}$		-	70	100	ns
Fall Time	t_f		-	20	80	ns
Total Gate Charge	$Q_{g(TOT)}$	V_{DS} = 15V, V_{GS} = 10V, $I_D \cong$ 10A	-	35	60	nC
Gate to Source Charge	Q_{gs}		-	7.5	-	nC
Gate to Drain Charge	Q_{gd}		-	5.8	-	nC
Input Capacitance	C_{ISS}	V_{DS} = 25V, V_{GS} = 0V, f = 1MHz (Figure 4)	-	1600	-	pF
Output Capacitance	C_{OSS}		-	685	-	pF
Reverse Transfer Capacitance	C_{RSS}		-	115	-	pF
Thermal Resistance Junction to Ambient	$R_{\theta JA}$	Pulse Width < 10s (Figure 11) Device Mounted on FR-4 Material	-	-	50	°C/W

Source to Drain Diode Specifications

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Source to Drain Diode Voltage	V_{SD}	I_{SD} = 2.3A (Figure 7)	-	0.75	1.1	V
Reverse Recovery Time	t_{rr}	I_{SD} = 2.3A, dI_{SD}/dt = 100A/μs	-	50	80	ns

Typical Performance Curves Unless Otherwise Specified

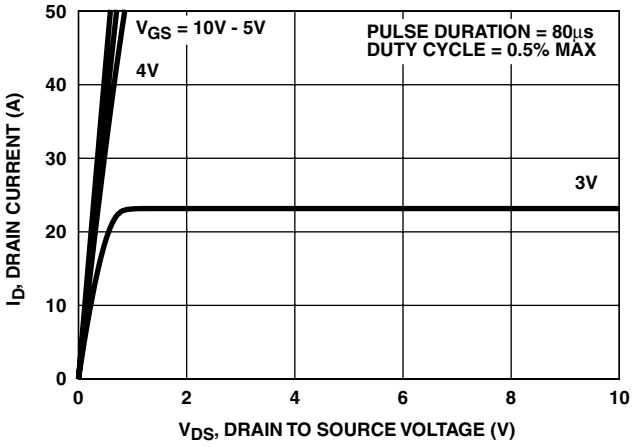


FIGURE 1. OUTPUT CHARACTERISTICS

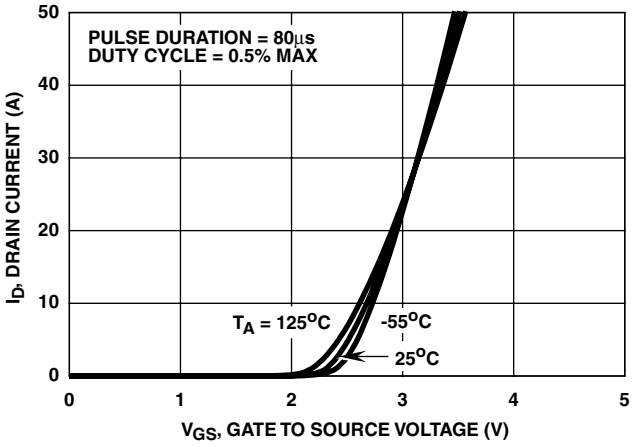


FIGURE 2. TRANSFER CHARACTERISTICS

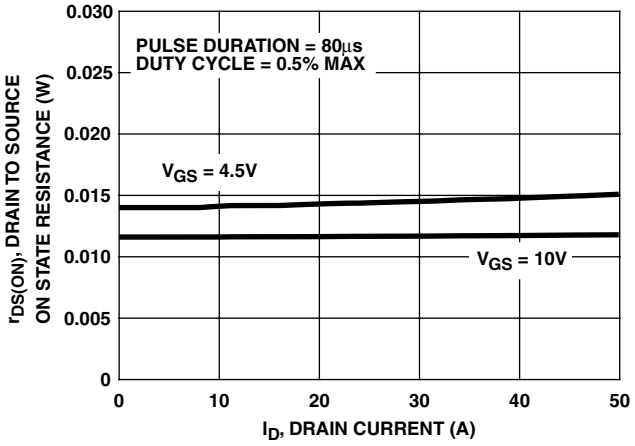


FIGURE 3. DRAIN TO SOURCE ON RESISTANCE vs GATE VOLTAGE AND DRAIN CURRENT

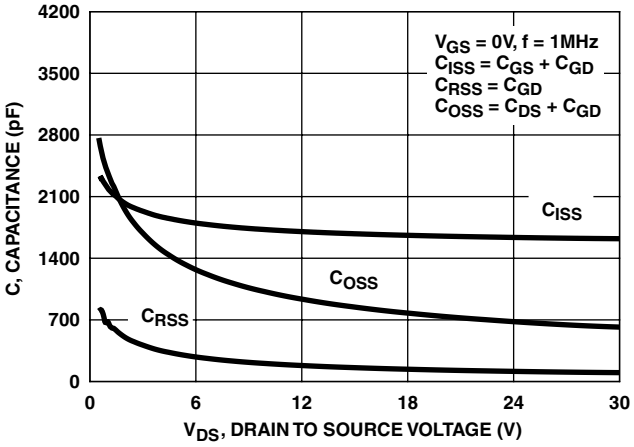


FIGURE 4. CAPACITANCE vs DRAIN TO SOURCE VOLTAGE

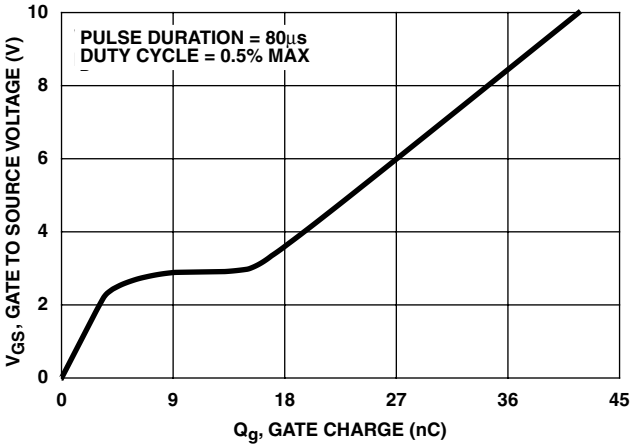


FIGURE 5. GATE TO SOURCE VOLTAGE vs GATE CHARGE

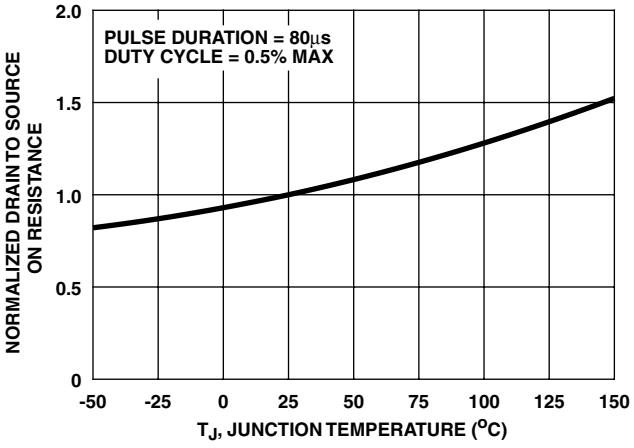


FIGURE 6. NORMALIZED DRAIN TO SOURCE ON RESISTANCE vs JUNCTION TEMPERATURE

Typical Performance Curves Unless Otherwise Specified (Continued)

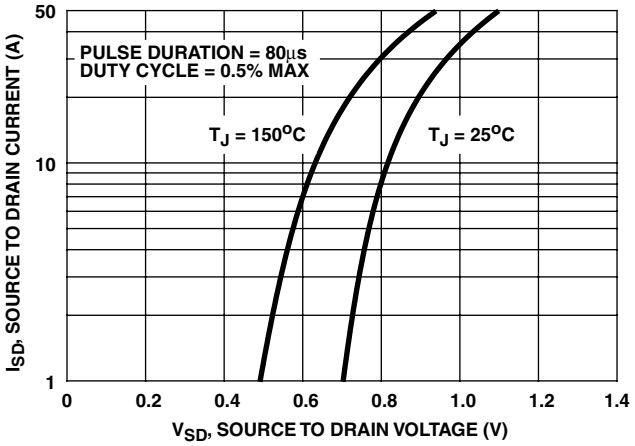


FIGURE 7. SOURCE TO DRAIN DIODE VOLTAGE

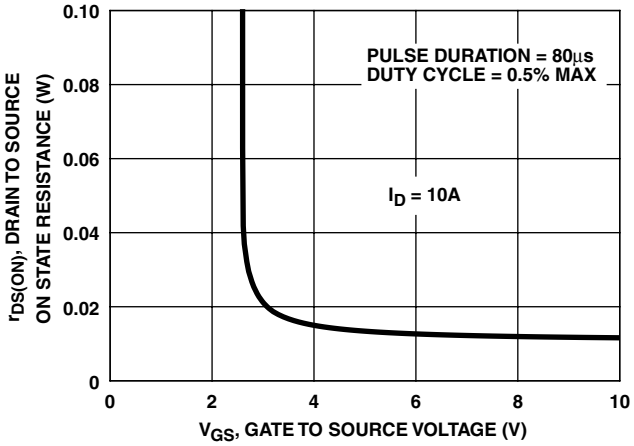


FIGURE 8. DRAIN TO SOURCE ON RESISTANCE vs GATE TO SOURCE VOLTAGE

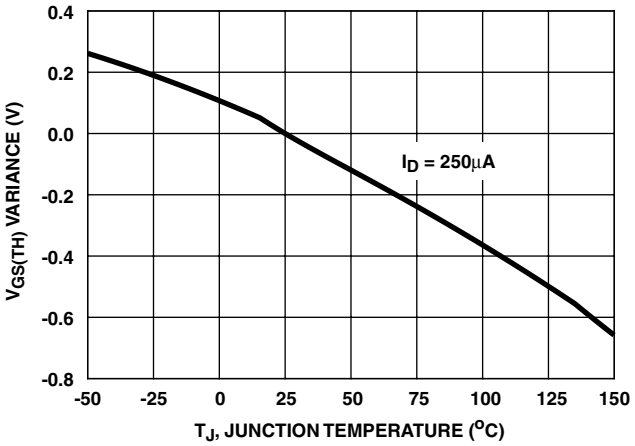


FIGURE 9. GATE THRESHOLD VOLTAGE VARIANCE vs JUNCTION TEMPERATURE

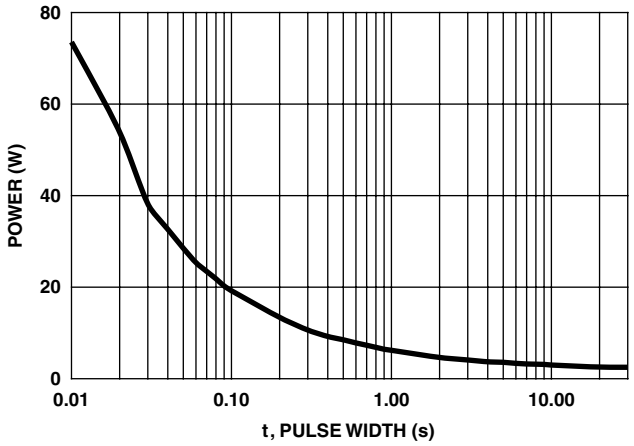


FIGURE 10. SINGLE PULSE POWER CAPABILITY vs PULSE WIDTH

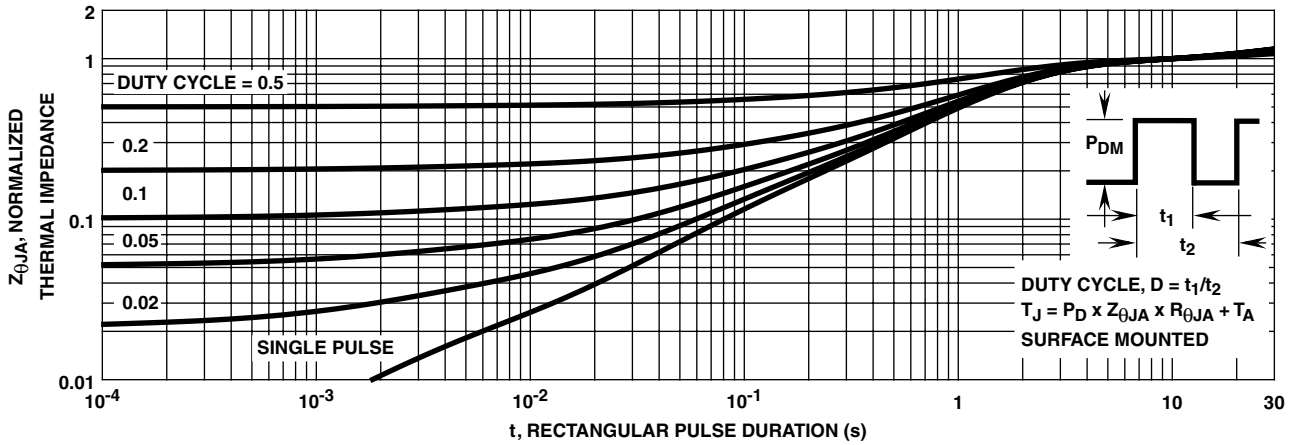


FIGURE 11. NORMALIZED MAXIMUM TRANSIENT THERMAL IMPEDANCE

Test Circuits and Waveforms

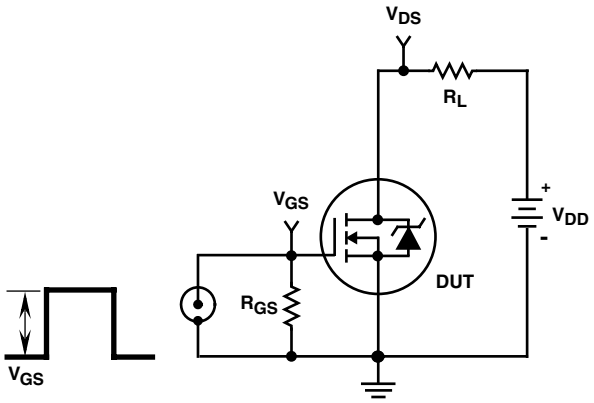


FIGURE 12. SWITCHING TIME TEST CIRCUIT

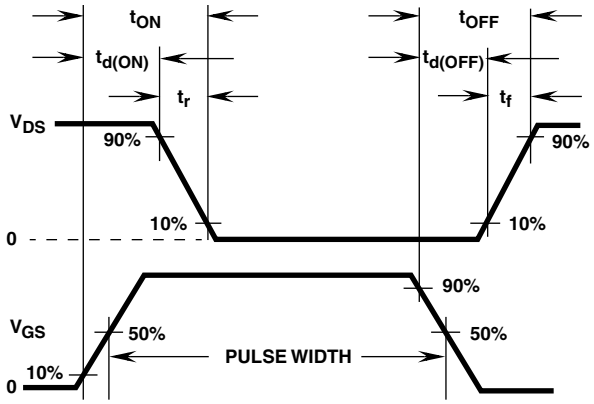


FIGURE 13. SWITCHING TIME WAVEFORM

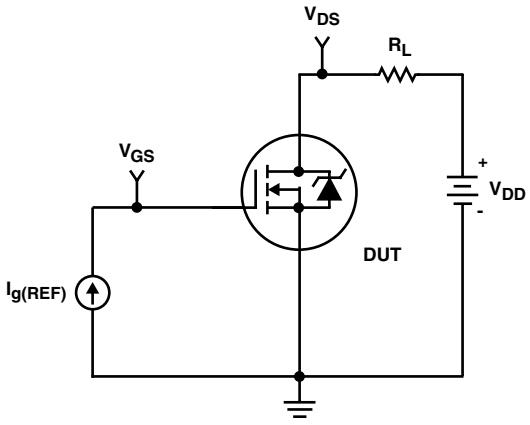


FIGURE 14. GATE CHARGE TEST CIRCUIT

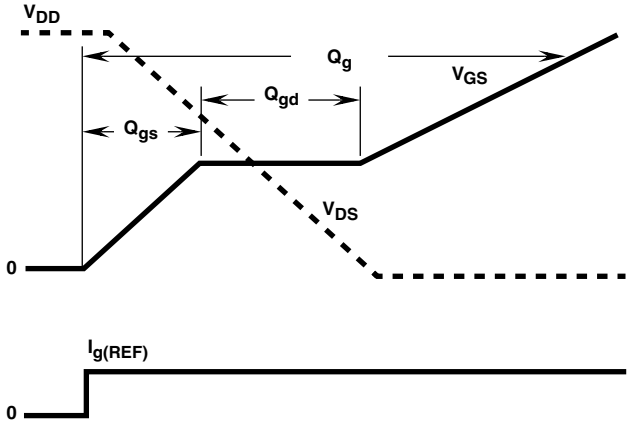


FIGURE 15. GATE CHARGE WsAVEFORMS

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