Radiation Hardened 8K x 8 CMOS PROM

Intersil's Satellite Applications Flow™ (SAF) devices are fully tested and guaranteed to 100kRAD total dose. These QML Class T devices are processed to a standard flow intended to meet the cost and shorter lead-time needs of large volume satellite manufacturers, while maintaining a high level of reliability.

The Intersil HS-6664RH-T is a radiation hardened 64K CMOS PROM, organized in an 8K word by 8-bit format. The chip is manufactured using a radiation hardened CMOS process, and utilizes synchronous circuit design techniques to achieve high speed performance with very low power dissipation.

On-chip address latches are provided, allowing easy interfacing with microprocessors that use a multiplexed address/data bus structure. The output enable control ($\overline{G}$) simplifies system interfacing by allowing output data bus control in addition to the chip enable control ($\overline{E}$). All bits are manufactured storing a logical "0" and can be selectively programmed for a logical "1" at any bit location.

Specifications

Specifications for Rad Hard QML devices are controlled by the Defense Supply Center in Columbus (DSCC). The SMD numbers listed below must be used when ordering.

Detailed Electrical Specifications for the HS-666s4RH-T are contained in SMD 5962-95626. A "hot-link" is provided from our website for downloading.
www.intersil.com/spacedefense/newsafclasst.asp

Intersil's Quality Management Plan (QM Plan), listing all Class T screening operations, is also available on our website.
www.intersil.com/quality/manuals.asp

Ordering Information

ORDERING INFORMATION	PART NUMBER	TEMP. RANGE (^oC)
5962R9562601TXC	HS1-6664RH-T	-55 to 125
HS1-6664RH/Proto	HS1-6664RH/Proto	-55 to 125
5962R9562601TYC	HS9-6664RH-T	-55 to 125
HS9-6664RH/Proto	HS9-6664RH/Proto	-55 to 125

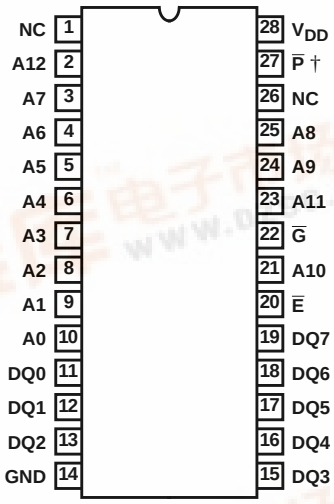
NOTE: ***Minimum order quantity for -T is 150 units through distribution, or 450 units direct.***

Features

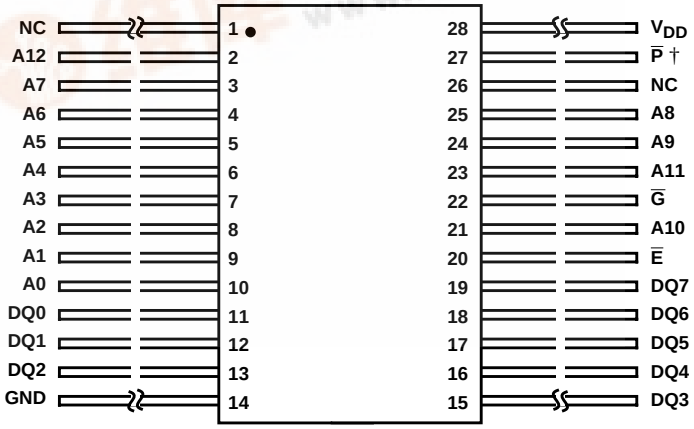
- QML Class T, Per MIL-PRF-38535
- Radiation Performance
  - Gamma Dose (γ) 1 x 10^5 RAD(Si)
  - No Latch-Up, SEU LET >100MeV/mg/cm^2
- Transient Output Upset >5 x 10^8 RAD (Si)/s
- Fast Access Time - 35ns (Typical)
- Single 5V Power Supply, Synchronous Operation
- Single Pulse 10V Field Programmable NiCr Fuses
- On-Chip Address Latches, Three-State Outputs
- Low Standby Current <500µA (Pre-Rad)
- Low Operating Current <15mA/MHz

Pinouts

HS1-6664RH-T (SBDIP), CDIP2-T28
TOP VIEW

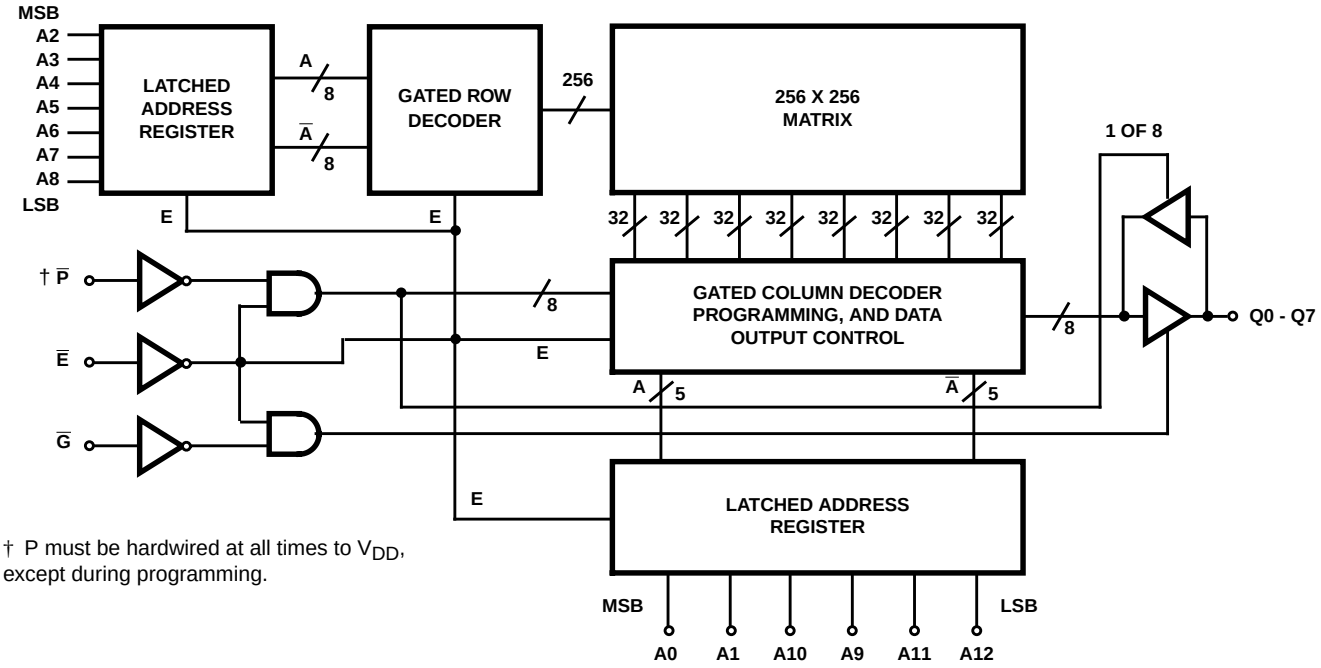


HS9-6664RH-T (FLATPACK), CDFP3-F28
TOP VIEW



† $\overline{P}$ must be hardwired at all times to V_{DD}, except during programming.

Functional Diagram



† P must be hardwired at all times to V_{DD}, except during programming.

TRUTH TABLE

$\overline{E}$	$\overline{G}$	MODE
0	0	Enabled
0	1	Output Disabled
1	X	Disabled

Timing Waveform

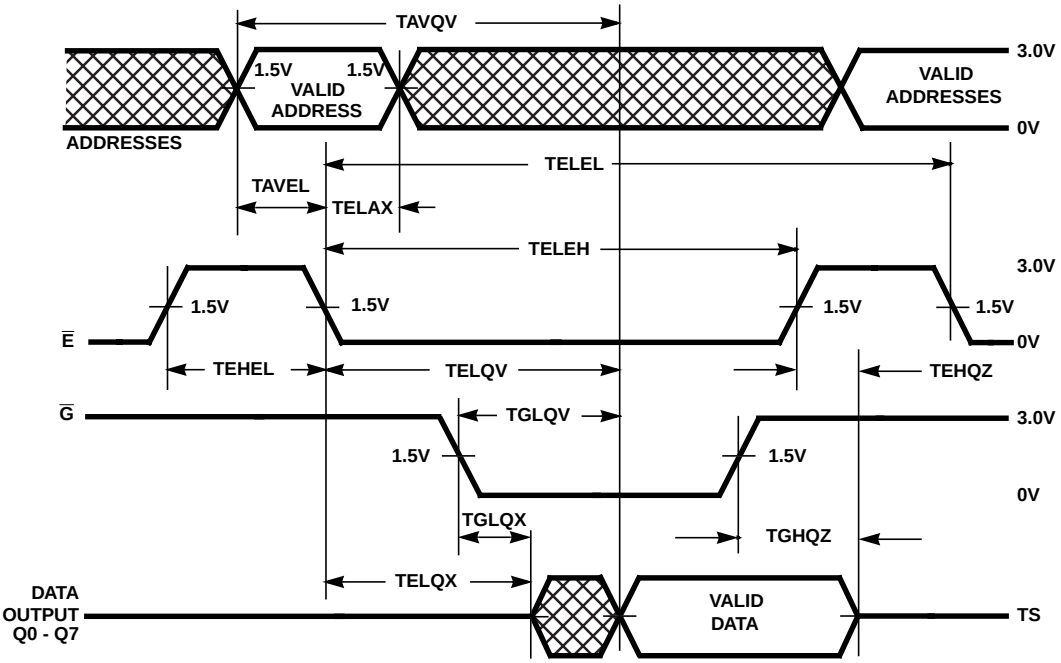


FIGURE 1. READ CYCLE

Die Characteristics

DIE DIMENSIONS:

(6883µm x 7798µm x 483µm ±25.4µm)

271 x 307 x 19mils ±1mil

METALLIZATION:

MI: 6kÅ ±1kÅ Si/Al/Cu

2kÅ ±500Å TiW

M2: 10kÅ ±2kÅ Si/Al/Cu

SUBSTRATE POTENTIAL:

V_{DD}

BACKSIDE FINISH:

Silicon

PASSIVATION:

Type: Silox (S_iO_2)

Thickness: 8kÅ ±1kÅ

WORST CASE CURRENT DENSITY:

< 2.0e5 A/cm^2

TRANSISTOR COUNT:

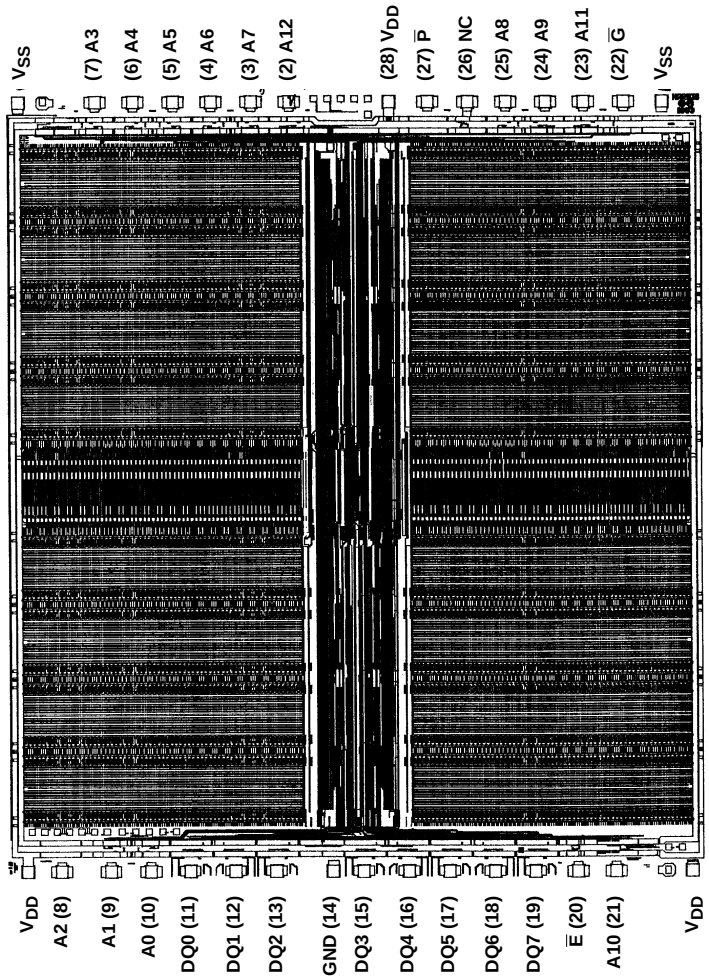
110, 874, (27,719 Gates)

PROCESS:

AVLSI

Metallization Mask Layout

HS-6664RH-T



All Intersil semiconductor products are manufactured, assembled and tested under **ISO9000** quality systems certification.