HIGH TEMPERATURE µP COMPATIBLE 12-BIT A/D CONVERTER

HT574

FEATURES

- Specified Over -55 to +225°C
- Includes On-Chip Clock, Reference, µP Interface and Sample/Hold
- 11-Bit Linearity
- 10 µs Maximum Conversion, Including Acquisition
- Hermetic 28-Lead Ceramic DIP

APPLICATIONS

- Down-Hole Oil Well
- Avionics
- Turbine Engine Control
- Industrial Process Control
- Nuclear Reactor
- Electric Power Conversion
- Heavy Duty Internal Combustion Engines

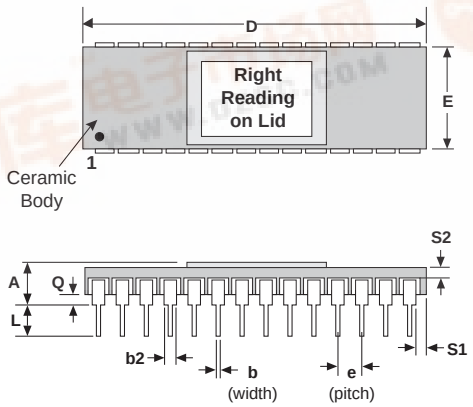
GENERAL DESCRIPTION

The HT574 is a general purpose, 12-bit successive approximation A/D converter intended for applications with an extremely wide operating temperature range. Fabricated with Honeywell's dielectrically isolated high temperature (HTMOS™) process, it is designed specifically for severe high-temperature applications.

The HT574 includes a switched capacitor, digital-to-analog converter, internal reference, comparator, successive approximation register, sample and hold, oscillator and architecture which allows it to be used with minimal external components. Tristate output buffers and digital control pins are also provided for microprocessor interfacing. Analog input signal ranges of 0 to +10V, 0 to +20V, or ±5V may be selected from the internal resistor scaling network.

The HT574 provides 12-bit conversions in 10µs over the entire -55 to +225°C temperature range. Typically, parts will operate up to +300°C for a year, with derated performance. All parts are burned in at 250°C to eliminate infant mortality.

28-LEAD PACKAGE

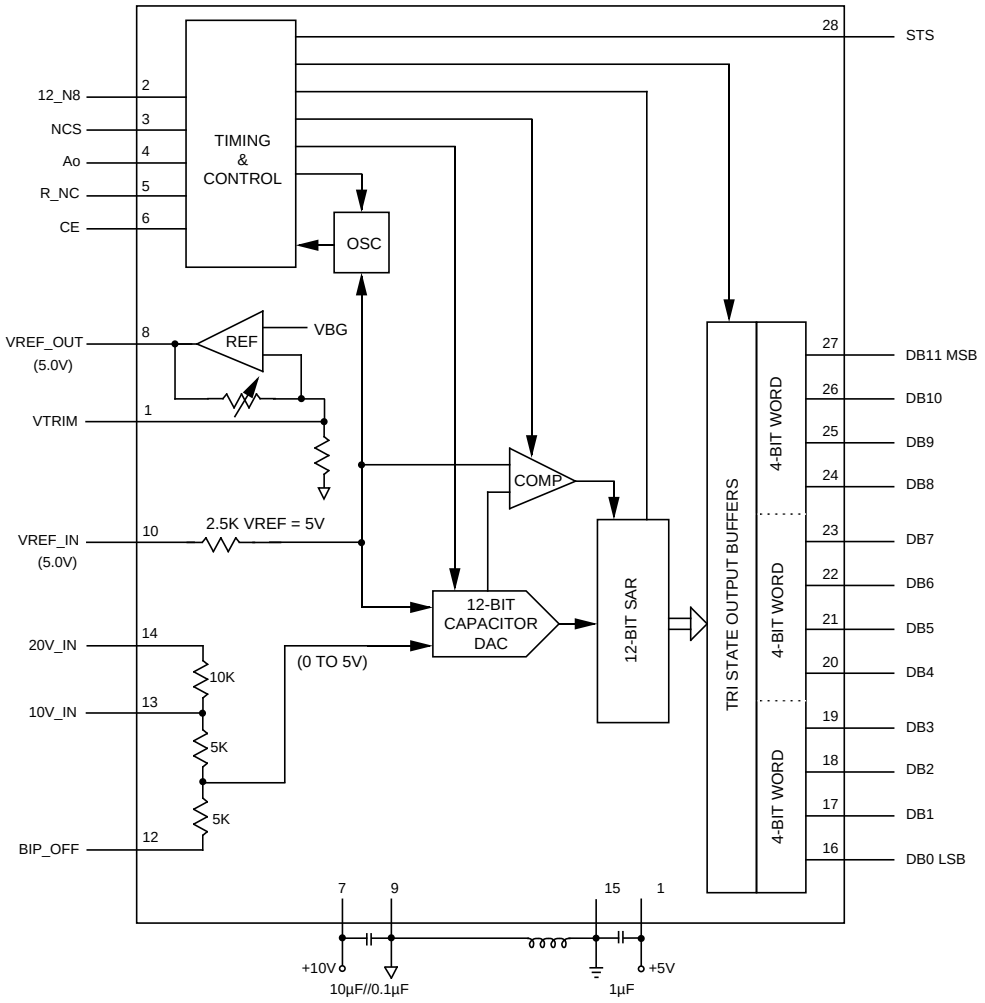


All dimensions in inches

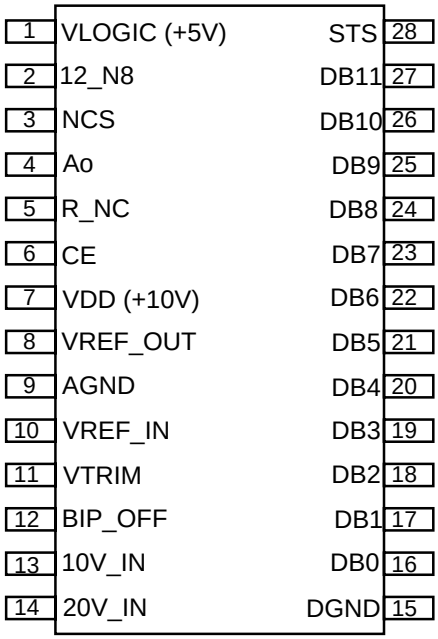
A	0.175 (max)
b	0.018 ± 0.002
b2	0.050 (typ)
C	0.010 to 0.002
D	1.400 ± 0.014
E	0.594 ± 0.010
e	0.100 ±0.005
eA	0.600 ±0.010
L	0.125 to 0.175
Q	0.050 ±0.010
S1	0.005 (min)
S2	0.005 (min)

HT574

FUNCTIONAL DIAGRAM



PINOUT DIAGRAM



NAME	FUNCTION
VLOGIC	Digital Supply (5V)
12_N8	Data Mode Select (1 = 12 bits; 0 = 8 bits)
NCS	Chip Select (Active Low)
Ao	Byte Size Select
R_NC	Read/Convert (1 = Read; 0 = Convert)
CE	Chip Enable (Active High)
VDD	Analog Supply (10V)
VREF_OUT	Reference Output (5 V)
AGND	Analog Ground
VREF_IN	Reference Input
VTRIM	Trims Vref-out
BIP_OFF	Bipolar Offset
10V_IN	10 Volt Analog Input
20V_IN	20 Volt Analog Input
DGND	Digital Ground
DB0:11	12-Bit Digital Output (DB11 = MSB, DB0 = LSB)
STS	Status

DC ELECTRICAL CHARACTERISTICS

Temperature ranges = -55 to +225°C, VDD = 10.0V ±10%
Typical @ +25°C, Vlogic = +5V, unless otherwise specified

Parameter	Conditions	Typ	Min	Max	Units
Resolution				12	Bits
Integral Non-Linearity (INL)	Tmin to Tmax			±1	LSB
Differential Non-Linearity (DNL)	Tmin to Tmax			±1	LSB
Unipolar Offset Error	Adjustable to zero			±2	LSB
Bipolar Offset Error	Adjustable to zero			±10	LSB
Full Scale Calibration Error (1)	No adjustment at +25℃, Tmin to Tmax	0.8			% of FS
	With adjustment at +25℃, Tmin to Tmax	0.5			% of FS
Temperature Coefficients	Using internal reference, Tmin to Tmax				
Unipolar Offset				±2 (5)	LSB (ppm/℃)
Bipolar Offset				±4 (10)	LSB (ppm/℃)
Full Scale Calibration				±20 (50)	LSB (ppm/℃)
Power Supply Rejection	Max change in full scale calibration				
+9.0V<VDD<11>V				±2	LSB
+4.5V<VLOGIC<5.5V				±0.5	LSB
Analog Input Ranges					
Bipolar			-5	+5	V
Unipolar			0	+10	V
			0	+20	V
Impedance	Temperature coefficient = ±100ppm/℃				
10 Volt Span		3.3	2.64	3.96	KΩ
20 Volt Span		13.3	10.64	15.96	kΩ
Operating Voltage Range					
VLOGIC			+4.5	+5.5	V
VDD			+9	+11	V
Operating Current					
ILOGIC		1		3	mA
IDD		7		9	mA
Power Dissipation	VDD = 10V, VLOGIC = 5 V	75		105	mW
Internal Reference Voltage		5	4.965	5.035	V
Output Current (2)	Sink or source			8	mA

(1) Can be adjusted by tying VTRIM to external resistor and VREF_OUT or VSSA.
(2) Available for external loads, external load should not change during conversion.

DIGITAL CHARACTERISTICS

Temperature ranges = -55 to +225°C, VDD = 10.0V ±10%
Typical @ +25°C, Vlogic = +5V, unless otherwise specified

Parameter	Conditions	Typical	Min	Max	Units
Logic Inputs (CE, NCS, R_NC, Ao, 12_N8)					
Logic "1"			2.4	5.5	V
Logic "0"			-0.5	+0.8	V
Current	0 to +5.5V input	±0.01		+5	µA
Capacitance		5			pF
Logic Outputs (DB11-DBO, STS)					
Logic "0"	(ISink = 1.6mA)			+0.4	V
Logic "1"	(ISource = 500µA)		+2.4		V
Leakage	(High Z state, DB11-DBO only)	±0.1	-5	+5	µA
Capacitance		5			pF

READ MODE AC TIMING CHARACTERISTICS

Temperature ranges = -55 to +225°C, VDD = 10.0V ±10%
Typical @ +25°C, Vlogic = +5V, unless otherwise specified

Symbol	Parameter	Conditions (1)	Typical	Min	Max	Units
tDD	Access Time from CE				150	ns
tHD	Data Valid after CE Low			25		ns
tHL	Output Float Delay				150	ns
tSSR	NCS to CE Setup		0	50		ns
tSRR	R_NC to CE Setup		0	0		ns
tSAR	Ao to CE Setup			50		ns
tHSR	NCS Valid after CE Low		0	0		ns
tHRR	R_NC High after CE Low		0	0		ns
tHAR	Ao Valid after CE Low			50		ns
tHS	STS Delay after Data Valid			300	1000	ns

(1) Time is measured from 50% level of digital transitions. Tested with a 100pF and 3kΩ load for high impedance to drive and tested with 10pF and 3kΩ load for drive to high impedance.

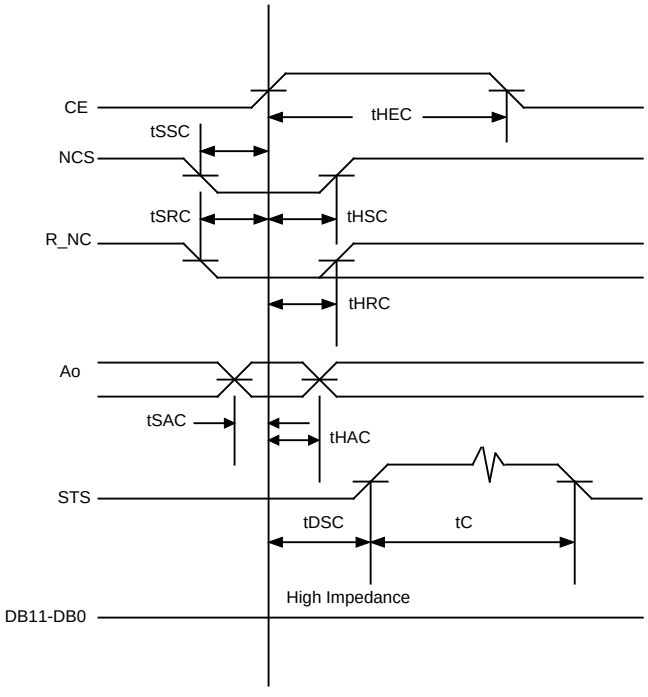
CONVERT MODE TIMING CHARACTERISTICS

Temperature ranges = -55 to +225°C, VDD = 10.0V ±10%
Typical @ +25°C, Vlogic = +5V, unless otherwise specified

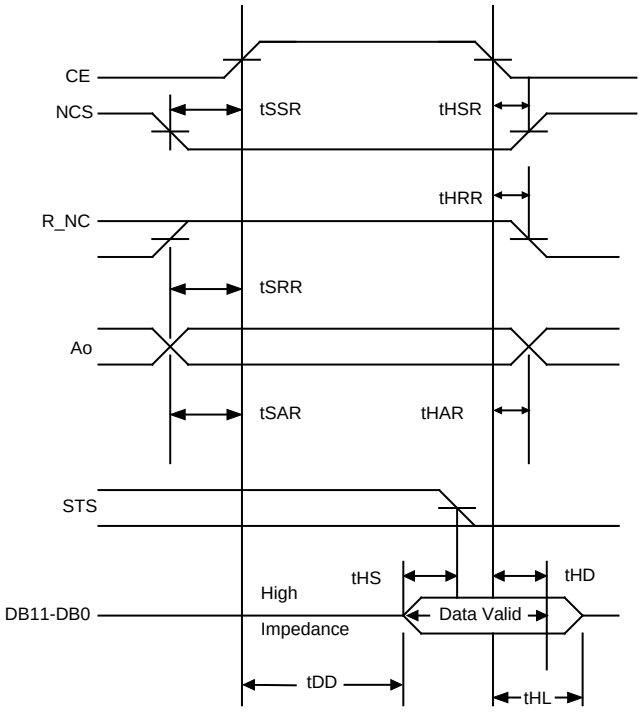
Symbol	Parameter	Conditions (1)	Typical	Min	Max	Units
tDSC	STS Delay from CE				200	ns
tHEC	CE Pulse Width			50		ns
tSSC	NCS to CE Setup			50		ns
tHCS	NCS Low during CE High			50		ns
tSRC	R_NC to CE Setup			50		ns
tHRC	R_NC Low during CE High			50		ns
tSAC	Ao to CE Setup			0		ns
tHAC	Ao Valid during CE High			50		ns
tC	Conversion Time 12-Bit Cycle 8-Bit Cycle	Including Acquisition Tmin to Tmax Tmin to Tmax			 10 7.2	 µs µs

(1) Time is measured from 50% level of digital transitions. Tested with a 100pF and 3kΩ load for high impedance to drive and tested with 10pF and 3kΩ load for drive to high impedance.

CONVERT MODE TIMING DIAGRAM



READ MODE TIMING DIAGRAM



STAND ALONE MODE TIMING CHARACTERISTICS

Temperature ranges = -55 to +225°C, VDD = 10.0V ±10%
Typical @ +25°C, Vlogic = +5V, unless otherwise specified

Symbol	Parameter	Conditions (1)	Typical	Min	Max	Units
tHRL	Low R_NC Pulse Width			50		ns
tDS	STS Delay from R_NC				200	ns
tHDR	Data Valid after R_NC Low			25		ns
tHS	STS Delay after Data Valid			300	1000	ns
tHRH	High R_NC Pulse Width			150		ns
tDDR	Data Access Time				150	ns

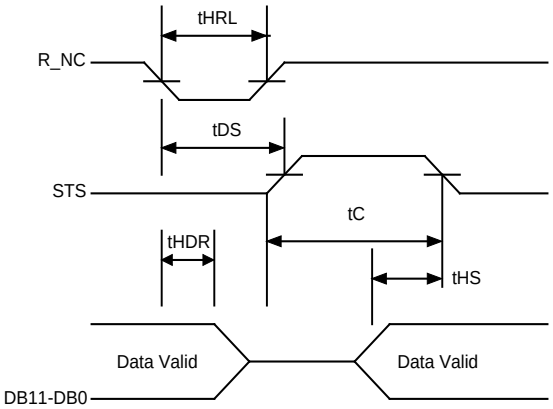
SAMPLE AND HOLD CHARACTERISTICS

-55 to 225°C, VDD = +10V, VLOGIC = +5V
Unless otherwise specified

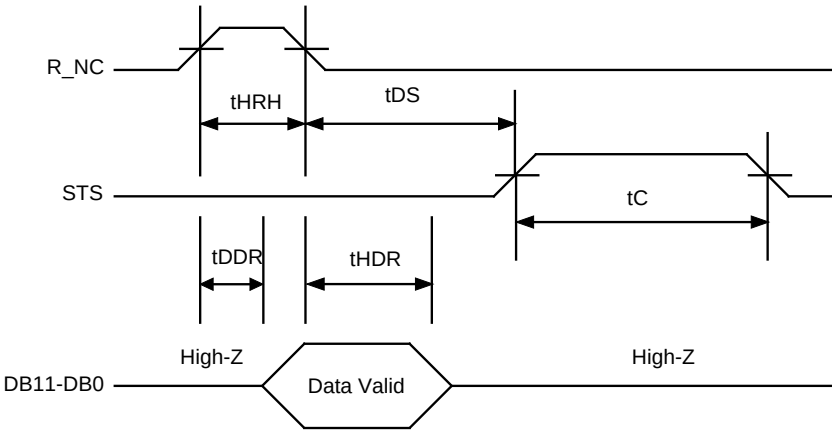
	Parameter	Conditions (1)	Typical	Min	Max	Units
	Acquisition Time				1.26	µs
	Aperture Uncertainty Time		20			ns

(1) Time is measured from 50% level of digital transitions. Tested with a 100pF and 3kΩ load for high impedance to drive and tested with 10pF and 3kΩ load for drive to high impedance.

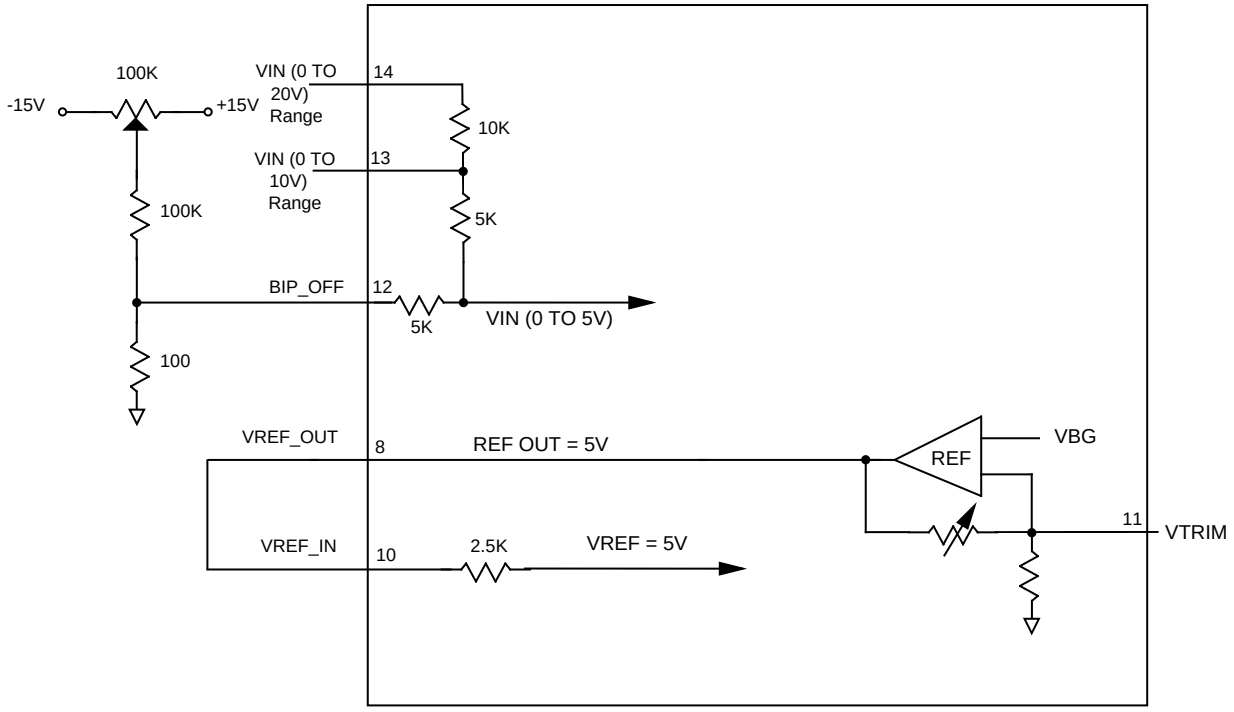
STAND ALONE MODE TIMING LOW PULSE FOR R_NC



STAND ALONE MODE TIMING HIGH PULSE FOR R_NC

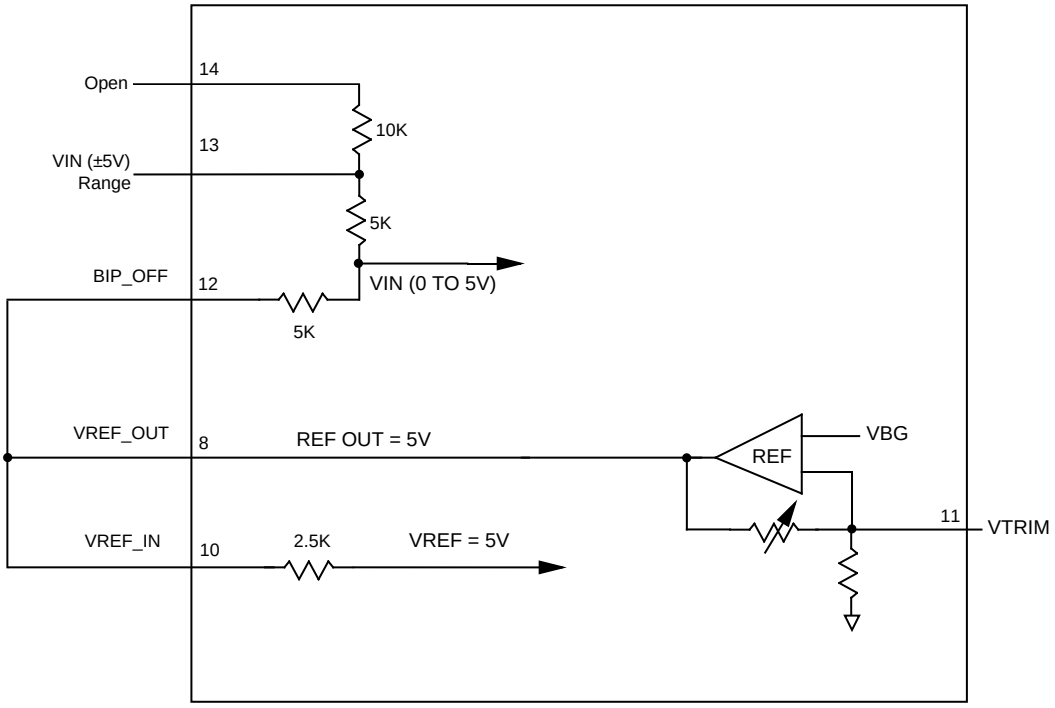


UNIPOLAR INPUT CONNECTIONS



Note: If no offset adjustment is required, BIP_OFF can be tied directy to AGND (0 volts).

BIPOLAR INPUT CONNECTIONS



TRUTH TABLE FOR HT574 CONTROL

Case	CE	NCS	R_NC	12_N8	A0	Operation
1	0	X	X	X	X	None
2	X	1	X	X	X	None
3	⌐¬	0	0	X	0	Initiate 12 Bit Conversion
4	⌐¬	0	0	X	1	Initiate 8 Bit Conversion
5	1	¬⌐	0	X	0	Initiate 12 Bit Conversion
6	1	¬⌐	0	X	1	Initiate 8 Bit Conversion
7	1	0	¬⌐	X	0	Initiate 12 Bit Conversion
8	1	0	¬⌐	X	1	Initiate 8 Bit Conversion
9	1	0	1	1	X	Enable 12 Bit Output
10	1	0	1	0	0	Enable 8 MSB's Only
11	1	0	1	0	1	Enable 4 LSB's + 4 Trailing Zero's

ABSOLUTE MAXIMUM RATINGS (1)

VDD to Analog Common ..... 0V to +12.5V
VLOGIC to Digital Common ..... 0V to +7V
Analog Common to Digital Common ..... ±1V
Control Inputs (CE, NCS, 12_N8, Ao, R_NS) to Digital Common ..... -0.5V to VLOGIC +0.5V
Analog Inputs (VREF_IN, BIP_OFF, 10V_IN) to Analog Common ..... ±12.5V
20V_IN to Analog Common ..... ±24V
VREF_OUT ..... Indefinite Short Circuit to Ground
Power Dissipation 1000mW
Storage Temperature ..... -65 to +325°C
Lead Temperature (Attachment, 10 sec.) ..... 355°C
ESD Protection 2000V

(1) Stresses in excess of those listed above may result in permanent damage. These are stress ratings only, and operation at these levels is not implied. Frequent or extended exposure to absolute maximum conditions may effect device reliability.

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