

# 3<sup>18</sup> Series of Decoders

## **Features**

- Operating voltage: 2.4V~12V
- Low power and high noise immunity CMOS technology
- · Low standby current
- · Capable of decoding 18 bits of information
- Pairs with HOLTEK's 3<sup>18</sup> series of encoders
- 8~18 address pins
- 0~8 data pins

# **Applications**

- Burglar alarm system
- Smoke and fire alarm system
- Garage door controllers
- Car door controllers

# **General Description**

The 3<sup>18</sup> decoders are a series of CMOS LSIs for remote control system applications. They are paired with the 3<sup>18</sup> series of encoders. For proper operation a pair of encoder/decoder pair with the same number of address and data format should be selected (refer to the encoder/decoder cross reference tables).

The 3<sup>18</sup> series of decoders receives serial address and data from that series of encoders that are transmitted by a carrier using an RF or an IR transmission medium. It then compares the serial input data twice continuously with its local address. If no errors or unmatched codes

- Trinary address setting
- Two times of receiving check
- Built-in oscillator needs only a 5% resistor
- Valid transmission indictor
- Easily interface with an RF or an infrared transmission medium
- Minimal external components
- · Car alarm system
- Security system
- Cordless telephones
- Other remote control systems

are encountered, the input data codes are decoded and then transferred to the output pins. The VT pin also goes high to indicate a valid transmission.

The 3<sup>18</sup> decoders are capable of decoding 18 bits of information that consists of N bits of address and 18–N bits of data. To meet various applications they are arranged to provide a number of data pins whose range is from 0 to 8 and an address pin whose range is from 8 to 18. In addition, the 3<sup>18</sup> decoders provide various combinations of address/data number in different packages.

### **Selection Table**

Function	Address	Data		VT	Oscillator	Tuisson	Package		
Item	No.	No.	Туре	VI	Oscillator	Trigger	1 ackage		
HT602L	12	2	L	√	RC oscillator	DIN active "Hi"	20 DIP/20 SOP		
HT604L	10	4	L	√	RC oscillator	DIN active "Hi"	20 DIP/20 SOP		
HT605L	9	5	L	$\sqrt{}$	RC oscillator	DIN active "Hi"	20 DIP/20 SOP		
HT611	14	0		√	RC oscillator	DIN active "Hi"	20 DIP/20 SOP		







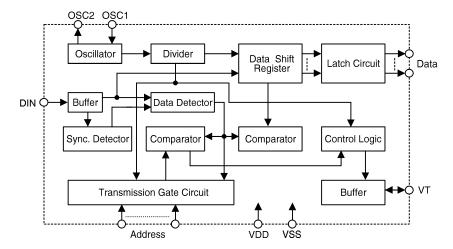
Function	Address	D			Oscillator	Tuissan	Doolsogo	
Item	No.	No.	Туре	VT	Oscillator	Trigger	Package	
HT612	12	2	M		RC oscillator	DIN active "Hi"	20 DIP/20 SOP	
HT614	10	4	M		RC oscillator	DIN active "Hi"	20 DIP/20 SOP	
HT615	9	5	M		RC oscillator	DIN active "Hi"	20 DIP/20 SOP	
HT644L	14	4	L		RC oscillator	DIN active "Hi"	24 SOP/24 SDIP	
HT646L	12	6	L	$\sqrt{}$	RC oscillator	DIN active "Hi"	24 SOP/24 SDIP	
HT648L	10	8	L		RC oscillator	DIN active "Hi"	24 SOP/24 SDIP	
HT651	18	0	_		RC oscillator	DIN active "Hi"	24 SOP/24 SDIP	
HT654	14	4	M	√	RC oscillator	DIN active "Hi"	24 SOP/24 SDIP	
HT656	12	6	M		RC oscillator	DIN active "Hi"	24 SOP/24 SDIP	
HT658	10	8	M		RC oscillator	DIN active "Hi"	24 SOP/24 SDIP	
HT682L	10	2	L	√	RC oscillator	DIN active "Hi"	18 DIP	
HT683L	9	3	L		RC oscillator	DIN active "Hi"	18 DIP	
HT684L	8	4	L		RC oscillator	DIN active "Hi"	18 DIP	
HT691	12	0	_	√	RC oscillator	DIN active "Hi"	18 DIP	
HT692	10	2	M	$\sqrt{}$	RC oscillator	DIN active "Hi"	18 DIP	
HT693	9	3	M	$\sqrt{}$	RC oscillator	DIN active "Hi"	18 DIP	
HT694	8	4	M	$\sqrt{}$	RC oscillator	DIN active "Hi"	18 DIP	

Note: Data type: M represents momentary type of data output. L represents latch type of data output.

VT can be used as a momentary data output.



# **Block Diagram**



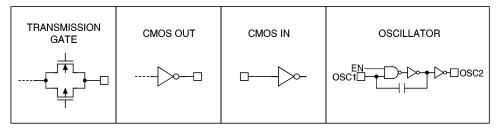
Note: The address/data pins are available in various combinations (refer to the address/data table).

# **Pin Description**

Pin Name	I/O	Internal Connection	Description
A0~A17	I	TRANSMISSION GATE	Input pins for address A0~A17 setting They can be externally set to VDD, VSS, or left open.
D10~D17	О	CMOS OUT	Output data pins
DIN	I	CMOS IN	Serial data input pin
VT	О	CMOS OUT	Valid transmission, active high
OSC1	I	OSCILLATOR	Oscillator input pin
OSC2	О	OSCILLATOR	Oscillator output pin
VSS	I	_	Negative power supply (GND)
VDD	I	_	Positive power supply



# Approximate internal connection circuits



# **Absolute Maximum Ratings\***

Supply Voltage0.3V to 13V	Storage Temperature50°C to 125°C
Input VoltageV <sub>SS</sub> -0.3V to V <sub>DD</sub> +0.3V	Operating Temperature20°C to 75°C

\*Note: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of this device at these or any other conditions above those indicated in the operational sections of this specification is not implied and exposure to absolute maximum rating conditions for extened periods may affect device reliability.

## **Electrical Characteristics**

 $(Ta=25^{\circ}C)$ 

C	D	Te	est Conditions	M:	т	34	Unit	
Symbol	Parameter	$V_{DD}$	Conditions	Min.	Тур.	Max.	Omt	
$V_{\mathrm{DD}}$	Operating Voltage	_	_	3	_	12	V	
Lamp	Standby Current	5V	Oscillator stone	_	0.1	1	μΑ	
I <sub>STB</sub>	Standby Current	12V	Oscillator stops	_	2	4	μΑ	
$I_{DD}$	Operating Current	5V	No load F <sub>OSC</sub> =100kHz	_	0.2	1	mA	
т.	Data Output Source Current (D10~D17)		V <sub>OH</sub> =4.5V	-0.5	-1	_	mA	
Io	Data Output Sink Current (D10~D17)	5V	V <sub>OL</sub> =0.5V	0.5	1	_	mA	
т	VT Output Source Current	5V	V <sub>OH</sub> =4.5V	-2	-4	_	mA	
$I_{VT}$	VT Output Sink Current		V <sub>OL</sub> =0.5V	1	2	_	mA	
$V_{IH}$	"H" Input Voltage	5V	_	3.5	_	5	V	
V <sub>IL</sub>	"L" Input Voltage	5V	_	0	_	1	V	
Fosc	Oscillator Frequency	10V	R <sub>OSC</sub> =330kΩ	_	100	_	kHz	



# **Functional Description**

## Operation

The  $3^{18}$  series of decoders provides various combinations of address and data pins in different packages. It is paired with the 3<sup>18</sup> series of encoders. The decoders receive data transmitted by the encoders and interpret the first N bits of the code period as address and the last 18-N bits as data (where N is the address code number). A signal on the DIN pin then activates the oscillator which in turns decodes the incoming address and data. The decoders will check the received address twice continuously. If all the received address codes match the contents of the decoder's local address, the 18-N bits of data are decoded to activate the output pins, and the VT pin is set high to indicate a valid transmission. That will last until the address code is incorrect or no signal has been received. The output of the VT pin is high only when the transmission is valid. Otherwise it is low always.

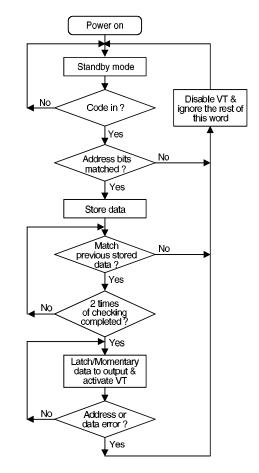
#### **Output type**

There are 2 types of output to select from:

- Momentary type
  - The data outputs follow the encoder during a valid transmission and then reset.
- Latch type

The data outputs follow the encoder during a valid transmission, and are then latched in this state until the next valid transmission occurs.

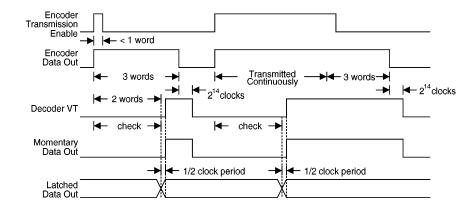
#### **Flowchart**



Note: The oscillator is disabled in the standby state and activated as long as a logic "high" signal is applied to the DIN pin. i.e., the DIN should be kept "low" if there is no signal input.



# **Decoder timing**



# **Encoder/Decoder selection tables**

• Latch type of data output

							Pacl	kage			
Part No.	Data Pins	Address Pins	VT	Pair Encoder	1	Encode	r	Decoder			
					DIP	SOP	SDIP	DIP	SOP	SDIP	
HT682L	2	10	<b>√</b>	HT680	18	_	_	18	_	_	
HT683L	3	9	<b>√</b>	HT680	18	_		18	_		
HIUOSL	3	9	V	HT6187	18	_		10			
HT684L	4	8	<b>√</b>	HT680	18	_	_	18	_	_	
HT602L	2	12	<b>V</b>	HT600	20	20	_	20	20	_	
HT604L	4	4 10	V	HT600	20	20		20	20		
11004L	4	10	V	HT6207	20	_	_	20	20		
HT605L	5	9	<b>V</b>	HT600	20	20	_	20	20	_	
HT644L	4	14	<b>V</b>	HT640	24	24	24		24	24	
HT646L	6	12	ا	HT640	24	24	9.4			24	
11040L	O	12	V	HT6247	24	_	24	_	24	24	
HT648L	8	10	<b>V</b>	HT640	24	24	24		24	24	



# • Momentary type of data output

	B. A.I.					Pacl	cage				
Part No.	Data Pins	Address Pins	VT	Pair Encoder	J	Encode	r	Decoder			
					DIP	SOP	SDIP	DIP	SOP	SDIP	
HT691	0	12	<b>√</b>	HT680	18	_	_	18	_	_	
HT692	2	10	√	HT680	18	_	_	18	_	_	
LITEO	0	0	V	HT680	18	_		10			
HT693	3	9	V	HT6187	18	_		18	_	_	
HT694	4	8	<b>√</b>	HT680	18	_	_	18	_	_	
HT611	0	14	√	HT600	20	20	_	20	20	_	
HT612	2	12	√	HT600	20	20	_	20	20	_	
LITCIA	4	10	<b>√</b>	HT600	20	20		20	20		
HT614	4	10	V	HT6207	20			20	20	_	
HT615	5	9	√	HT600	20	20	_	20	20	_	
HT651	0	18	√	HT640	24	24	24	_	24	24	
HT654	4	14	<b>√</b>	HT640	24	24	24		24	24	
LITEE	I I I I I I I I I I I I I I I I I I I		<b>√</b>	HT640	24 24		9.4		0.4	9.4	
HT656	O	6 12		HT6247	24	_	24	_	24	24	
HT658	8	10	<b>√</b>	HT640	24	24	24		24	24	



# Address/Data sequence

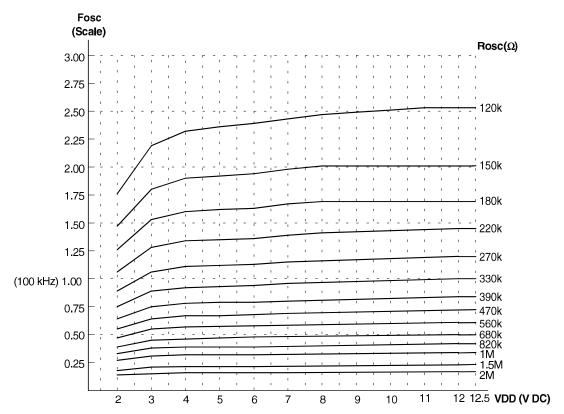
The following provides a table of address/data sequence for various models of the  $3^{18}$  series decoders. A correct device should be selected according to the requirements of individual address and data.

Part No.		Address/Data Bits													
Part No.	0~3	4	5	6~9	10	11	12	13	14	15	16	17			
HT602L	A0~A3	A4	_	A6~A9	-	A11	A12	A13	D14	D15	_	_			
HT604L	A0~A3	A4	_	A6~A9	-	A11	D12	D13	D14	D15	_	_			
HT605L	A0~A3	A4	_	A6~A9	ı	D11	D12	D13	D14	D15	_	_			
HT611	A0~A3	A4	_	A6~A9	ı	A11	A12	A13	A14	A15	_	_			
HT612	A0~A3	A4	_	A6~A9	-	A11	A12	A13	D14	D15	_	_			
HT614	A0~A3	A4	_	A6~A9	-	A11	D12	D13	D14	D15	_	_			
HT615	A0~A3	A4	_	A6~A9	ı	D11	D12	D13	D14	D15	_	_			
HT644L	A0~A3	A4	A5	A6~A9	A10	A11	A12	A13	D14	D15	D16	D17			
HT646L	A0~A3	A4	A5	A6~A9	A10	A11	D12	D13	D14	D15	D16	D17			
HT648L	A0~A3	A4	A5	A6~A9	D10	D11	D12	D13	D14	D15	D16	D17			
HT651	A0~A3	A4	A5	A6~A9	A10	A11	A12	A13	A14	A15	A16	A17			
HT654	A0~A3	<b>A4</b>	A5	A6~A9	A10	A11	A12	A13	D14	D15	D16	D17			
HT656	A0~A3	A4	A5	A6~A9	A10	A11	D12	D13	D14	D15	D16	D17			
HT658	A0~A3	A4	A5	A6~A9	D10	D11	D12	D13	D14	D15	D16	D17			
HT682L	A0~A3	_	_	A6~A9	_	A11	A12	_	D14	D15	_	_			
HT683L	A0~A3	_	_	A6~A9		A11	D12	_	D14	D15	_	_			
HT684L	A0~A3	_	_	A6~A9	ı	D11	D12	_	D14	D15	_	_			
HT691	A0~A3	_	_	A6~A9	ı	A11	A12	_	A14	A15	_	_			
HT692	A0~A3	_	_	A6~A9		A11	A12	_	D14	D15		_			
HT693	A0~A3		_	A6~A9		A11	D12	_	D14	D15		_			
HT694	A0~A3		_	A6~A9	ı	D11	D12	_	D14	D15	_	_			

Note: "—" is a dummy code which is left "open" and not bonded out.



# Oscillator frequency vs supply voltage

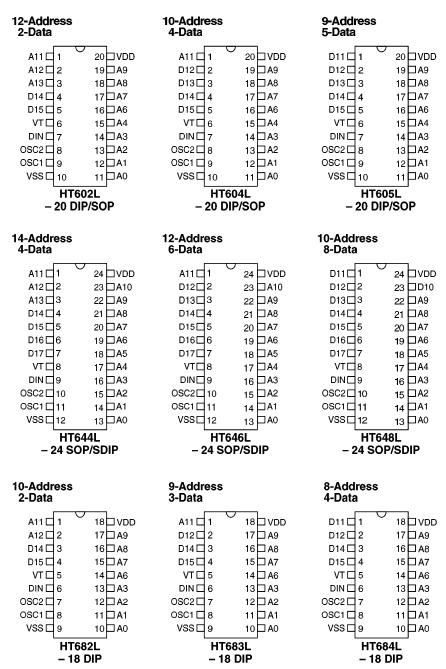


The recommended oscillator frequency is  $F_{OSCD}$  (decoder)  $\cong F_{OSCE}$  (encoder).



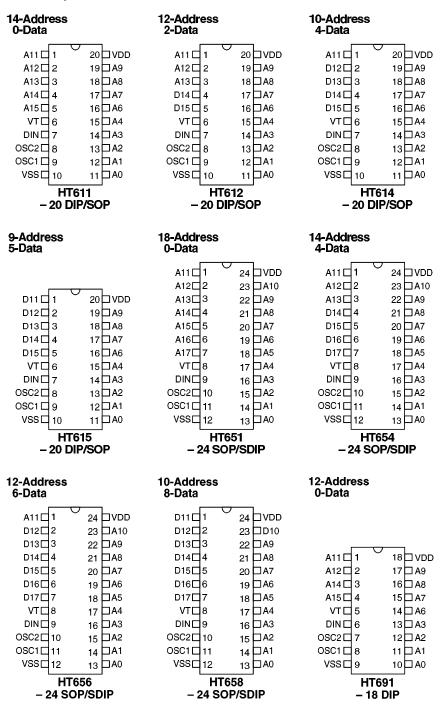
## **Package Information**

#### Latch series





## **Momentary series**



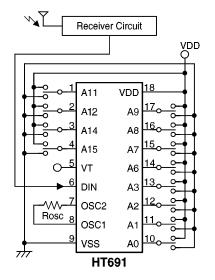


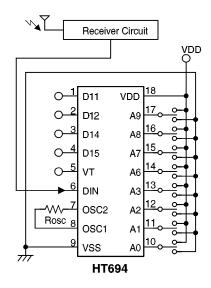
# **Momentary series**

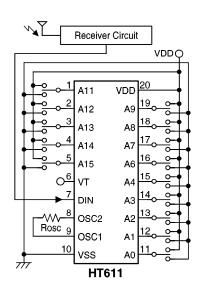
10-Addre 2-Data	ess		9-Addı 3-Data				8-Addr 4-Data	ess		
A11 🗗	1 18	PADD	A11 □	1	18	PADD	D11	1	18	⊐VDD
A12 □	2 17	□ <b>A</b> 9	D12 □	2	17	<b>□ A</b> 9	D12 □	2	17	□ <b>A</b> 9
D14 □	3 16	□ A8	D14 □	3	16	□ A8	D14 □	3	16	□ A8
D15 🗆	4 15	□ A7	D15 □	4	15	□ A7	D15 □	4	15	□ A7
VT □	5 14	□ <b>A</b> 6	VT□	5	14	□ A6	VT □	5	14	□ <b>A</b> 6
DIN 🗆	6 13	<b>□</b> A3	DIN□	6	13	□ A3	DIN□	6	13	□ <b>A</b> 3
OSC2 □	7 12	□ A2	OSC2 □	7	12	□ A2	OSC2□	7	12	□ A2
OSC1 □	8 11	□ A1	OSC1 □	8	11	□ A1	OSC1 □	8	11	□ A1
vss□	9 10	□ A0	VSS□	9	10	□ A0	VSS□	9	10	□ A0
_	HT692 - 18 DIP	1		HT69:		1	'	HT69-	-	

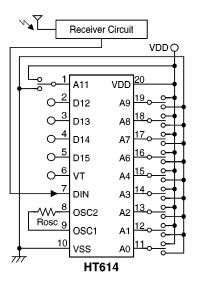


# **Application Circuits**

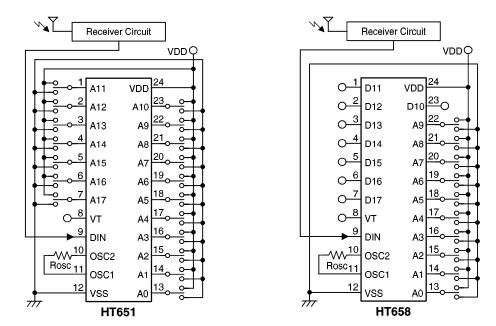












Note: Typical infrared receiver: PIC-12043T/PIC-12043C (KODENSHI CORP.) or LTM9052 (LTTEON CORP.)

Typical RF receiver: JR-200 (JUWA CORP.) RE-99 (MING MICROSYSTEM, U.S.A.)