HT6230
Infrared Remote Encoder

Features

- Operating voltage: 2.4V~5.2V
- 32 system codes, each system with 64 command codes
- Programmable transmission codes
- Biphase transmission method
- Generated modulation output data (1/2 system frequency and 1/4 duty cycle)
- Single pin oscillator
- 429kHz resonator system clock
- Test pins available
- 28-pin SOP package

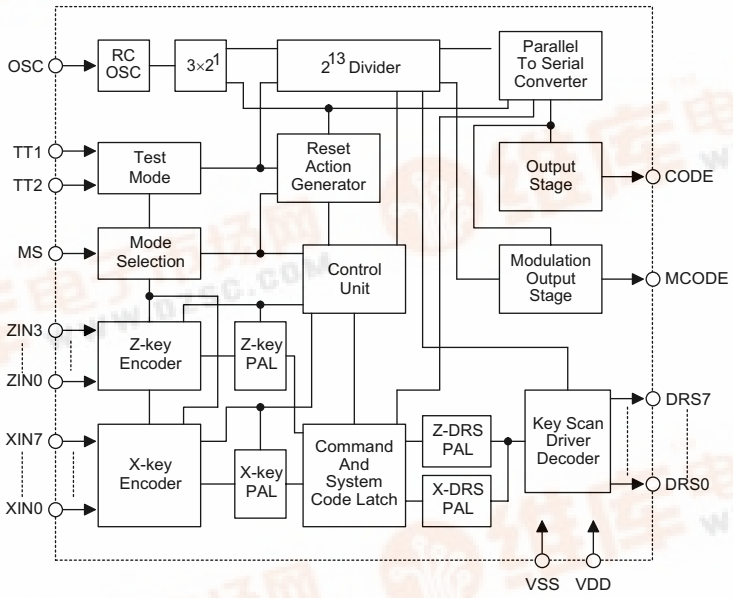
Applications

- Televisions and video cassette recorder controllers
- Garage door controllers
- Car door controllers
- Security systems
- Other remote control systems

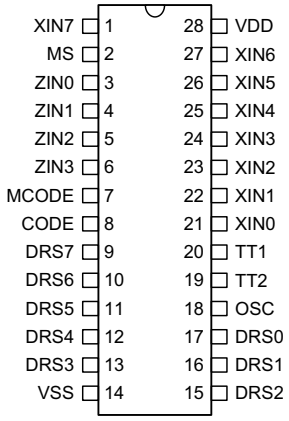
General Description

The HT6230 is designed as infrared remote encoder, usually applied to TV systems. A total of 2048 different commands can be generated and arranged into 32 systems where each system contains 64 different commands. There are 96 keys and to each key is assigned one programmable code. The code is programmable by mask option. Legal and illegal key operation can be distinguished.

Block Diagram

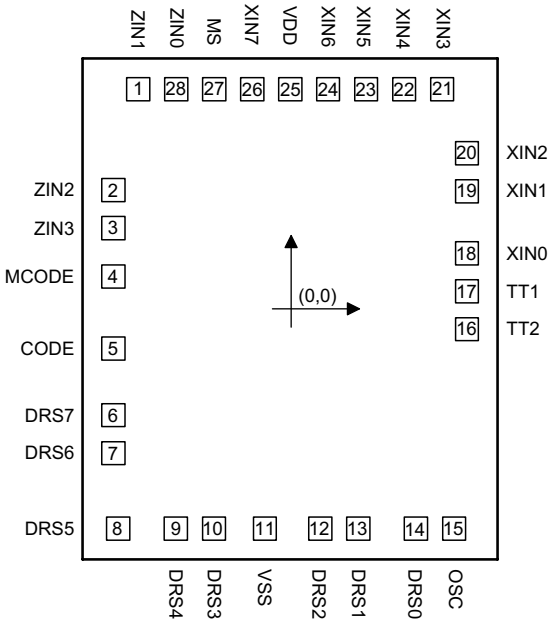


Pin Assignment



HT6230
– 28 SOP

Pad Assignment



Chip size: 1605 × 1910 (μm)^2

* The IC substrate should be connected to VDD in the layout artwork.

Pad Coordinates

Unit: μm

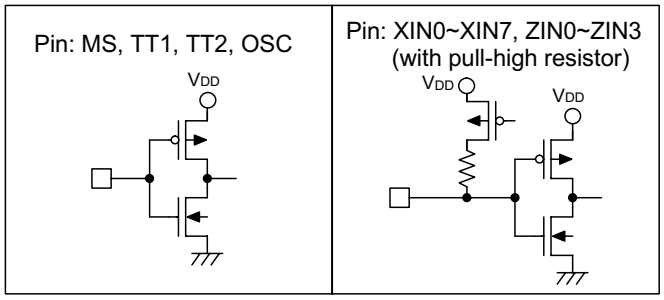
Pad No.	X	Y	Pad No.	X	Y
1	–570.19	817.68	15	605.12	–817.68
2	–662.85	442.16	16	653.07	–75.59
3	–662.85	300.74	17	653.07	65.84
4	–662.85	120.29	18	653.07	207.26
5	–662.85	–147.93	19	653.07	437.29
6	–662.85	–395.02	20	653.07	578.71
7	–662.85	–536.45	21	561.23	817.68
8	–644.16	–817.68	22	419.80	817.68
9	–429.58	–817.68	23	278.37	817.68
10	–288.15	–817.68	24	136.94	817.68
11	–98.77	–817.68	25	–4.48	817.68
12	107.68	–817.68	26	–145.91	817.68
13	249.11	–817.68	27	–287.34	817.68
14	463.69	–817.68	28	–428.76	817.68

Pad Description

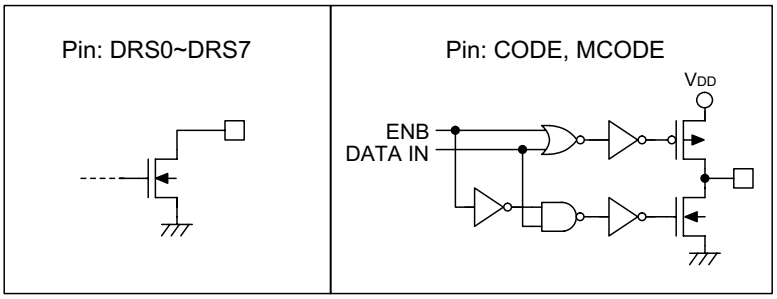
Pad No.	Pad Name	I/O	Internal Connection	Description
1~3 28	ZIN1~ZIN3 ZIN0	I	CMOS with PMOS Pull-high	Detect inputs from Z-key matrix
4	MCODE	O	Tri-state CMOS	Generate modulation output data code with 1/12 system frequency and 1/4 duty cycle
5	CODE	O	Tri-state CMOS	Generates output data code
6~10	DRS7~DRS3	O	Open Drain NMOS	Drive for key scanning
11	VSS	—	—	Negative power supply, ground
12~14	DRS2~DRS0	O	Open Drain NMOS	Drive for key scanning
15	OSC	I	CMOS	Oscillator input
16~17	TT2~TT1	I	CMOS	Switch to four operating modes: 0 0 normal mode 0 1 test mode 1 1 0 test mode 2 1 1 Reset
18~24	XIN0~XIN6	I	CMOS with PMOS Pull-high	Detect inputs from X-key matrix
25	VDD	—	—	Positive power supply
26	XIN7	I	CMOS with PMOS Pull-high	Detect input from X-key matrix
27	MS	I	CMOS	Select system mode (Two modes provided: One-key system mode and Two-key system mode)

Approximate internal connection circuits

• Input terminal



• Output terminal



Absolute Maximum Ratings

Supply Voltage.....–0.3V to 5.5V
Input Voltage.....V_{SS}–0.3V to V_{DD}+0.3V
Storage Temperature.....–50°C to 125°C
Operating Temperature .....–25°C to 75°C

Note: These are stress ratings only. Stresses exceeding the range specified under "Absolute Maximum Ratings" may cause substantial damage to the device. Functional operation of this device at other conditions beyond those listed in the specification is not implied and prolonged exposure to extreme conditions may affect device reliability.

Electrical Characteristics

Ta=25°C

Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
		V_{DD}	Conditions				
V_{DD}	Supply Voltage	—	—	2.4	—	5.2	V
V_{OL1}	DRS0~DRS7 Output Voltage Low	3V	I_{OL1}=0.3mA	—	—	0.3	V
V_{OL2}	CODE, MCODE Output Voltage Low	3V	I_{OL2}=0.6mA	—	—	0.3	V
V_{OH}	CODE, MCODE Output Voltage High	3V	I_{OH}=–0.4mA	V_{DD}–0.3	—	—	V
R_{PH}	XIN0~XIN7 and ZIN0~ZIN3 Pull-high	3V	TT1=TT2=MS=Low V_I=0V	—	27	—	kΩ
f_{OSC}	Oscillator Frequency Operational	3V	—	—	429	—	kHz
	Free-running		—	30	50	100	kHz

Functional Description

Key operation

When MS is low, the legal key operation is that only one ZIN or XIN can be connected to one DRS driver and if more than one XIN, ZIN or both are pressed at the same time then the key operation is recognized as illegal; hence, the oscillator will not start. When MS is high, the legal key operation is that exactly one ZIN and one XIN are connected to two DRS drivers and other cases of key operation are all considered as illegal.

However, when one XIN or ZIN is connected to more than one DRS, the last key scan driver is to generate output data code.

Format of transmission code

The output pin CODE transmits the data code as a code format, as shown at the bottom figure.

The method of transmitting one code bit is called biphase transmission and is represented by the following fig:

Where one code bit time is $3\times2^8\times T_{OSC}$. The output signal of the MCODE pin is the signal of the generated output code modulated by 1/12 of the system frequency with 1/4 duty cycle. In quiescent state both CODE and MCODE are high impedance.

Key scan drivers

The key scan drivers DRS0 to DRS7 are open drain NMOS and the outputs of these are all low in quiescent state. When a legal key operation is detected, the debounce cycle starts and at the end of the debounce cycle, the DRS outputs are high impedance. Furthermore, the scanning cycle starts and DRS outputs take turns to switch to low state.

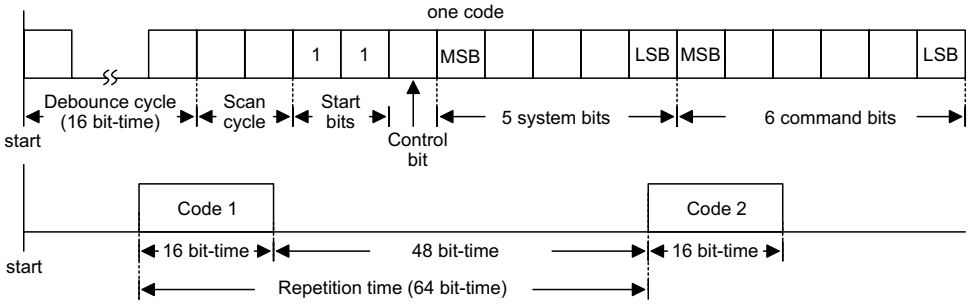
Programmable output data code

The output data code corresponding to each key is programmable by hardware mask option. The PAL circuit is necessary for this purpose.

Operation mode

- One-key system mode

  The device enters this mode by switching the MS input pin to low state. The pull-high resistors are connected to all XIN and ZIN inputs so that all sense inputs are at high state, until pulled to low state by key operation. In this mode the legal key operation is that only one ZIN or XIN can be connected to one DRS. When a sense input detects a low level, an enable signal is generated to latch the system or command latches. If the sense input belongs to ZIN, the corresponding system code is generated and the command code is defined as all



Transmission code format

logic 1. If the sense input comes from XIN, the corresponding command code together with the system code stored in the system latches are generated.

- Two-key system mode

  The device goes into this mode by switching the MS input pin to high state. The pull-high resistors are only connected to XIN inputs except the first scan cycle. In the first scan cycle, there only exists pull-high resistors in ZIN inputs. In this mode, the legal key operation is that exactly one XIN and one ZIN are connected to two DRS drivers. In the first scan duration, it detects which key in Z-key matrix is pressed and generates an enable signal to latch the system latches. While in the second scan duration, it detects which key in the X-key matrix is pressed and generates an enabled signal to latch the command latches. After being latched, the system and command codes are transmitted.

Control bit

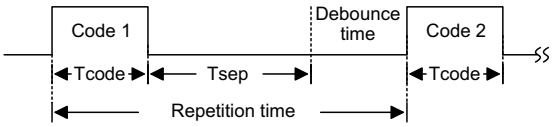
A control bit is added after two start bits and will be complemented if one key is released. The decoder can decide whether the next code is a new command or not.

Oscillator

The embedded part of the oscillator is an RC-oscillation circuit. The OSC pin is the input terminal of the RC-oscillation circuit and is connected to an external ceramic resonator (429kHz). A resistor of 6.8kΩ must be in series with the resonator. The resonator and resistor are grounded at one side.

Reset (after key release)

In a complete code repetition time, as shown in the figure below, the following situation of key release results in a reset action.



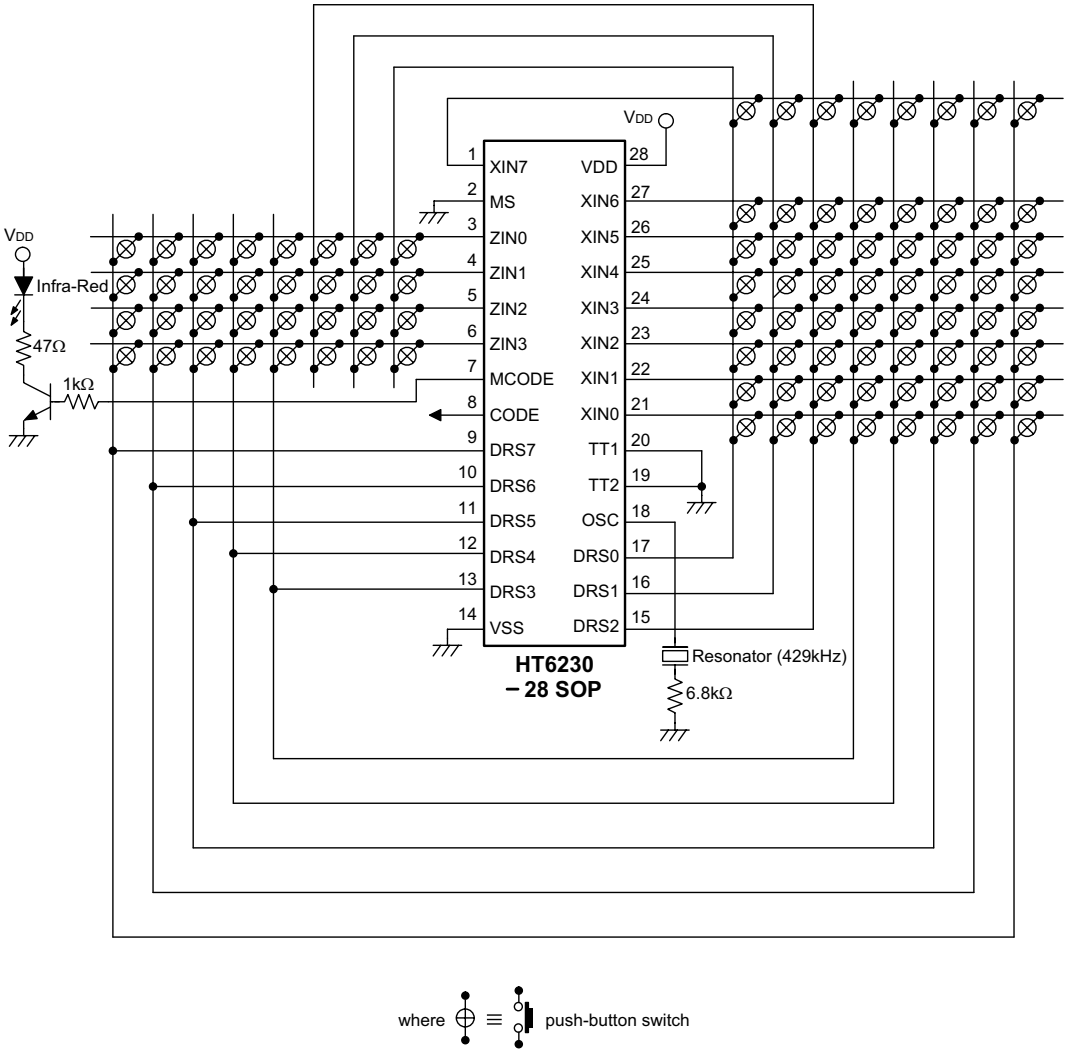
- During Tsep and debounce time, the device will reset immediately if a key is released.
- During Scan cycle in Tcode, a reset will occur if a key is released in three cases described below:
  - When one of the key scan drivers is in the low state
  - Before that key has been detected
  - When MS is high and there is no wired connection in Z-key matrix

Test pins (TT1 and TT2)

There are four modes by the combination of TT1 and TT2.

TT1	TT2	Mode
0	0	Normal mode
1	1	Reset
1	0	Test mode 1
0	1	Test mode 2

Application Circuits



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