

HOLTEK



HT93LC66

4K 3-Wire CMOS Serial EEPROM

Features

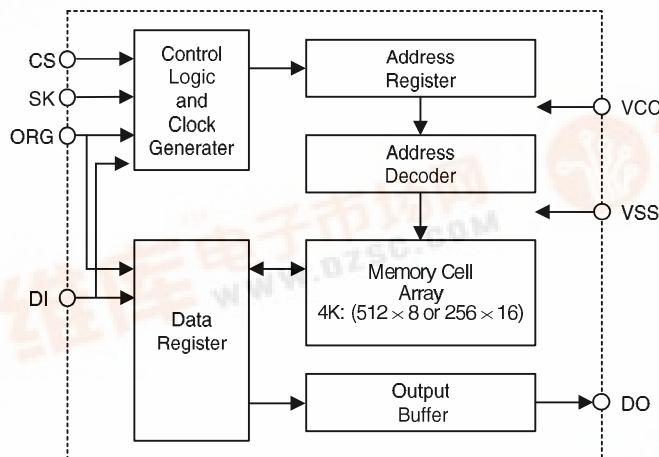
- Operating voltage V_{CC}
 - Read: 2.0V~5.5V
 - Write: 2.4V~5.5V
- Low power consumption
 - Operating: 5mA max.
 - Standby: 10 μ A max.
- User selectable internal organization
 - 4K(HT93LC66): 512 \times 8 or 256 \times 16
- 3-wire Serial Interface
- Write cycle time: 5ms max.
- Automatic erase-before-write operation
- Word/chip erase and write operation
- Write operation with built-in timer
- Software controlled write protection
- 10-year data retention after 100K rewrite cycles
- 10⁶ rewrite cycles per word
- 8-pin DIP/SOP package
- Commercial temperature range (0°C to +70°C)

General Description

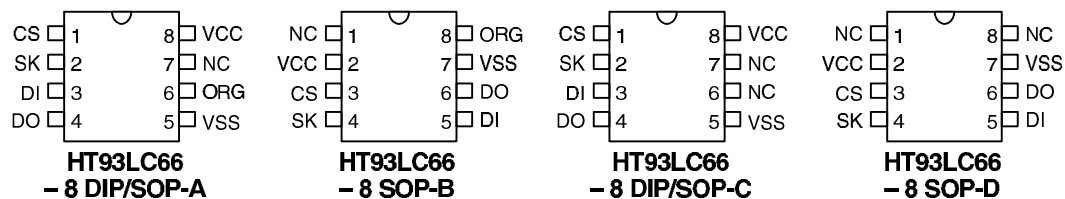
The HT93LC66 is a 4K-bit low voltage nonvolatile, serial electrically erasable programmable read only memory device using the CMOS floating gate process. Its 4096 bits of memory are organized into 256 words of 16 bits each when the ORG pin is connected to VCC or organized into 512 words of 8 bits each when it is tied to VSS. The

device is optimized for use in many industrial and commercial applications where low power and low voltage operation are essential. By popular microcontroller, the versatile serial interface including chip select (CS), serial clock (SK), data input (DI) and data output (DO) can be easily controlled.

Block Diagram



Pin Assignment



Pin Description

Pin Name	I/O	Description
CS	I	Chip select input
SK	I	Serial clock input
DI	I	Serial data input
DO	O	Serial data output
VSS	I	Negative power supply
ORG	I	Internal Organization
NC	—	No connection
VCC	I	Positive power supply

Absolute Maximum Ratings

Operation Temperature (Commercial) 0°C to 70°C
 Applied V_{CC} Voltage with Respect to V_{SS} -0.3V to 6.0V
 Applied Voltage on any Pin with Respect to V_{SS} V_{SS}-0.3V to V_{CC}+0.3V
 Supply READ Voltage 2V to 5.5V

Note: These are stress ratings only. Stresses exceeding the range specified under “Absolute Maximum Ratings” may cause substantial damage to the device. Functional operation of this device at other conditions beyond those listed in the specification is not implied and prolonged exposure to extreme conditions may affect device reliability.

D.C. Characteristics

Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
		V _{CC}	Conditions				
V _{CC}	Operating Voltage	—	Read	2.0	—	5.5	V
			Write	2.4	—	5.5	V
I _{CC1}	Operating Current (TTL)	5V	DO unload, SK=1MHz	—	—	5	mA
I _{CC2}	Operating Current (CMOS)	5V	DO unload, SK=1MHz	—	—	5	mA
		2~5.5V	DO unload, SK=250kHz	—	—	5	mA
I _{STB}	Standby Current (CMOS)	5V	CS=SK=DI=0V	—	—	10	μA
I _{LI}	Input Leakage Current	5V	V _{IN} =V _{SS} ~V _{CC}	0	—	1	μA
I _{LO}	Output Leakage Current	5V	V _{OUT} =V _{SS} ~V _{CC} CS=0V	0	—	1	μA
V _{IL}	Input Low Voltage	5V	—	0	—	0.8	V
		2~5.5V	—	0	—	0.1V _{CC}	V
V _{IH}	Input High Voltage	5V	—	2	—	V _{CC}	V
		2~5.5V	—	0.9V _{CC}	—	V _{CC}	V
V _{OL}	Output Low Voltage	5V	I _{OL} =2.1mA	—	—	0.4	V
		2~5.5V	I _{OL} =10μA	—	—	0.2	V
V _{OH}	Output High Voltage	5V	I _{OH} =-400μA	2.4	—	—	V
		2~5.5V	I _{OH} =-10μA	V _{CC} -0.2	—	—	V
C _{IN}	Input Capacitance	—	V _{IN} =0V, f=250kHz	—	—	5	pF
C _{OUT}	Output Capacitance	—	V _{OUT} =0V, f=250kHz	—	—	5	pF

A.C. Characteristics

Symbol	Parameter	VCC=5V±10%		VCC=3V±10%		VCC=2V*		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
f _{SK}	Clock Frequency	0	2000	0	500	0	250	kHz
t _{SKH}	SK High Time	250	—	1000	—	2000	—	ns
t _{SKL}	SK Low Time	250	—	1000	—	2000	—	ns
t _{CSS}	CS Setup Time	50	—	200	—	200	—	ns
t _{CSH}	CS Hold Time	0	—	0	—	0	—	ns
t _{CDS}	CS Deselect Time	250	—	250	—	1000	—	ns
t _{DIS}	DI Setup Time	100	—	200	—	400	—	ns
t _{DIH}	DI Hold Time	100	—	200	—	400	—	ns
t _{PD1}	DO Delay to "1"	—	250	—	1000	—	2000	ns
t _{PD0}	DO Delay to "0"	—	250	—	1000	—	2000	ns
t _{SV}	Status Valid Time	—	250	—	250	—	—	ns
t _{HV}	DO Disable Time	100	—	400	—	400	—	ns
t _{PR}	Write Cycle Time	—	5	—	5	—	—	ms

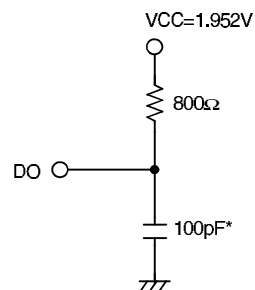
* For Read Operating Only

A.C. test conditions

Input rise and fall time: 5ns (1V to 2V)

Input and output timing reference levels: 1.5V

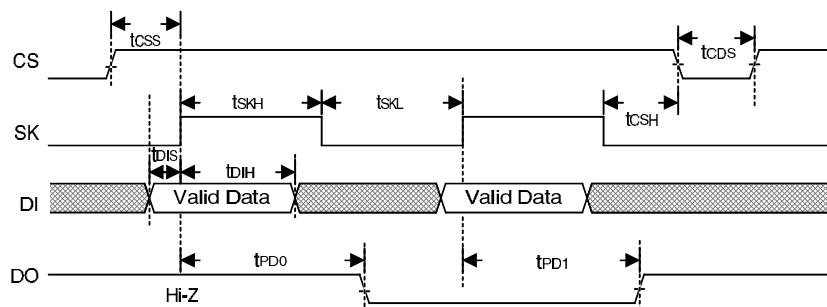
Output load: See Figure right



*Including scope and jig

Output load circuit

Timing Diagrams



Functional Description

The HT93LC66 is accessed via a three-wire serial communication interface. The device is arranged into 256 words by 16 bits or 512 words by 8 bits depending whether the ORG pin is connected to VCC or VSS. The HT93LC66 contains seven instructions: READ, ERASE, WRITE, EWEN, EWDS, ERAL and WRAL. When the user selectable internal organization is arranged into 256×16 (512×8), these instructions are all made up of 11(12) bits data: 1 start bit, 2 op code bits and 8(9) address bits.

By using the control signal CS, SK and data input signal DI, these instructions can be given to the HT93LC66. These serial instruction data presented at the DI input will be written into the device at the rising edge of SK. During the READ cycle, DO pin acts as the data output and during the WRITE or ERASE cycle, DO pin indicates the BUSY/READY status. When the DO pin is active for read data or as a BUSY/READY indicator the CS pin must be high; otherwise DO pin will be in a high-impedance state. For successful instructions, CS must be low once after the instruction is sent. After power on, the device is by default in the EWDS state. And, an EWEN instruction must be performed before any ERASE or WRITE instruction can be executed. The following are the functional descriptions and timing diagrams of all seven instructions.

READ

The READ instruction will stream out data at a specified address on the DO pin. The data on DO pin changes during the low-to-high edge of SK signal. The 8 bits or 16 bits data stream is preceded by a logical "0" dummy bit. Irrespective of the condition of the EWEN or EWDS instruction, the READ command is always valid and independent of these two instructions. After the data word has been read the internal address will be automatically incremented by 1 allowing the next consecutive data word to be read out without entering further address data. The address will wrap around with CS High until CS returns to LOW.

EWEN/EWDS

The EWEN/EWDS instruction will enable or disable the programming capabilities. At both the power on and power off state the device automatically entered the disable mode. Before a WRITE, ERASE, WRAL or ERAL instruction is given, the programming enable instruction EWEN must be issued, otherwise the ERASE/WRITE instruction is invalid. After the EWEN instruction is issued, the programming enable condition remains until power is turned off or a EWDS instruction is given. No data can be written into the device in the programming disabled state. By so doing, the internal memory data can be protected.

ERASE

The ERASE instruction erases data at the specified addresses in the programming enable mode. After the ERASE op-code and the specified address have been issued, the data erase is activated by the falling edge of CS. Since the internal auto-timing generator provides all timing signals for the internal erase, so the SK clock is not required. During the internal erase, we can verify the busy/ready status if CS is high. The DO pin will remain low but when the operation is over, the DO pin will return to high and further instructions can be executed.

WRITE

The WRITE instruction writes data into the device at the specified addresses in the programming enable mode. After the WRITE op-code and the specified address and data have been issued, the data writing is activated by the falling edge of CS. Since the internal auto-timing generator provides all timing signal for the internal writing, so the SK clock is not required. The auto-timing write cycle includes an automatic erase-before-write capability. So, it is not necessary to erase data before the WRITE instruction. During the internal writing, we can verify the busy/ready status if CS is high. The DO pin will remain low but when the operation is over, the DO pin will return to high and further instructions can be executed.

ERAL

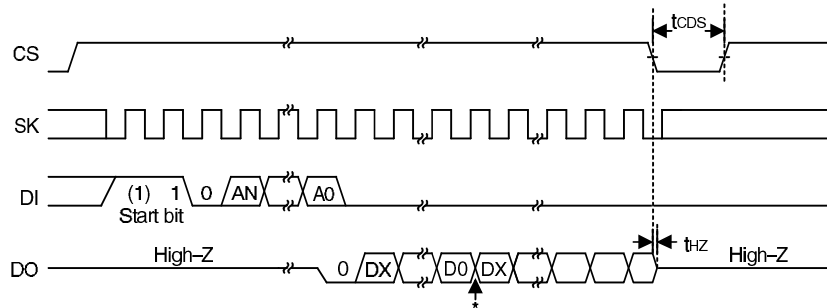
The ERAL instruction erases the entire 256×16 or 512×8 memory cells to logical “1” state in the programming enable mode. After the erase-all instruction set has been issued, the data erase feature is activated by the falling edge of CS. Since the internal auto-timing generator provides all timing signal for the erase-all operation, so the SK clock is not required. During the internal erase-all operation, we can verify the busy/ready status if CS is high. The DO pin will remain low but when the operation is over, the DO pin will return to high and further instruction can be executed.

WRAL

The WRAL instruction writes data into the entire 256×16 or 512×8 memory cells in the programming enable mode. After the write-all instruction set has been issued, the data writing is activated by the falling edge of CS. Since the internal auto-timing generator provides all timing signals for the write-all operation, so the SK clock is not required. During the internal write-all operation, we can verify the busy/ready status if CS is high. The DO pin will remain low but when the operation is over the DO pin will return to high and further instruction can be executed.

Timing Diagrams

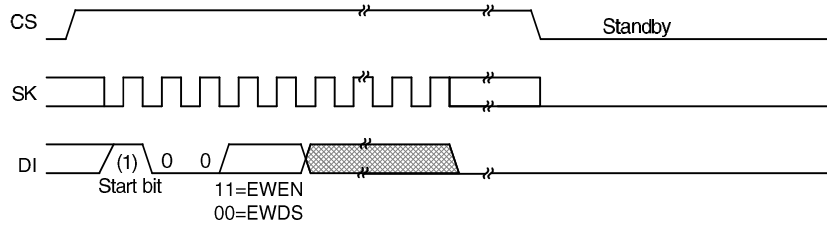
READ



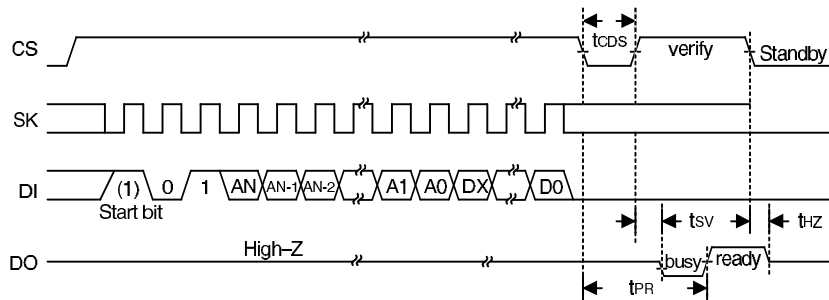
* Address pointer automatically cycles to the next word

Mode	(X16)	(X8)
AN	A7	A8
DX	D15	D7

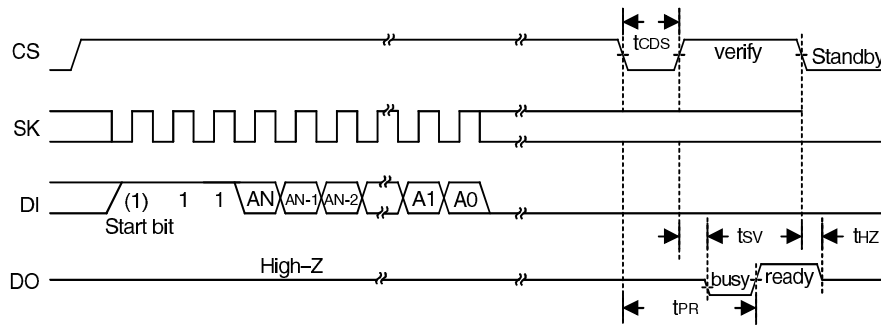
EWEN/EWDS



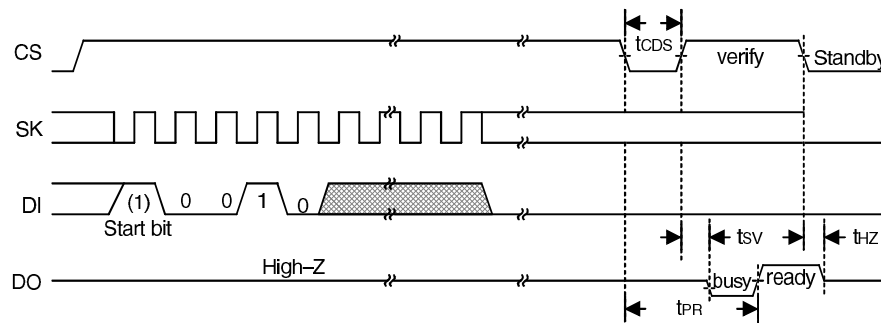
WRITE



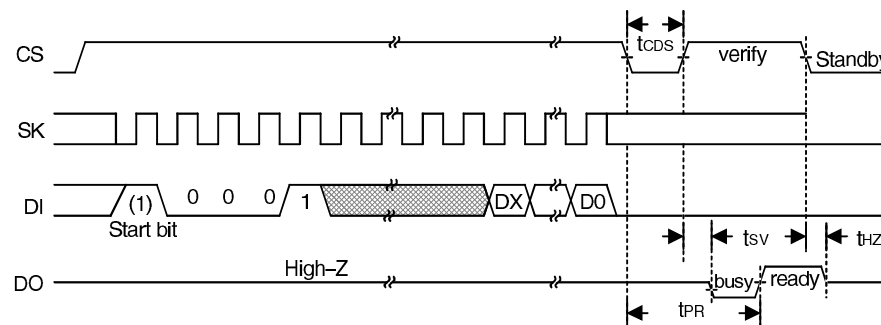
ERASE



ERAL



WRAL



Instruction Set Summary
HT93LC66

Instruction	Comments	Start bit	Op Code	Address		Data	
				ORG=0 X8	ORG=1 X16	ORG=0 X8	ORG=1 X16
READ	Read data	1	10	A8~A0	A7~A0	D7~D0	D15~D0
ERASE	Erase data	1	11	A8~A0	A7~A0	—	
WRITE	Write data	1	01	A8~A0	A7~A0	D7~D0	D15~D0
EWEN	Erase/Write Enable	1	00	11XXXXXXXX	11XXXXXX	—	
EWDS	Erase/Write Disable	1	00	00XXXXXXXX	00XXXXXX	—	
ERAL	Erase All	1	00	10XXXXXXXX	10XXXXXX	—	
WRAL	Write All	1	00	01XXXXXXXX	01XXXXXX	D7~D0	D15~D0

Note: X stands for “don’t care”

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