intersil

HUF75229P3

Data Sheet June 1998 File Number 4536.1

44A, 50V, 0.022 Ohm, N-Channel UltraFET Power MOSFET

This N-Channel power MOSFET is manufactured using the innovative UltraFET™ process. This advanced process technology achieves the lowest possible on-resistance per silicon area, resulting in outstanding performance. This device is capable of withstanding high energy in the avalanche mode and the diode exhibits very low reverse recovery time and stored charge. It was designed for use in applications where power efficiency is important, such as switching regulators, switching converters, motor drivers, relay drivers, low-voltage bus switches, and power management in portable and battery-operated products.

Ordering Information

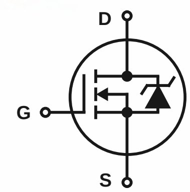
PART NUMBER	PACKAGE	BRAND
HUF75229P3	TO-220AB	75229P

NOTE: When ordering use the entire part number.

Features

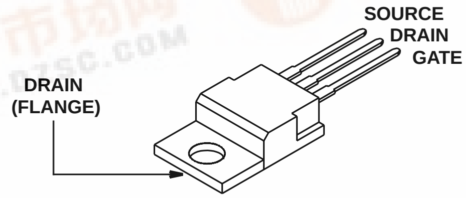
- 44A, 50V
- *Low On-Resistance,* $r_{DS(ON)} = 0.022\Omega$
- *Temperature Compensating* PSPICE Model
- *Thermal Impedance* SPICE Model
- Peak Current vs Pulse Width Curve
- UIS Rating Curve
- Related Literature
  - TB334, “Guidelines for Soldering Surface Mount Components to PC Boards”

Symbol



Packaging

JEDEC TO-220AB



Absolute Maximum Ratings $T_C = 25^oC$, Unless Otherwise Specified

			UNITS
Drain to Source Voltage (Note 1)	V_{DSS}	50	V
Drain to Gate Voltage (R_{GS} = 20kΩ) (Note 1)	V_{DGR}	50	V
Gate to Source Voltage	V_{GS}	±20	V
Drain Current			
Continuous (Figure 2)	I_D	44	A
Pulsed Drain Current	I_{DM}	Figure 5	
Pulsed Avalanche Rating	E_{AS}	Figure 6, 14, 15	
Power Dissipation	P_D	90	W
Derate Above 25^oC		0.6	$W/^oC$
Operating and Storage Temperature	T_J, T_{STG}	-55 to 175	^oC
Maximum Temperature for Soldering			
Leads at 0.063in (1.6mm) from Case for 10s	T_L	300	^oC
Package Body for 10s, See Techbrief 334	T_{pkg}	260	^oC

CAUTION: Stresses above those listed in “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

1. $T_J = 25^oC$ to 150^oC.

Electrical Specifications $T_C = 25^oC$, Unless Otherwise Specified

PARAMETER	SYMBOL	TEST CONDITIONS		MIN	TYP	MAX	UNITS
Drain to Source Breakdown Voltage	BV_{DSS}	I_D = 250μA, V_{GS} = 0V (Figure 11)		50	-	-	V
Gate to Source Threshold Voltage	$V_{GS(TH)}$	$V_{GS} = V_{DS}$, I_D = 250μA (Figure 10)		2	-	4	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 45V, V_{GS} = 0V		-	-	1	μA
		V_{DS} = 40V, V_{GS} = 0V, $T_C = 150^oC$		-	-	250	μA
Gate to Source Leakage Current	I_{GSS}	V_{GS} = ±20V		-	-	±100	nA
Drain to Source On Resistance	$r_{DS(ON)}$	I_D = 44A, V_{GS} = 10V (Figure 9)		0.017	0.020	0.022	Ω
Turn-On Time	t_{ON}	V_{DD} = 30V, $I_D \cong$ 44A, R_L = 0.68Ω, V_{GS} = 10V, R_{GS} = 9.1Ω (Figures 18, 19)		-	-	105	ns
Turn-On Delay Time	$t_{d(ON)}$			-	12	-	ns
Rise Time	t_r			-	58	-	ns
Turn-Off Delay Time	$t_{d(OFF)}$			-	33	-	ns
Fall Time	t_f			-	33	-	ns
Turn-Off Time	t_{OFF}			-	-	100	ns
Total Gate Charge	$Q_{g(TOT)}$	V_{GS} = 0V to 20V	V_{DD} = 30V, $I_D \cong$ 44A, R_L = 0.68Ω, $I_{g(REF)}$ = 1.0mA (Figures 13, 16, 17)	-	60	75	nC
Gate Charge at 10V	$Q_{g(10)}$	V_{GS} = 0V to 10V		-	35	43	nC
Threshold Gate Charge	$Q_{g(TH)}$	V_{GS} = 0V to 2V		-	2.0	2.5	nC
Input Capacitance	C_{ISS}	V_{DS} = 25V, V_{GS} = 0V, f = 1MHz (Figure 12)		-	1060	-	pF
Output Capacitance	C_{OSS}			-	405	-	pF
Reverse Transfer Capacitance	C_{RSS}			-	95	-	pF
Thermal Resistance Junction to Case	$R_{\theta JC}$	(Figure 3)		-	-	1.66	$^oC/W$
Thermal Resistance Junction to Ambient	$R_{\theta JA}$	TO-220		-	-	62	$^oC/W$

Source to Drain Diode Specifications

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Source to Drain Diode Voltage	V_{SD}	I_{SD} = 44A	-	-	1.25	V
Reverse Recovery Time	t_{rr}	I_{SD} = 44A, dI_{SD}/dt = 100A/μs	-	-	72	ns
Reverse Recovered Charge	Q_{RR}	I_{SD} = 44A, dI_{SD}/dt = 100A/μs	-	-	120	nC

Typical Performance Curves

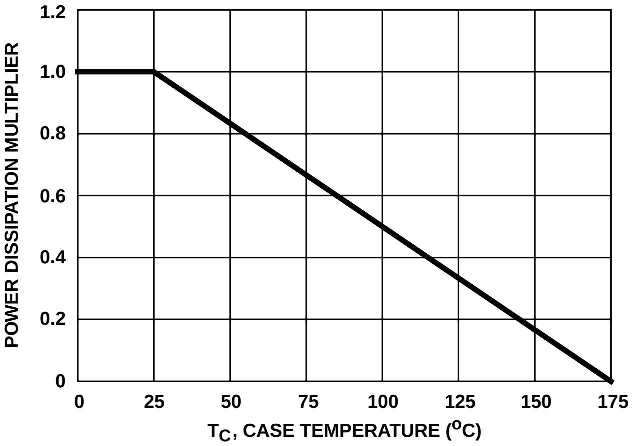


FIGURE 1. NORMALIZED POWER DISSIPATION vs CASE TEMPERATURE

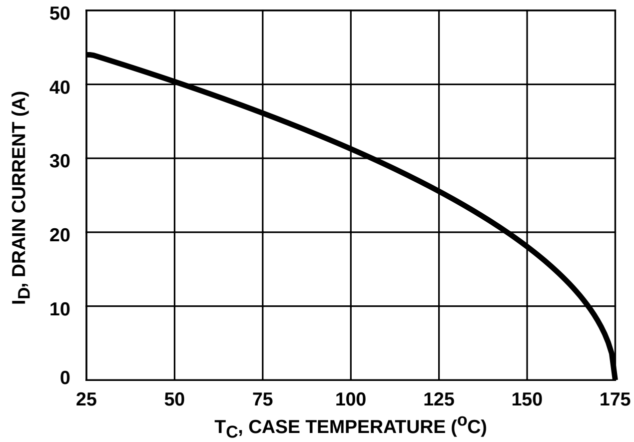


FIGURE 2. MAXIMUM CONTINUOUS DRAIN CURRENT vs CASE TEMPERATURE

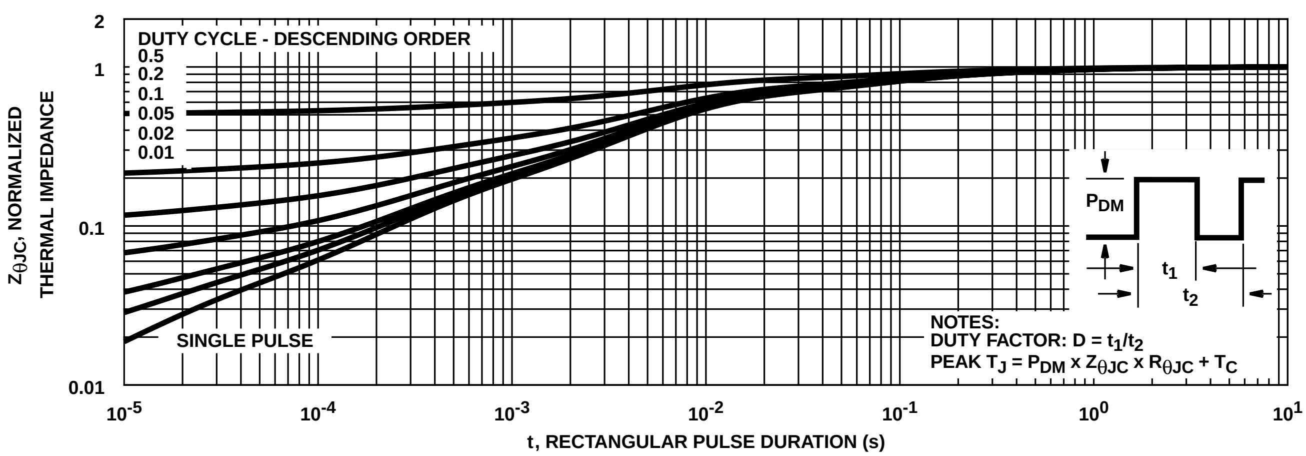


FIGURE 3. NORMALIZED MAXIMUM TRANSIENT THERMAL IMPEDANCE

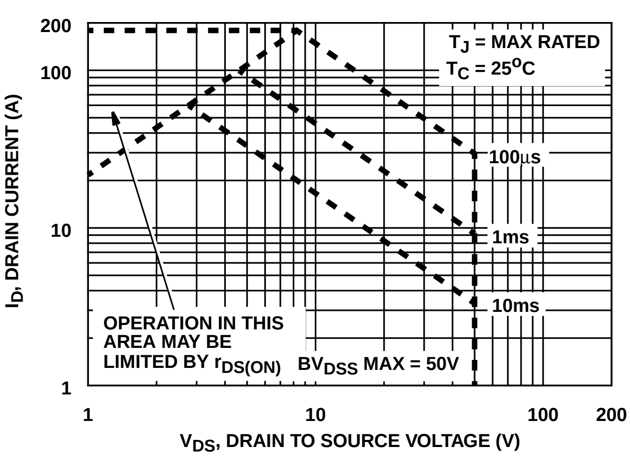


FIGURE 4. FORWARD BIAS SAFE OPERATING AREA

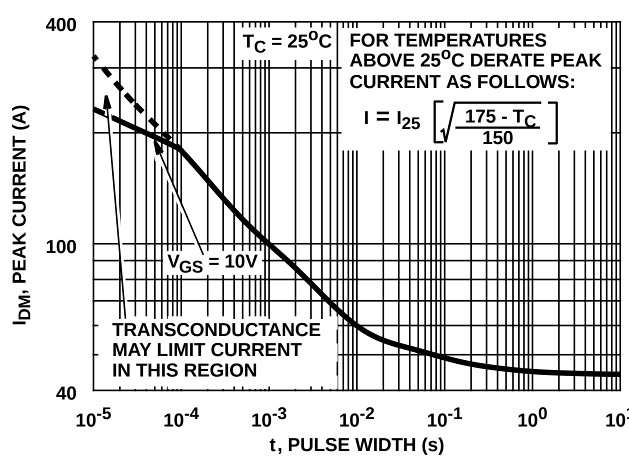
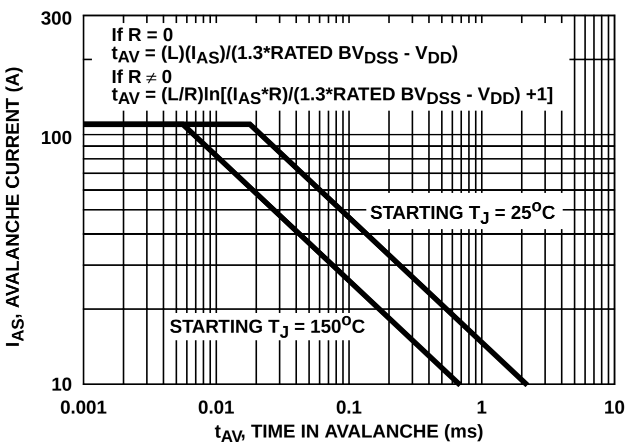


FIGURE 5. PEAK CURRENT CAPABILITY

Typical Performance Curves (Continued)



NOTE: Refer to Intersil Application Notes AN9321 and AN9322.

FIGURE 6. UNCLAMPED INDUCTIVE SWITCHING CAPABILITY

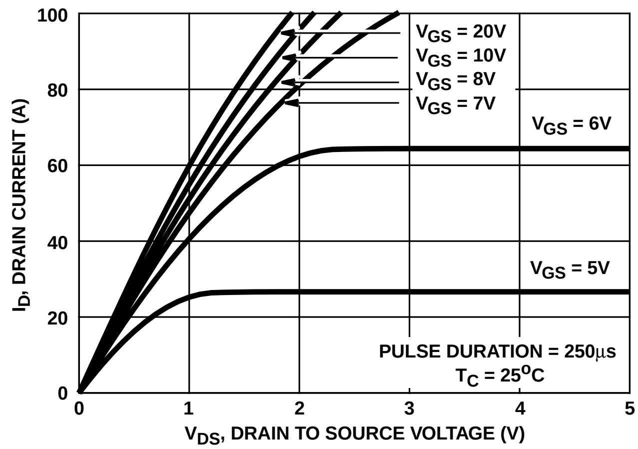


FIGURE 7. SATURATION CHARACTERISTICS

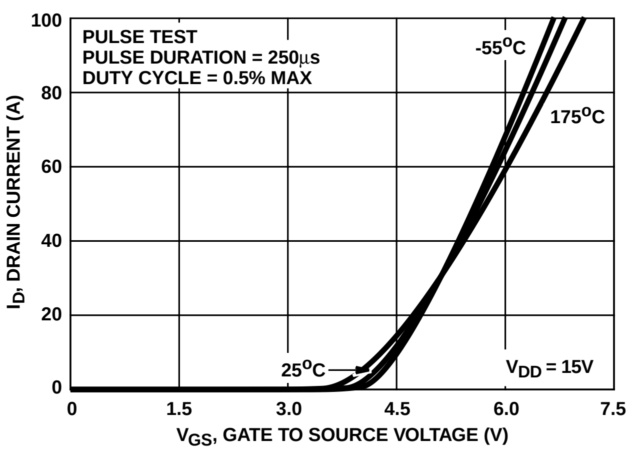


FIGURE 8. TRANSFER CHARACTERISTICS

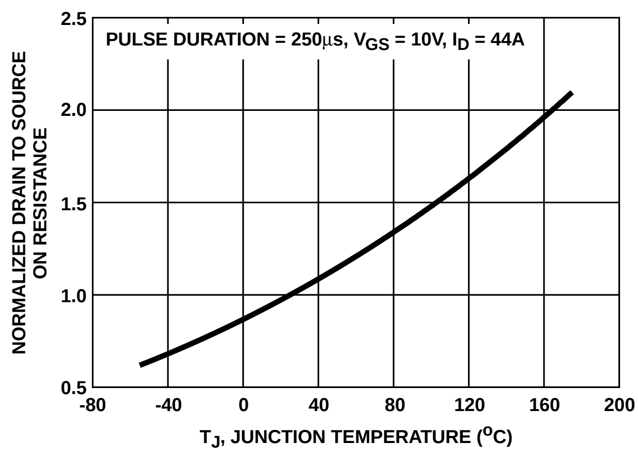


FIGURE 9. NORMALIZED DRAIN TO SOURCE ON RESISTANCE vs JUNCTION TEMPERATURE

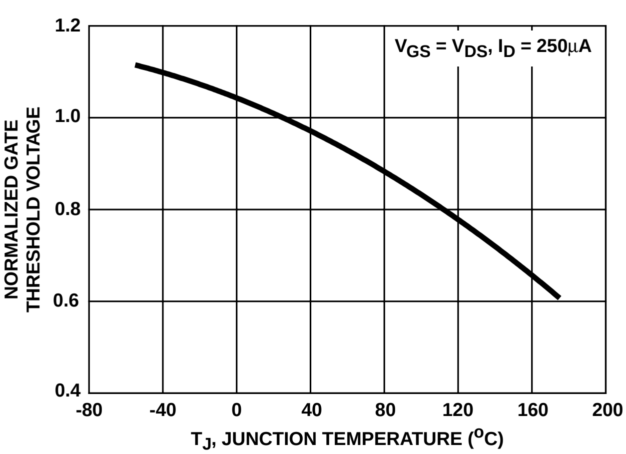


FIGURE 10. NORMALIZED GATE THRESHOLD VOLTAGE vs JUNCTION TEMPERATURE

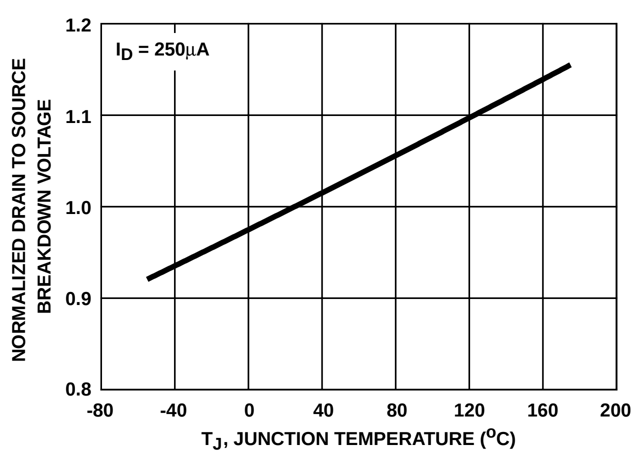


FIGURE 11. NORMALIZED DRAIN TO SOURCE BREAKDOWN VOLTAGE vs JUNCTION TEMPERATURE

Typical Performance Curves (Continued)

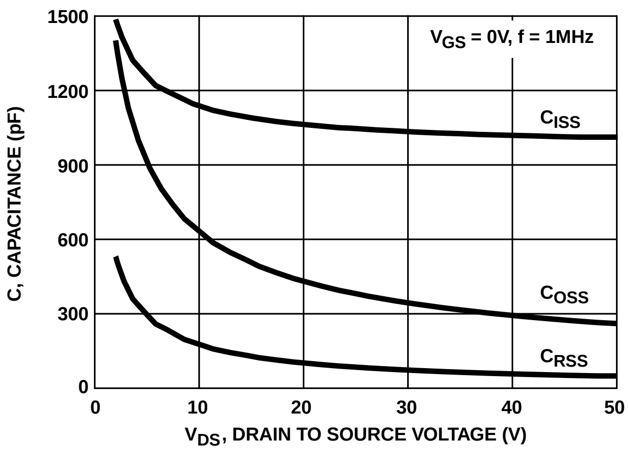
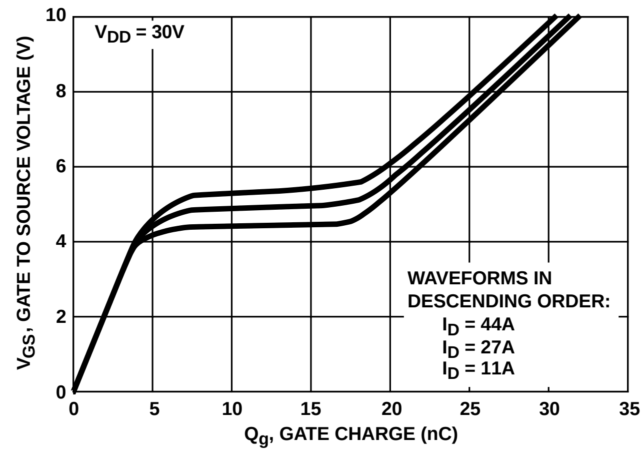


FIGURE 12. CAPACITANCE vs DRAIN TO SOURCE VOLTAGE



NOTE: Refer to Intersil Application Notes AN7254 and AN7260.

FIGURE 13. GATE CHARGE WAVEFORMS FOR CONSTANT GATE CURRENT

Test Circuits and Waveforms

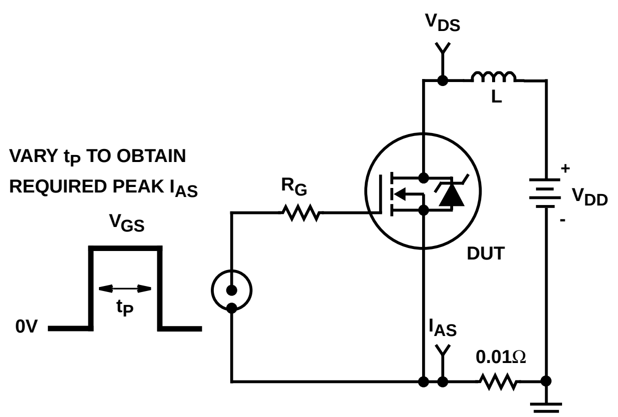


FIGURE 14. UNCLAMPED ENERGY TEST CIRCUIT

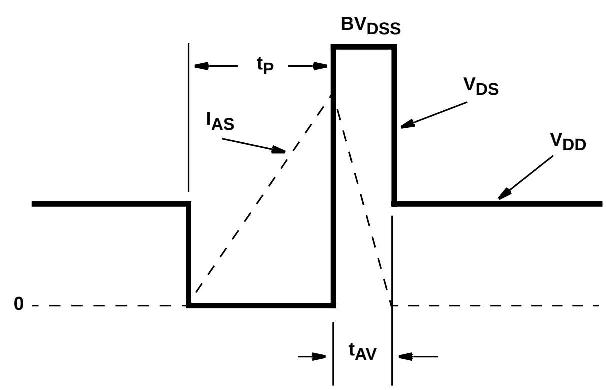


FIGURE 15. UNCLAMPED ENERGY WAVEFORMS

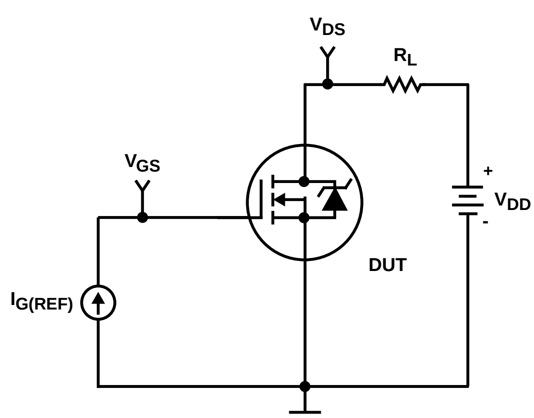


FIGURE 16. GATE CHARGE TEST CIRCUIT

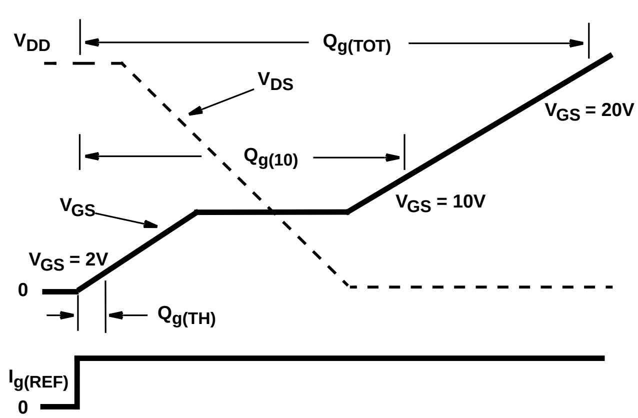


FIGURE 17. GATE CHARGE WAVEFORM

Test Circuits and Waveforms (Continued)

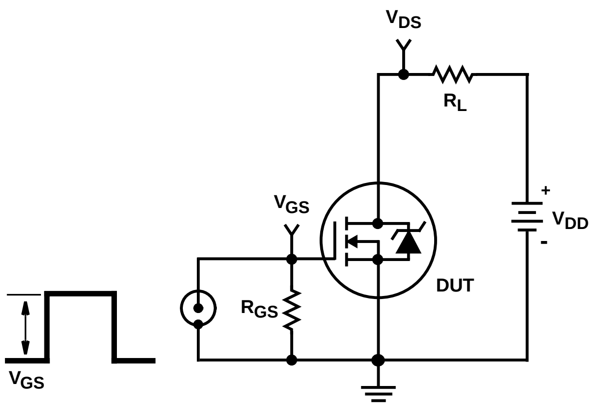


FIGURE 18. SWITCHING TIME TEST CIRCUIT

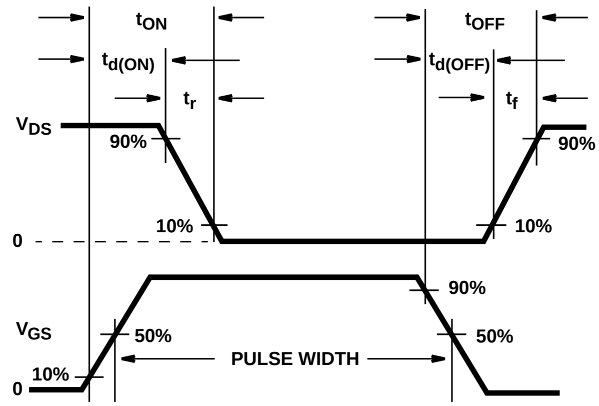


FIGURE 19. RESISTIVE SWITCHING WAVEFORMS

PSPICE Electrical Model

SUBCKT HUF75229P3 2 1 3 ; rev 6/19/97

CA 12 8 1.72e-9
CB 15 14 1.52e-9
CIN 6 8 9.61e-10

DBODY 7 5 DBODYMOD
DBREAK 5 11 DBREAKMOD
DPLCAP 10 5 DPLCAPMOD

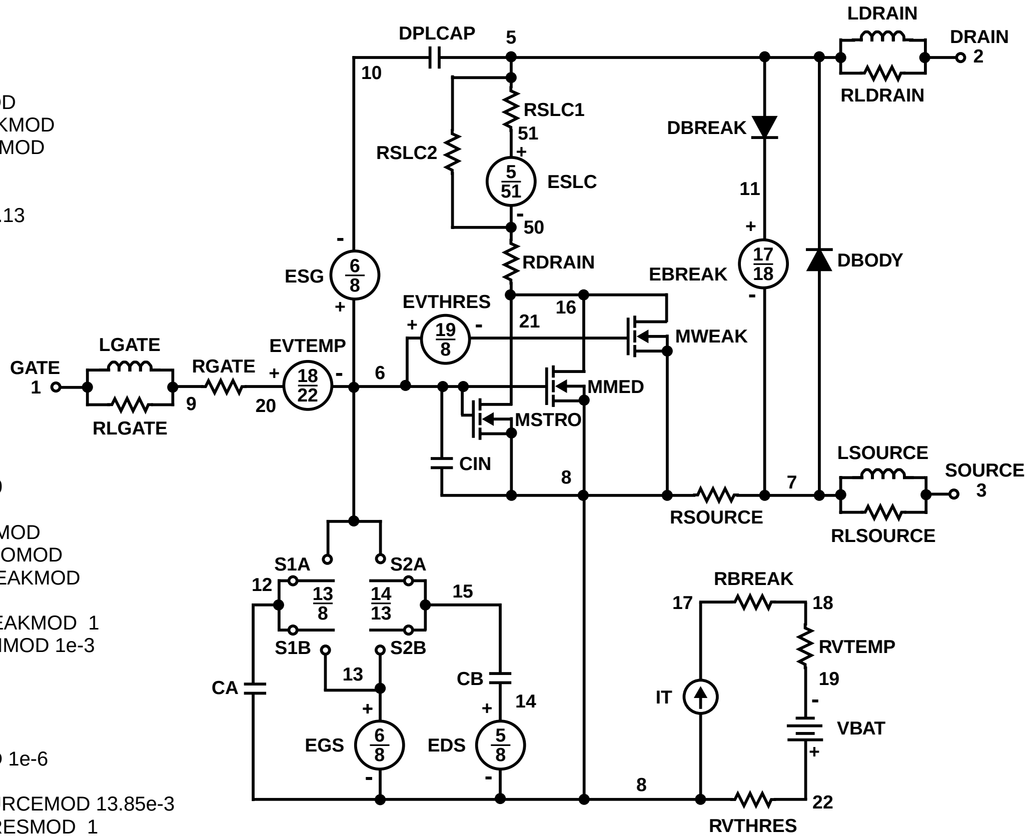
EBREAK 11 7 17 18 58.13
EDS 14 8 5 8 1
EGS 13 8 6 8 1
ESG 6 10 6 8 1
EVTHRES 6 21 19 8 1
EVTEMP 20 6 18 22 1

IT 8 17 1

LDRAIN 2 5 1e-9
LGATE 1 9 2.86e-9
LSOURCE 3 7 2.69e-9

MMED 16 6 8 8 MMEDMOD
MSTRO 16 6 8 8 MSTROMOD
MWEAK 16 21 8 8 MWEAKMOD

RBREAK 17 18 RBREAKMOD 1
RDRAIN 50 16 RDRAINMOD 1e-3
RGATE 9 20 1.52
RLDRAIN 2 5 10
RLGATE 1 9 26.9
RLSOURCE 3 7 28.6
RSLC1 5 51 RSLCMOD 1e-6
RSLC2 5 50 1e3
RSOURCE 8 7 RSOURCEMOD 13.85e-3
RVTHRES 22 8 RVTHRESMOD 1
RVTEMP 18 19 RVTEMPMOD 1



S1A 6 12 13 8 S1AMOD
S1B 13 12 13 8 S1BMOD
S2A 6 15 14 13 S2AMOD
S2B 13 15 14 13 S2BMOD

VBAT 22 19 DC 1

ESLC 51 50 VALUE={(V(5,51)/ABS(V(5,51)))*(PWR(V(5,51)/(1e-6*135),3.5))}

.MODEL DBODYMOD D (IS = 7.50e-13 RS = 5.05e-3 TRS1 = 2.21e-3 TRS2 = 1.02e-6 CJO = 1.51e-9 TT = 4.05e-8 M = 0.5)
.MODEL DBREAKMOD D (RS = 2.14e-1 TRS1 = 9.62e-4 TRS2 = 1.23e-6)
.MODEL DPLCAPMOD D (CJO = 13.5e-10 IS = 1e-30 N = 10 M = 0.85)
.MODEL MMEDMOD NMOS (VTO = 3.25 KP = 2.50 IS = 1e-30 N = 10 TOX = 1 L = 1u W = 1u RG = 1.52)
.MODEL MSTROMOD NMOS (VTO = 3.80 KP = 70.0 IS = 1e-30 N = 10 TOX = 1 L = 1u W = 1u)
.MODEL MWEAKMOD NMOS (VTO = 2.91 KP = 0.06 IS = 1e-30 N = 10 TOX = 1 L = 1u W = 1u RG = 15.2 RS = 0.1)
.MODEL RBREAKMOD RES (TC1 = 1.05e-3 TC2 = 1.94e-7)
.MODEL RDRAINMOD RES (TC1 = 8.04e-2 TC2 = 1.37e-4)
.MODEL RSLCMOD RES (TC1 = 4.83e-3 TC2 = 1.16e-6)
.MODEL RSOURCEMOD RES (TC1 = 0 TC2 = 0)
.MODEL RVTHRESMOD RES (TC = -3.43e-3 TC2 = -1.63e-5)
.MODEL RVTEMPMOD RES (TC1 = -1.35e-3 TC2 = 1.16e-6)

.MODEL S1AMOD VSWITCH (RON = 1e-5 ROFF = 0.1 VON = -7.90 VOFF= -4.90)
.MODEL S1BMOD VSWITCH (RON = 1e-5 ROFF = 0.1 VON = -4.90 VOFF= -7.90)
.MODEL S2AMOD VSWITCH (RON = 1e-5 ROFF = 0.1 VON = -0.50 VOFF= 2.50)
.MODEL S2AMOD VSWITCH (RON = 1e-5 ROFF = 0.1 VON = 2.50 VOFF= -0.50)

.ENDS

NOTE: For further discussion of the PSPICE model, consult **A New PSPICE Sub-Circuit for the Power MOSFET Featuring Global Temperature Options**; IEEE Power Electronics Specialist Conference Records, 1991, written by William J. Hepp and C. Frank Wheatley.

SPICE Thermal Model

REV 16 June 97

HUF75229P3

CTHERM1 7 6 4.90e-7
CTHERM2 6 5 4.90e-4
CTHERM3 5 4 1.96e-3
CTHERM4 4 3 7.90e-3
CTHERM5 3 2 1.85e-1
CTHERM6 2 1 2.70

RTHERM1 7 6 1.10e-2
RTHERM2 6 5 3.30e-2
RTHERM3 5 4 1.64e-1
RTHERM4 4 3 7.90e-1
RTHERM5 3 2 3.60e-1
RTHERM6 2 1 1.60e-1