3-Pin Hotswap Controller

Introduction

The Supertex HV101DB1 demo board contains all necessay circuitry to demonstrate the features of the HV100 hotswap controller. Intended primarily as a negative hotswap controller, the HV101 controls the negative supply path.

Included on board is a 100µF capacitor (C_3) to provide a capacitive load for testing. Additional capacitance may be connected to the V_{OUT} terminals. Or the 100µF may be removed altogether

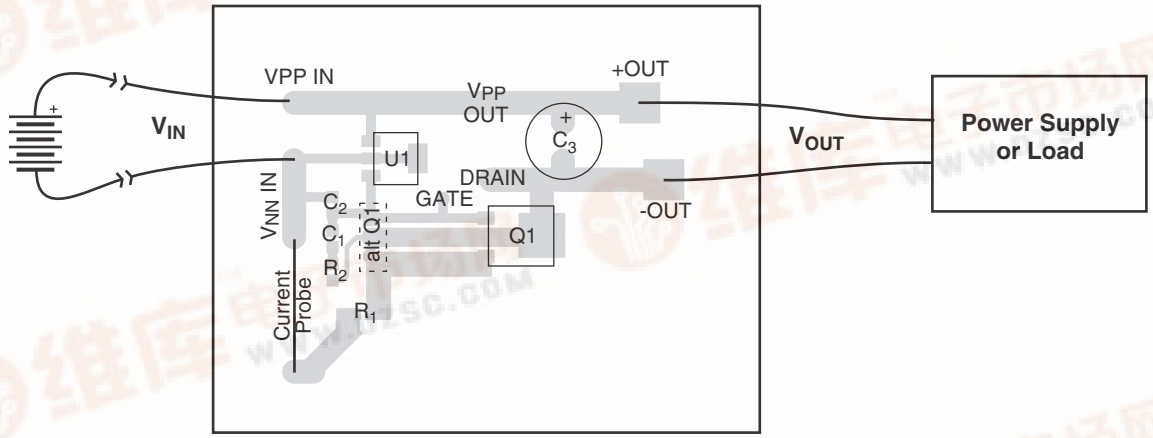
The board may be modified to meet custom requirements. Instructions are provided on the next page for modifications.

Specifications

Input Voltage	10V to 72V
Peak Inrush Limit	1.4A typ
Max Short Circuit Current[1]	4A typ
Circuit Breaker Response Time[1]	1ms typ
Auto Retry	2.5s typ
On Resistance	210mW_ max
Undervoltage Trip	15V on, 14V off

[1] *During inrush limiting*

Board Layout and Connections



V_{IN}

Connect the supply voltage to these terminals. Supply voltage may range from 10 volts to 72 volts.

A high source impedance may cause oscillations when the input voltage is near the undervoltage trip point. A high source impedance results in a large voltage drop when loaded, causing undervoltage lockout to kick in, disconnecting the load. With the load removed, input voltage rises, causing undervoltage to release and reconnecting the load. The cycle repeats, resulting in oscillations. Source impedance must be less than the following to avoid oscillations:

$$R_{SOURCE} = \frac{1.5V}{I_{LOAD}}$$

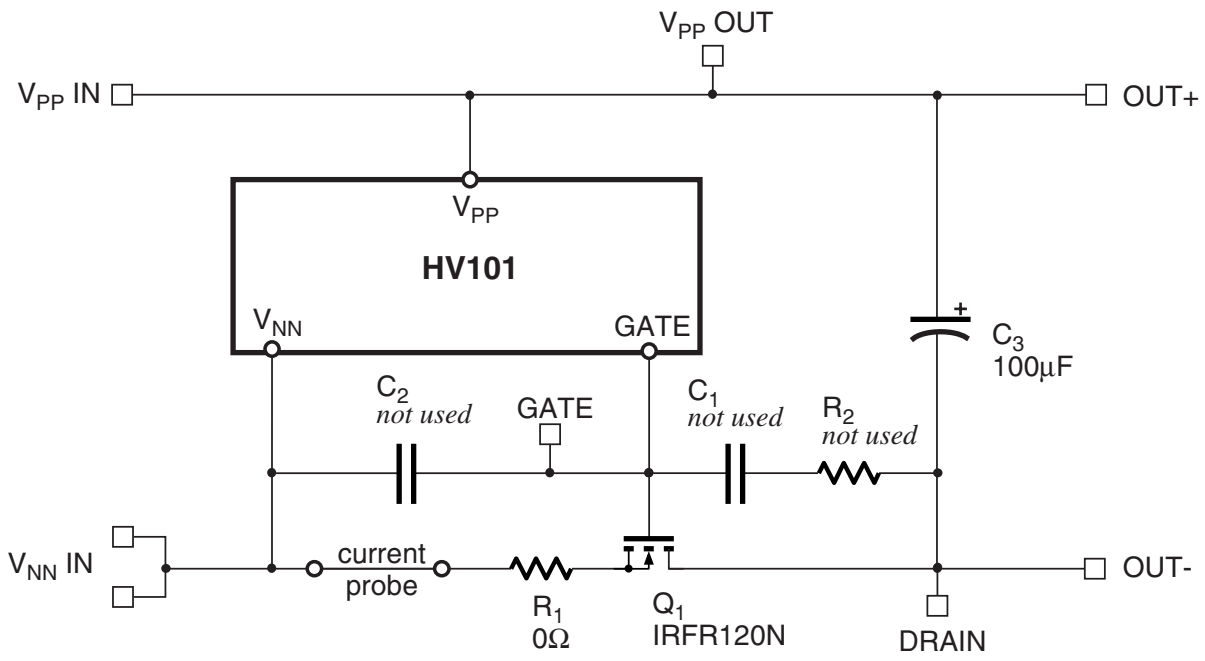
V_{OUT}

Connect the power supply or other load to these terminals. V_{OUT+} is connected to V_{IN+}, it is V_{OUT-} that is switched.

Application of a DC load during start-up and/or additional load capacitance extends the time inrush limiting is active. If this time exceeds 100ms, the HV101 shuts off, retrying 2.5s later. For this reason, DC load at start-up should be less than 900mA. Note that DC start-up load limitation decreases with added load capacitance.

Note that the circuit breaker functions during inrush only.

HV101 Demo Board Schematic



A very high dV/dt on the input can overload the HV101's internal gate clamp, causing turn-on transients. A capacitor in the C_2 position may be used to clamp the gate, preventing the transients. A 1nF value is usually adequate. Voltage rating should be 16 volts.

To limit short-at-turn-on current, zero-ohm resistor R_1 may be replaced with a low value resistor. This resistor causes a voltage drop that tends to cancel-out the applied gate voltage, thus limiting drain current.

To reduce peak inrush current, a capacitor from gate to drain (C_1) may be employed. A resistor (R_2) is also needed in this configuration for loop stability. Please refer to the HV101 data sheet for further information.

Note: When making positive-ground measurements, scope probe loading on the GATE pin may interfere with normal operation. To observe gate voltages, use negative-ground measurements.