

# Low Charge Injection 8-Channel High Voltage Analog Switch

## Features

- HVCMOS technology for high performance
- Very low quiescent power dissipation-10 $\mu$ A
- Output On-resistance typically 11 $\Omega$
- Low parasitic capacitance
- DC to 10MHz analog signal frequency
- -60dB typical off-isolation at 5MHz
- CMOS logic circuitry for low power
- Excellent noise immunity
- Serial shift register logic control with latches
- Flexible operating supply voltages
- Surface mount packages

## Applications

- Medical Ultrasound Imaging
- Non-Destructive Evaluation

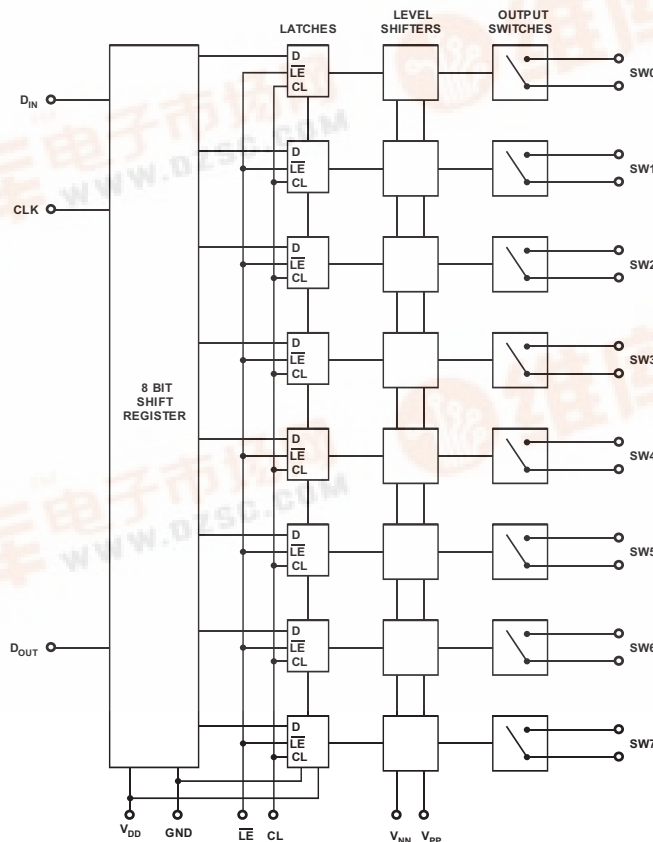
## General Description

The Supertex HV219 is a low switch resistance, low charge injection 8-channel 200V analog switch integrated circuit (IC) intended primarily for medical ultrasound imaging. The device can also be used for NDE, non-destructive evaluation applications. The HV219 is a lower switch resistance, 11ohms versus 22ohms, version of the Supertex HV20220 device. The lower switch resistance will help reduce insertion loss. It has the same pin configuration as that of the Supertex HV20220PJ and the HV20220FG.

The device is manufactured using Supertex's HVCMOS (high voltage CMOS) technology with high voltage bilateral DMOS structures for the outputs and low voltage CMOS logic for the input control. The outputs are configured as eight independent single pole single throw 11 ohms analog switches. The input logic is an 8-bit serial to parallel shift register followed by an 8-bit parallel latch. The switch states are determined by the data in the latch. Logic high will correspond to a closed switch and logic low as an opened switch.

The HV219 is designed to operate on various combinations of high voltage supplies. For example the  $V_{PP}$  and  $V_{NN}$  supplies can be: +40V/-160V, +100V/-100V, or +160V/-40V. This allows the user to maximize the signal voltage for uni-polar negative, bi-polar, or uni-polar positive.

## Block Diagram



## Ordering Information

$V_{PP}-V_{NN}$	Maximum Analog Switch Voltage	Package Options		
		28-lead plastic chip carrier PLCC	48-lead TQFP	Die
200V	180V <sub>P-P</sub>	HV219PJ	HV219FG	HV219X

## Absolute Maximum Ratings\*

$V_{DD}$ Logic supply	-0.5V to +15V	
$V_{PP}-V_{NN}$ differential supply	220V	
$V_{PP}$ Positive supply	-0.5V to $V_{NN}+200V$	
$V_{NN}$ Negative supply	+0.5V to -200V	
Logic input voltage	-0.5V to $V_{DD}+0.3V$	
Analog signal range	$V_{NN}$ to $V_{PP}$	
Peak analog signal current	3.0A	
Storage temperature	-65°C to +125°C	
Power dissipation	28-Lead PLCC	1.2W
	48 Lead TQFP	1.0W

\*Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied. Continuous operation of the device at the absolute rating level may affect device reliability. All voltages are referenced to device ground.

## Operating Conditions

Symbol	Parameter	Value
$V_{DD}$	Logic power supply	4.5V to 13.2V
$V_{PP}$	Positive high voltage supply	40V to $V_{NN}+200V$
$V_{NN}$	Negative high voltage supply	-40V to -160V
$V_{IH}$	Input logic voltage high	$V_{DD}-1.5V$ to $V_{DD}$
$V_{IL}$	Input logic voltage low	0V to 1.5V
$V_{SIG}$	Analog signal voltage peak to peak	$V_{NN}+10V$ to $V_{PP}-10V$
$T_A$	Operating free air temperature	0°C to 70°C

## Electrical Characteristics

### DC Characteristics *(over recommended operating conditions unless otherwise noted)*

Sym	Parameter	0°C		+25°C			+70°C		Units	Conditions	
		Min	Max	Min	Typ	Max	Min	Max			
R <sub>ONS</sub>	Small Signal Switch On-Resistance		15		13	19		24	Ohms	I <sub>SIG</sub> = 5mA	V <sub>PP</sub> = +40V
			13		11	14		16		I <sub>SIG</sub> = 200mA	V <sub>NN</sub> = -160V
			13		11	14		15		I <sub>SIG</sub> = 5mA	V <sub>PP</sub> = +100V
			9		9	12		14		I <sub>SIG</sub> = 200mA	V <sub>NN</sub> = -100V
			12		10	13		15		I <sub>SIG</sub> = 5mA	V <sub>PP</sub> = +160V
			11		8	13		14		I <sub>SIG</sub> = 200mA	V <sub>NN</sub> = -40V
ΔR <sub>ONS</sub>	Small Signal Switch On-Resistance Matching		20		5.0	20		20	%	I <sub>SIG</sub> = 5mA, V <sub>PP</sub> = +100V, V <sub>NN</sub> = -100V	
R <sub>ONL</sub>	Large Signal Switch On-Resistance				8				Ohms	V <sub>SIG</sub> = V <sub>PP</sub> -10V, I <sub>SIG</sub> = 1A	
I <sub>SOL</sub>	Switch Off Leakage per Switch		5.0		1.0	10		15	μA	V <sub>SIG</sub> = V <sub>PP</sub> -10V and V <sub>NN</sub> +10V	
	DC offset Switch off		300		100	300		300	mV	R <sub>LOAD</sub> = 100KΩ	
	DC offset Switch on		500		100	500		500	mV	R <sub>LOAD</sub> = 100KΩ	
I <sub>PPQ</sub>	Quiescent V <sub>PP</sub> supply current				10	50			μA	All switches off	
I <sub>NNQ</sub>	Quiescent V <sub>NN</sub> supply current				-10	-50			μA	All switches off	
I <sub>PPQ</sub>	Quiescent V <sub>PP</sub> supply current				10	50			μA	All switches on, I <sub>SW</sub> = 5mA	
I <sub>NNQ</sub>	Quiescent V <sub>NN</sub> supply current				-10	-50			μA	All switches on, I <sub>SW</sub> = 5mA	
	Switch output peak current		3.0		3.0	2.0		2.0	A	V <sub>SIG</sub> duty cycle < 0.1%	
f <sub>SW</sub>	Output switch frequency					50			kHz	Duty cycle = 50%	
I <sub>PP</sub>	Average V <sub>PP</sub> supply current		6.5			7.0		8.0	mA	V <sub>PP</sub> = +40V	All output switches are turning On and Off at 50KHz with no load.
			4.0			5.0		5.5		V <sub>NN</sub> = -160V	
			4.0			5.0		5.5		V <sub>PP</sub> = +100V V <sub>NN</sub> = -100V	
I <sub>NN</sub>	Average V <sub>NN</sub> supply current		6.5			7.0		8.0	mA	V <sub>PP</sub> = +160V	
			4.0			5.0		5.5		V <sub>NN</sub> = -40V	
			4.0			5.0		5.5		V <sub>PP</sub> = +100V V <sub>NN</sub> = -100V	
	4.0			5.0		5.5	V <sub>PP</sub> = +160V V <sub>NN</sub> = -40V				
I <sub>DD</sub>	Average V <sub>DD</sub> supply current		4.0			4.0		4.0	mA	f <sub>CLK</sub> = 5MHz, V <sub>DD</sub> = 5.0V	
I <sub>DDQ</sub>	Quiescent V <sub>DD</sub> supply current		10			10		10	μA	All logic inputs are static	
I <sub>SOR</sub>	Data out source current	0.45		0.45	0.70		0.40		mA	V <sub>OUT</sub> = V <sub>DD</sub> -0.7V	
I <sub>SINK</sub>	Data out sink current	0.45		0.45	0.70		0.40		mA	V <sub>OUT</sub> = 0.7V	
C <sub>IN</sub>	Logic input capacitance		10			10		10	pF		

## Electrical Characteristics

### AC Characteristics *(over recommended operating conditions, $V_{DD}=5.0V$ , unless otherwise noted)*

Sym	Parameter	0°C		+25°C			+70°C		Unit	Conditions
		Min	Max	Min	Typ	Max	Min	Max		
$t_{SD}$	Set Up Time Before $\overline{LE}$ Rises	150		150			150		ns	
$t_{WLE}$	Time Width of $\overline{LE}$	150		150			150		ns	
$t_{DO}$	Clock Delay Time to Data out		150			150		150	ns	
$t_{WCL}$	Time Width of CL	150		150			150		ns	
$t_{SU}$	Set Up Time Data to Clock	15		15	8.0		20		ns	
$t_H$	Hold Time Data from Clock	35		35			35		ns	
$f_{CLK}$	Clock Frequency		5.0			5.0		5.0	MHz	50% duty cycle, $f_{DATA} = f_{CLK}/2$
$t_{r,tf}$	Clock rise and fall Times		50			50		50	ns	
$T_{on}$	Turn on Time		5.0			5.0		5.0	$\mu s$	$V_{SIG} = V_{PP}-10V$ , $R_{LOAD} = 10K\Omega$
$T_{off}$	Turn off Time		5.0			5.0		5.0	$\mu s$	$V_{SIG} = V_{PP}-10V$ , $R_{LOAD} = 10K\Omega$
dv/dt	Maximum $V_{SIG}$ Slew Rate		20			20		20	V/ns	$V_{PP} = +40V$ , $V_{NN} = -160V$
			20			20		20		$V_{PP} = +100V$ , $V_{NN} = -100V$
			20			20		20		$V_{PP} = +160V$ , $V_{NN} = -40V$
KO	Off Isolation	-30		-30	-33		-30		dB	$F = 5MHz$ , $1K\Omega/15pF$ load
		-58		-58			-58			$F = 5.0MHz$ , $50\Omega$ load
Kcr	Switch Crosstalk			-60					dB	$F = 5.0MHz$ , $50\Omega$ load
I <sub>id</sub>	Output Switch Isolation Diode Current		300			300		300	mA	300ns pulse width, 2.0% duty cycle
$C_{SG(off)}$	Off Capacitance SW to Gnd	14	25	14	20	25	14	25	pF	0V, $f = 1MHz$
$C_{SG(on)}$	On Capacitance SW to Gnd	40	60	40	50	60	40	60	pF	0V, $f = 1MHz$
+ $V_{SPK}$	Output Voltage Spike					150			mV	$V_{PP} = +40V$ , $V_{NN} = -160V$ , $R_{LOAD} = 50ohm$
- $V_{SPK}$						200				
+ $V_{SPK}$						150			mV	$V_{PP} = +100V$ , $V_{NN} = -100V$ , $R_{LOAD} = 50ohm$
- $V_{SPK}$						200				
+ $V_{SPK}$						150			mV	$V_{PP} = +160V$ , $V_{NN} = -40V$ , $R_{LOAD} = 50ohm$
- $V_{SPK}$						200				
Q	Charge Injection				1450				pC	$V_{PP} = +40V$ , $V_{NN} = -160V$ , $V_{SIG} = 0V$
					1050					$V_{PP} = +100V$ , $V_{NN} = -100V$ , $V_{SIG} = 0V$
					550					$V_{PP} = +160V$ , $V_{NN} = -40V$ , $V_{SIG} = 0V$

## Power Up/Down Sequence

- 1) Power up/down sequence is arbitrary except GND must be powered up first and powered down last. This applies for applications powering GND of the IC with different voltages.
- 2) Vsig must always be at or in between V<sub>PP</sub> and V<sub>NN</sub> or floating during power up/down transition.
- 3) Rise and fall times of the power supplies V<sub>DD</sub>, V<sub>PP</sub>, and V<sub>NN</sub> should not be less than 1.0ms.

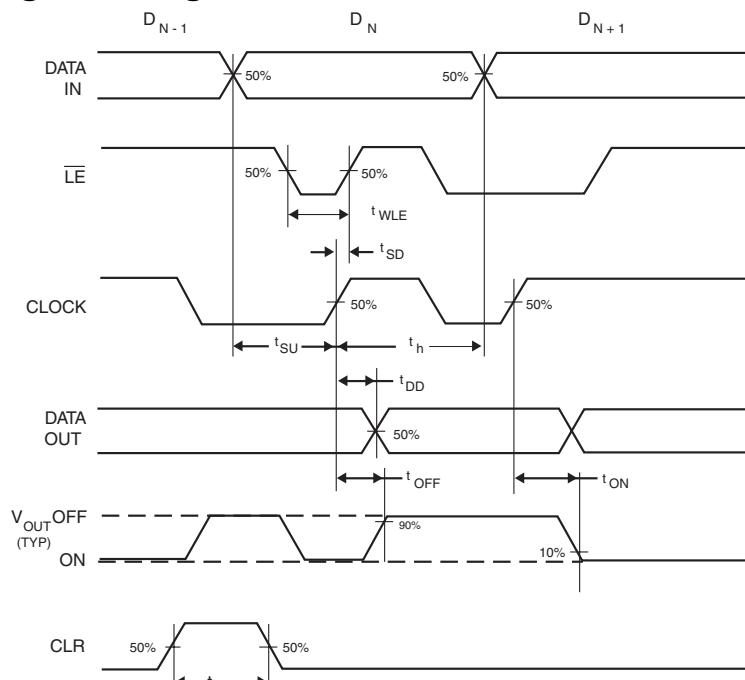
## Logic Truth Table

Data in the 8-bit Shift Register								$\overline{LE}$	CL	Output Switch State							
D0	D1	D2	D3	D4	D5	D6	D7			SW0	SW1	SW2	SW3	SW4	SW5	SW6	SW7
L								L	L	OFF							
H								L	L	ON							
	L							L	L		OFF						
	H							L	L		ON						
		L						L	L			OFF					
		H						L	L			ON					
			L					L	L				OFF				
			H					L	L				ON				
				L				L	L					OFF			
				H				L	L					ON			
					L			L	L						OFF		
					H			L	L						ON		
						L		L	L							OFF	
						H		L	L							ON	
X	X	X	X	X	X	X	X	H	L	HOLD PREVIOUS STATE							
X	X	X	X	X	X	X	X	X	H	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF

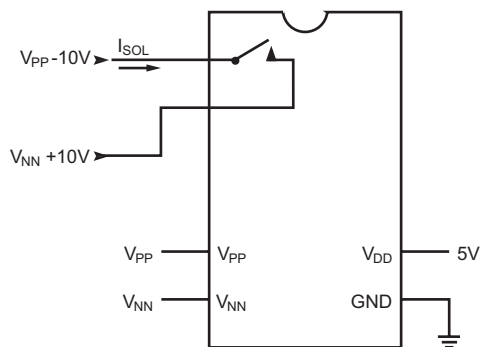
### Notes:

1. The eight switches operate independently.
2. Serial data is clocked in on the L to H transition clock.
3. The switches go to a state retaining their present condition at the rising edge of the  $\overline{LE}$ .
4. When  $\overline{LE}$  is low, the shift register data flows through the latch.
5. Shift register clocking has no effect on the switch states if  $\overline{LE}$  is high.
6. The clear input overrides all other inputs.

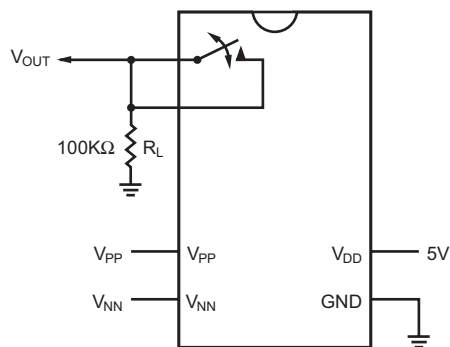
## Logic Timing Waveform



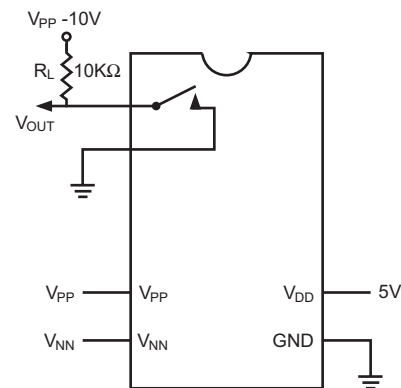
## Test Circuits



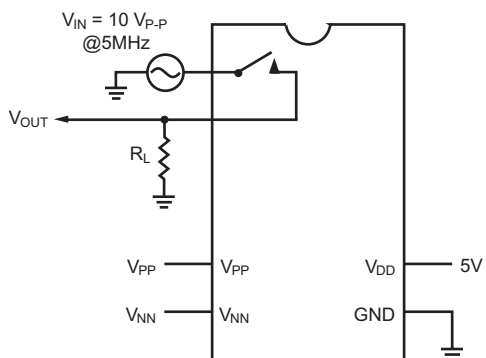
Switch OFF Leakage



DC Offset ON/OFF

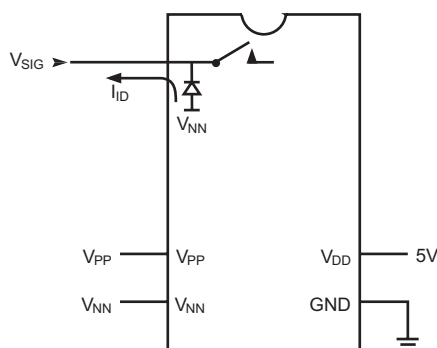


T<sub>ON</sub>/T<sub>OFF</sub> Test Circuit

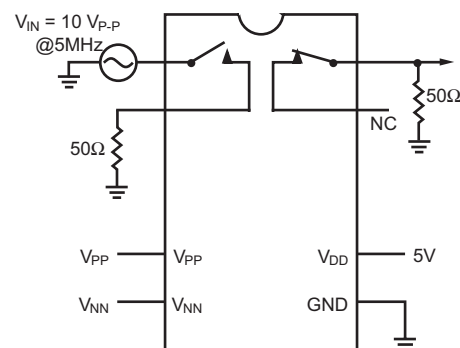


$$K_O = 20 \log \frac{V_{OUT}}{V_{IN}}$$

OFF Isolation

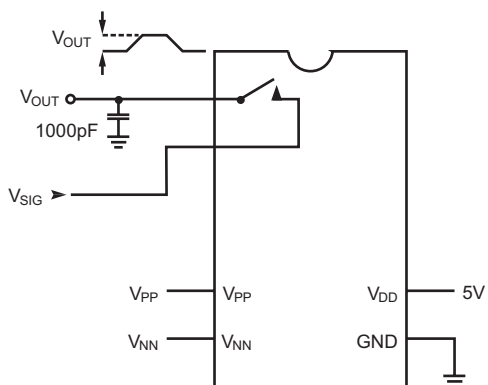


Isolation Diode Current



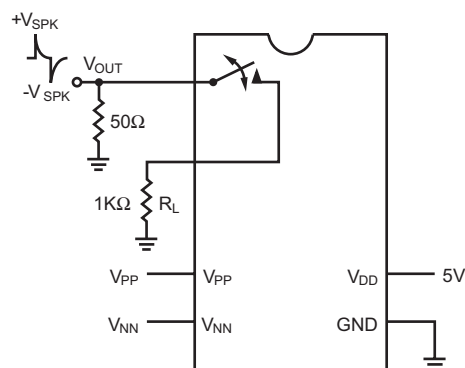
$$K_{CR} = 20 \log \frac{V_{OUT}}{V_{IN}}$$

Crosstalk



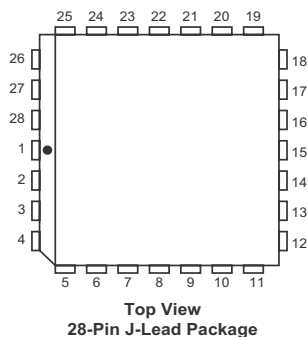
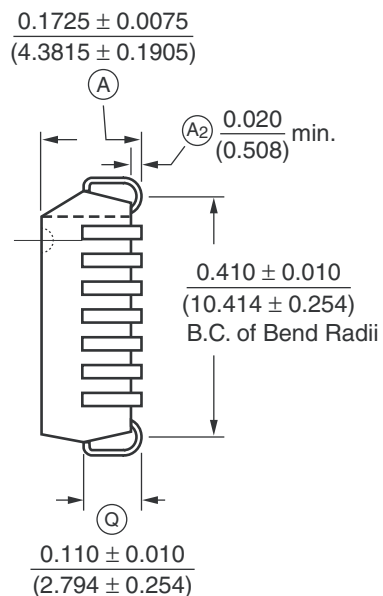
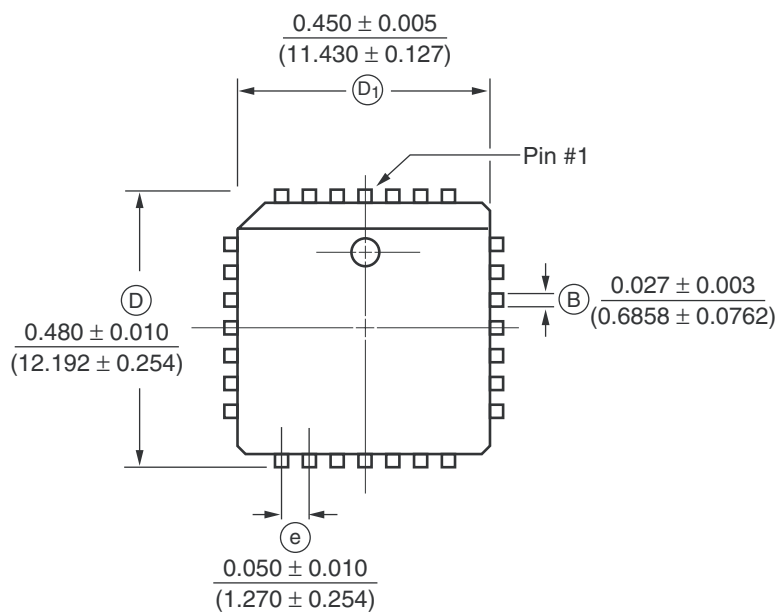
$$Q = 1000\text{pF} \times V_{OUT}$$

Charge Injection



Output Voltage Spike

## 28-Pin J-lead Package Outline



## Pin Configuration

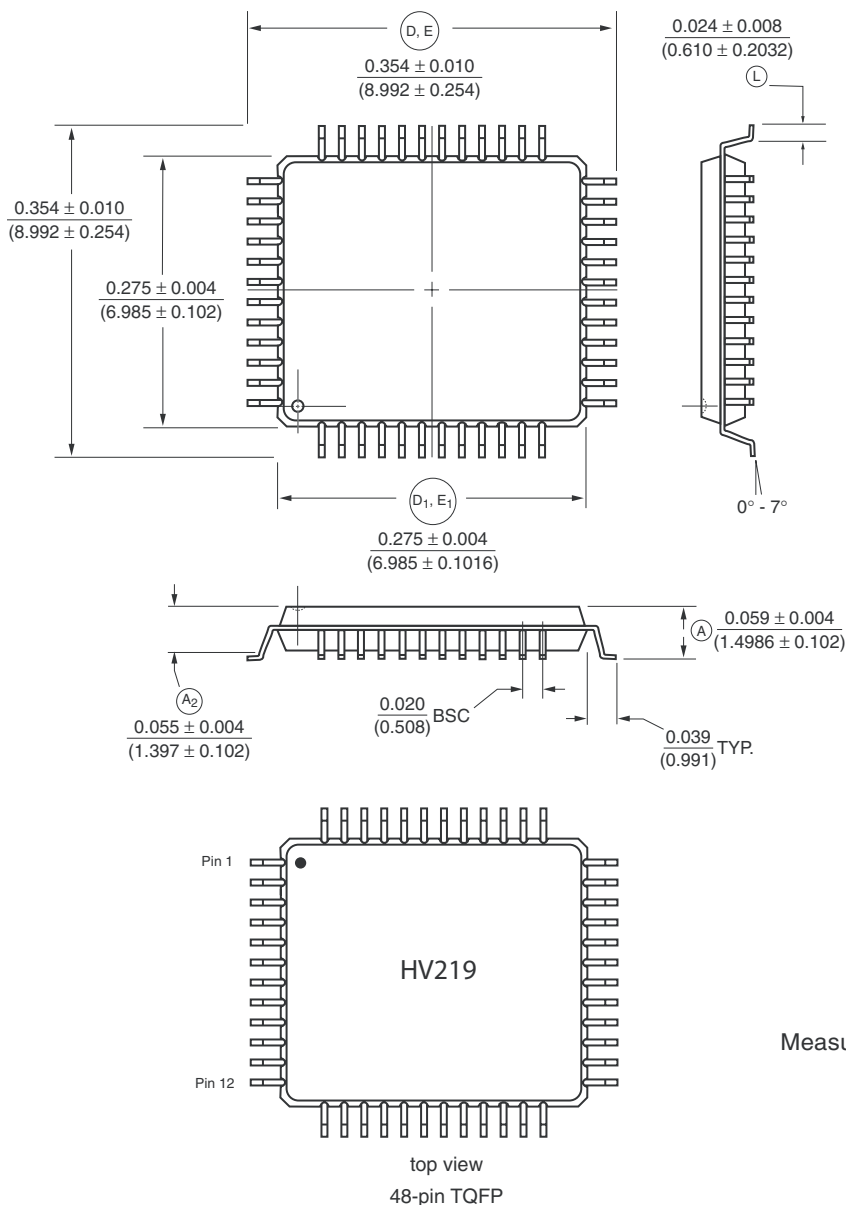
### 28 Pin J-Lead

Pin	Function	Pin	Function
1	SW3	15	N/C
2	SW3	16	D <sub>IN</sub>
3	SW2	17	CLK
4	SW2	18	LE
5	SW1	19	CL
6	SW1	20	D <sub>OUT</sub>
7	SW0	21	SW7
8	SW0	22	SW7
9	N/C	23	SW6
10	V <sub>PP</sub>	24	SW6
11	N/C	25	SW5
12	V <sub>NN</sub>	26	SW5
13	GND	27	SW4
14	V <sub>DD</sub>	28	SW4

Measurement Legend =  $\frac{\text{Dimensions in Inches}}{\text{(Dimensions in Millimeters)}}$

## 48-Pin TQFP

## Pin Configuration



### 48-Pin TQFP

Pin	Function	Pin	Function
1	SW5	25	$V_{NN}$
2	N/C	26	N/C
3	SW4	27	N/C
4	N/C	28	GND
5	SW4	29	$V_{DD}$
6	N/C	30	N/C
7	N/C	31	N/C
8	SW3	32	N/C
9	N/C	33	$D_{IN}$
10	SW3	34	CLK
11	N/C	35	$\overline{LE}$
12	SW2	36	CLR
13	N/C	37	$D_{OUT}$
14	SW2	38	N/C
15	N/C	39	SW7
16	SW1	40	N/C
17	N/C	41	SW7
18	SW1	42	N/C
19	N/C	43	SW6
20	SW0	44	N/C
21	N/C	45	SW6
22	SW0	46	N/C
23	N/C	47	SW5
24	$V_{PP}$	48	N/C

Measurement Legend =  $\frac{\text{Dimensions in Inches}}{\text{(Dimensions in Millimeters)}}$

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