HVL3224QE
LCD CONTROLLER

May/30//2003

■ GENERAL DESCRIPTION

The HYVIX-MAIN-R003, color-graphics LCD controller board displays 320-by-240 dot graphics for 65K STN colors. A 16-bit high-speed bus interface and external high-speed SRAM write function enable efficient data transfers and high-speed rewriting of data to the graphics RAM. The feature of this product is less afterimage than old product and possible 2 mode programming (pixel mode, block mode).

The HVL3224QE is suitable for any mid-sized product, such as PDA, digital camera, GPS and DVD/VCD player.

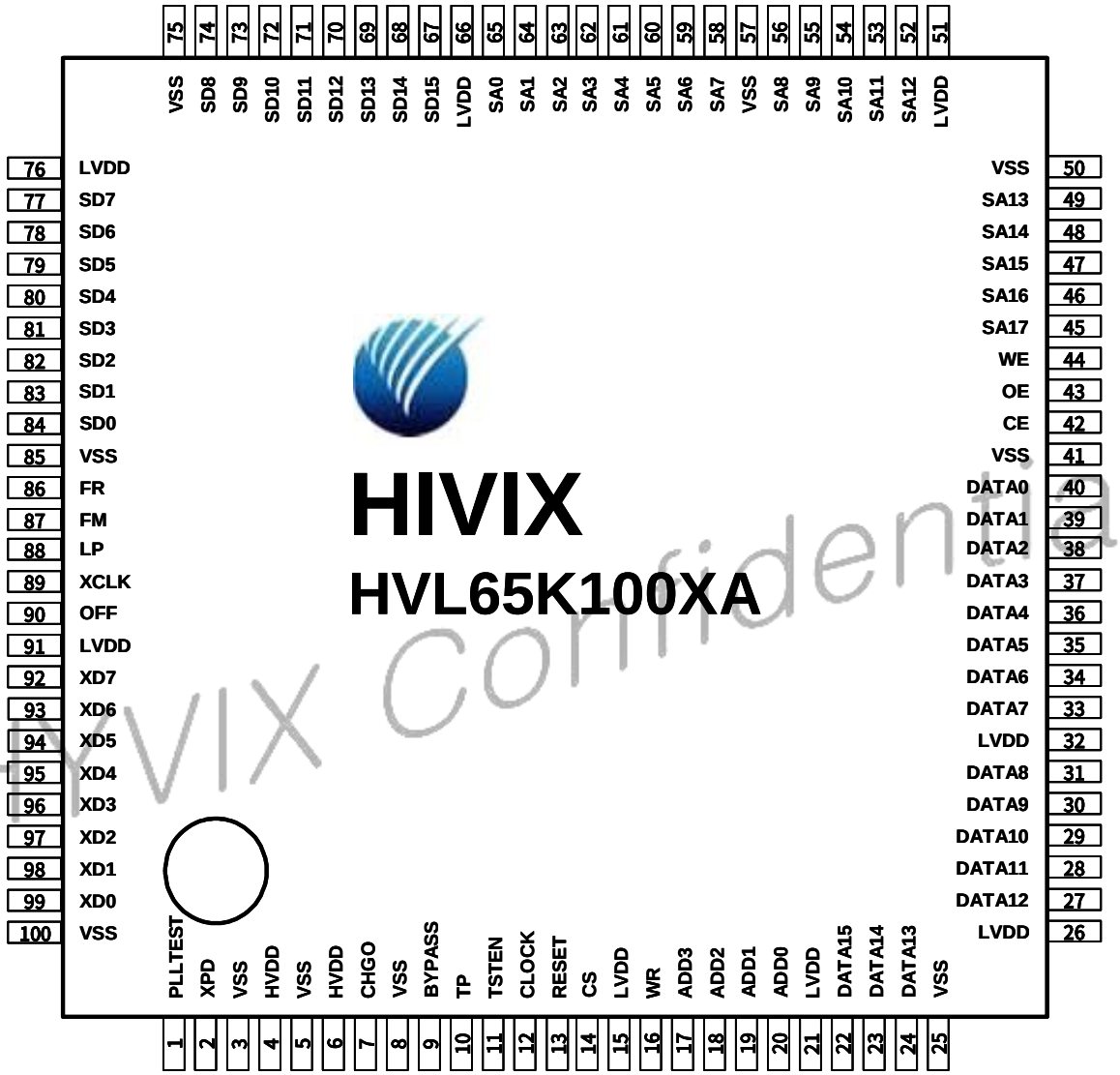
100 Pin TQFP

■ FEATURES

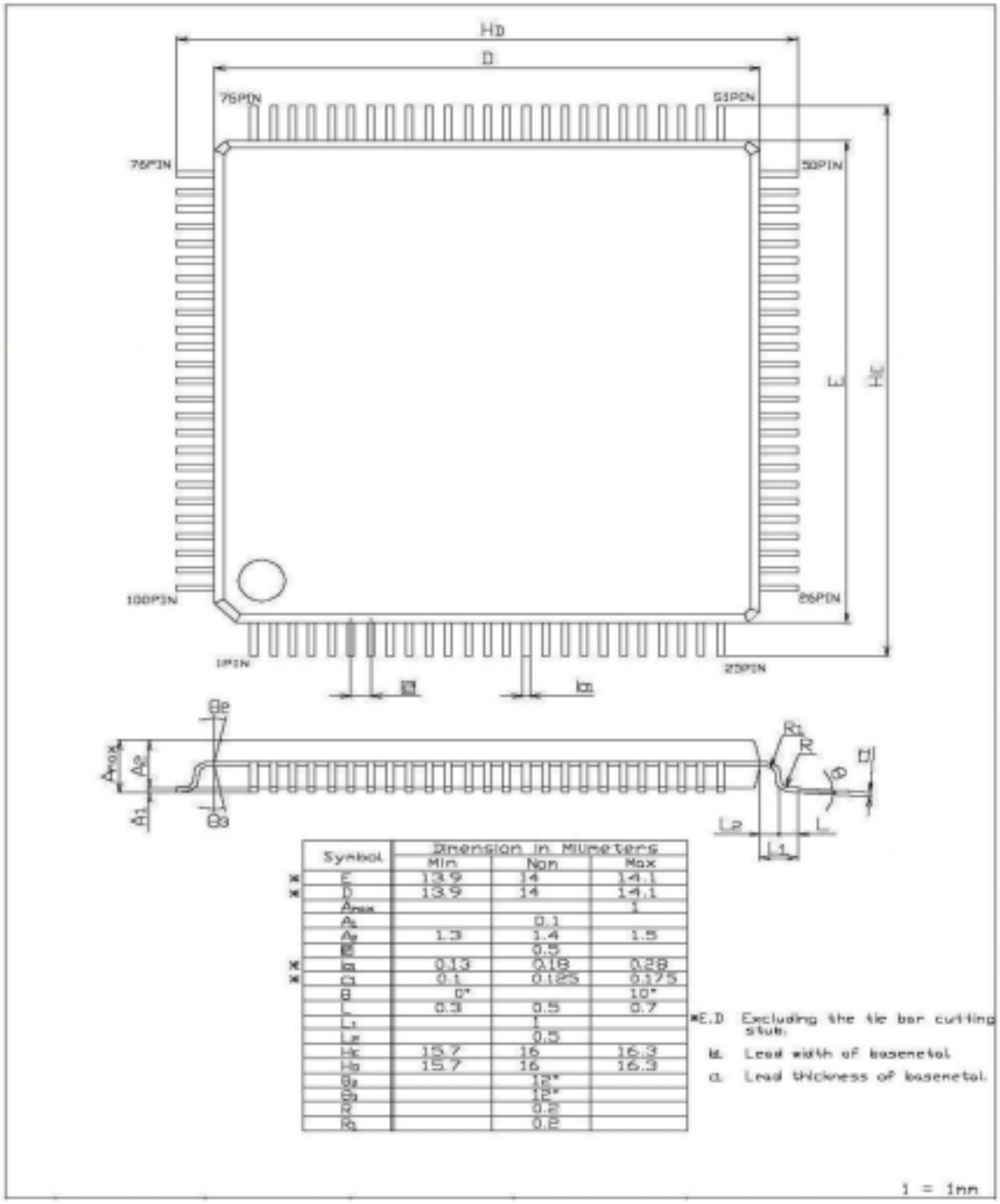
The HVL3224QE has the following features:

- 65K color bitmap STN-LCD display controller
- Max 30 frames
- RGB (5:6:5) format
- 16 bit BUS interface
- Less afterimage than old product
- Max display area (Horizontal 320 lines × Vertical 240 lines)
- LCD panel interface(frame, line, data 4 or 8 bits, clock(latch pulse), dispoff, bias)
- External frame memory interface (SRAM)
- Moving picture for the general color STN LCD panel
- Any size support within the max size
- Color inverting
- Display On/Off
- Flexible display resolution
- Display data writing start line and column address set
- Pixel write and block write
- Bias selection
- Logic supply (3.3V)
- C-MOS silicon process
- Low current consumption
- Package (100 pin TQFP)

■ PIN ASSIGNMENT - 100 TQFP



■ PIN DEMENSION



Symbol	Dimension in Milimeters		
	Min	Nom	Max
** E	13.9	14	14.1
** D	13.9	14	14.1
Amax			1
A1		0.1	
A2	1.3	1.4	1.5
e		0.5	
** bp	0.13	0.18	0.28
c1	0.1	0.125	0.175
θ	0°		10°
L	0.3	0.5	0.7
L1		1	
L2		0.5	
HE	15.7	16	16.3
HD	15.7	16	16.3
θ2		12°	
θ3		12°	
c		0.2	
R1		0.2	

*E,D Excluding the tie bar cutting stub.
bp Lead width of basemetal
c1 Lead thickness of basemetal

1 = 1mm

■ PIN DESCRIPTION

Signals	PIN NO.	I/O	Connected to	Functions
PLL TEST	1	INPUT	N. C.	For PLL Test
XPD	2	INPUT	N. C.	For PLL Test
VSS	3	VSS	GND	Common Ground
HVDD	4	VDD	3.3V	Power Supply for logic circuits(3.3V)
VSS	5	VSS	GND	Common Ground
HVDD	6	VDD	3.3V	Power Supply for logic circuits(3.3V)
CHGO	7		N. C.	For PLL Test
VSS	8	VSS	GND	Common Ground
BYPASS	9	INPUT	N. C.	For PLL Test
TP	10	INPUT	N. C.	For Chip Debugging
TSTEN	11	INPUT	N. C.	For Chip Debugging
CLOCK	12	INPUT		Main Clock
RESET	13	INPUT		Chip Reset
CS	14	INPUT	MPU	External Interface Chip select, Active "0"
LVDD	15	VDD	3.3V	Power Supply for logic circuits(3.3V)
WR	16	INPUT	MPU	Chip Write Signal
ADD3	17	INPUT	MPU	External Interface Address Input port
ADD2	18	INPUT	MPU	
ADD1	19	INPUT	MPU	
ADD0	20	INPUT	MPU	
LVDD	21	VDD	3.3V	Power Supply for logic circuits(3.3V)
DATA15	22	INPUT	MPU	External Data I/O port
DATA14	23	INPUT	MPU	
DATA13	24	INPUT	MPU	
VSS	25	VSS	GND	Common Ground
LVDD	26	VDD	3.3V	Power Supply for logic circuits(3.3V)
DATA12	27	INPUT	MPU	External Data I/O port
DATA11	28	INPUT	MPU	
DATA10	29	INPUT	MPU	
DATA9	30	INPUT	MPU	
DATA8	31	INPUT	MPU	
LVDD	32	VDD	3.3V	Power Supply for logic circuits(3.3V)
DATA7	33	INPUT	MPU	External Data I/O port
DATA6	34	INPUT	MPU	
DATA5	35	INPUT	MPU	
DATA4	36	INPUT	MPU	

DATA3	37	INPUT	MPU	External Data I/O port
DATA2	38	INPUT	MPU	
DATA1	39	INPUT	MPU	
DATA0	40	INPUT	MPU	
VSS	41	VSS	GND	Common Ground
CE	42	OUTPUT		SRAM Chip Enable, Active "0"
OE	43	OUTPUT	EXT. SRAM	SRAM Output Enable, Active "0"
WE	44	OUTPUT	EXT. SRAM	SRAM Write Enable, Active "0"
SA17	45	OUTPUT	EXT. SRAM	SRAM Address Output port
SA16	46	OUTPUT	EXT. SRAM	
SA15	47	OUTPUT	EXT. SRAM	
SA14	48	OUTPUT	EXT. SRAM	
SA13	49	OUTPUT	EXT. SRAM	
VSS	50	VSS	GND	Common Ground
LVDD	51	VDD	3.3V	Power Supply for logic circuits(3.3V)
SA12	52	OUTPUT	EXT. SRAM	SRAM Address Output port
SA11	53	OUTPUT	EXT. SRAM	
SA10	54	OUTPUT	EXT. SRAM	
SA9	55	OUTPUT	EXT. SRAM	
SA8	56	OUTPUT	EXT. SRAM	
VSS	57	VSS	GND	Common Ground
SA7	58	OUTPUT	EXT. SRAM	SRAM Address Output port
SA6	59	OUTPUT	EXT. SRAM	
SA5	60	OUTPUT	EXT. SRAM	
SA4	61	OUTPUT	EXT. SRAM	
SA3	62	OUTPUT	EXT. SRAM	
SA2	63	OUTPUT	EXT. SRAM	
SA1	64	OUTPUT	EXT. SRAM	
SA0	65	OUTPUT	EXT. SRAM	
LVDD	66	VDD	3.3V	Power Supply for logic circuits(3.3V)
SD15	67	BID	EXT. SRAM	SRAM Data I/O port
SD14	68	BID	EXT. SRAM	
SD13	69	BID	EXT. SRAM	
SD12	70	BID	EXT. SRAM	
SD11	71	BID	EXT. SRAM	
SD10	72	BID	EXT. SRAM	
SD9	73	BID	EXT. SRAM	

SD8	74	BID	EXT. SRAM	SRAM Data I/O port
VSS	75	VSS	GND	Common Ground
LVDD	76	VDD	3.3V	Power Supply for logic circuits(3.3V)
SD7	77	BID	EXT. SRAM	SRAM Data I/O port
SD6	78	BID	EXT. SRAM	
SD5	79	BID	EXT. SRAM	
SD4	80	BID	EXT. SRAM	
SD3	81	BID	EXT. SRAM	
SD2	82	BID	EXT. SRAM	
SD1	83	BID	EXT. SRAM	
SD0	84	BID	EXT. SRAM	
VSS	85	VSS	GND	Common Ground
FR	86	OUTPUT	LCM	LCD Bias Signal
FM	87	OUTPUT	LCM	LCD Synchronous Signal for driving scanning line
LP	88	OUTPUT	LCM	LCD Data Signal Latch Clock
XCLK	89	OUTPUT	LCM	LCD Data Signal Shift Clock
OFF	90	OUTPUT	LCM	LCD OFF
LVDD	91	VDD	3.3V	Power Supply for logic circuits(3.3V)
XD7	92	OUTPUT	LCM	LCD Display Data Output port
XD6	93	OUTPUT	LCM	
XD5	94	OUTPUT	LCM	
XD4	95	OUTPUT	LCM	
XD3	96	OUTPUT	LCM	
XD2	97	OUTPUT	LCM	
XD1	98	OUTPUT	LCM	
XD0	99	OUTPUT	LCM	
VSS	100	VSS	GND	Common Ground

■ PIN CROSS REFERENCE : NUMERICAL ORDER BY PIN NUMBER

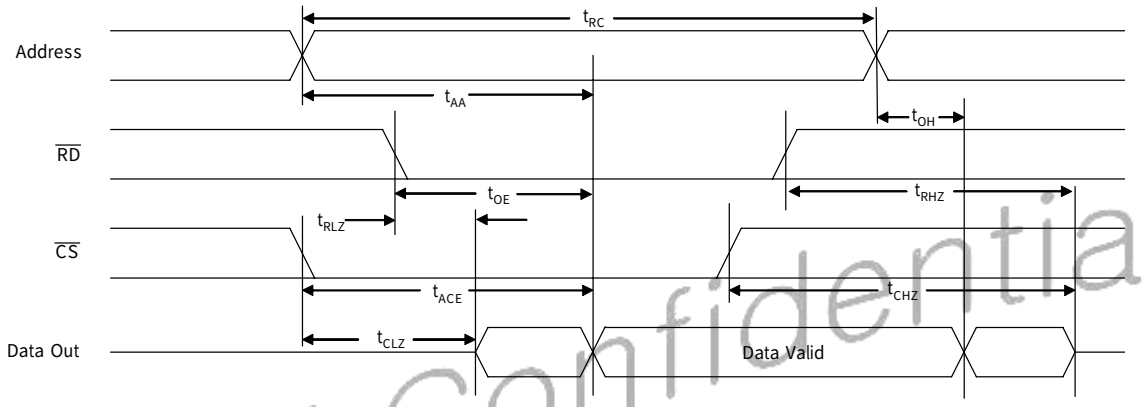
PIN #	PIN NAME	PIN #	PIN NAME	PIN #	PIN NAME	PIN #	PIN NAME
1	PLLTEST	26	VCCINT	51	VCCINT	76	VCCINT
2	XPD	27	DATA12	52	SA12	77	SD7
3	VSS	28	DATA11	53	SA11	78	SD6
4	MVDD	29	DATA10	54	SA10	79	SD5
5	VSS	30	DATA9	55	SA9	80	SD4
6	AVDD	31	DATA8	56	SA8	81	SD3
7	CHGO	32	VCCIO	57	GND	82	SD2
8	LPVSS	33	DATA7	58	SA7	83	SD1
9	BYPASS	34	DATA6	59	SA6	84	SD0
10	TP	35	DATA5	60	SA5	85	GND
11	TSTEN	36	DATA4	61	SA4	86	FR
12	CLOCK	37	DATA3	62	SA3	87	FM
13	RESET	38	DATA2	63	SA2	88	LP
14	CS	39	DATA1	64	SA1	89	XCLK
15	RD	40	DATA0	65	SA0	90	OFF
16	WR	41	GND	66	VCCIO	91	VCCIO
17	ADD3	42	CE	67	SD15	92	XD7
18	ADD2	43	OE	68	SD14	93	XD6
19	ADD1	44	WE	69	SD13	94	XD5
20	ADD0	45	SA17	70	SD12	95	XD4
21	VCCIO	46	SA16	71	SD11	96	XD3
22	DATA15	47	SA15	72	SD10	97	XD2
23	DATA14	48	SA14	73	SD9	98	XD1
24	DATA13	49	SA13	74	SD8	99	XD0
25	GND	50	GND	75	GND	100	GND

■ FUNCTIONAL DESCRIPTION

HVL3224QE receives the image pixel data from the interface (like a camera or Microprocessor) and saves it in SRAM. After that HVL3224QE brings the pixel data in order and makes it go through the unique data conversion algorithm and changes it to the proper color data through the RGB table, and then it is transmitted to color STN LCD with an address.

◆ Read Operation

▶ Read Waveform

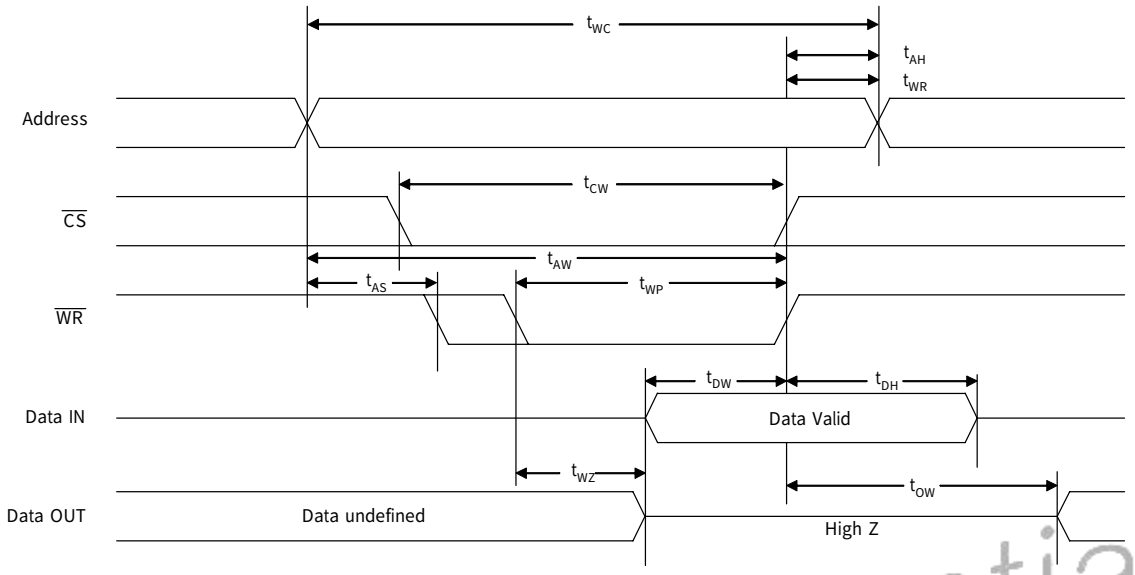


▶ Read Cycle

Parameter	Symbol	Min	Max	Unit
Read cycle time	t_{RC}	10	-	ns
Address access time	t_{AA}	-	10	ns
Chip select ($\overline{CS}$) access time	t_{ACE}	-	10	ns
Output enable ($\overline{RD}$) access time	t_{OE}	-	5	ns
Output hold from address change	t_{OH}	3	-	ns
$\overline{CS}$ Low to output in low Z	t_{CLZ}	0	-	ns
$\overline{CS}$ High to output in high Z	t_{CHZ}	-	5	ns
$\overline{RD}$ Low to output in low Z	t_{RLZ}	0	-	ns
$\overline{RD}$ High to output in high Z	t_{RHZ}	-	5	ns

◆ Write Operation

▶ Write Waveform

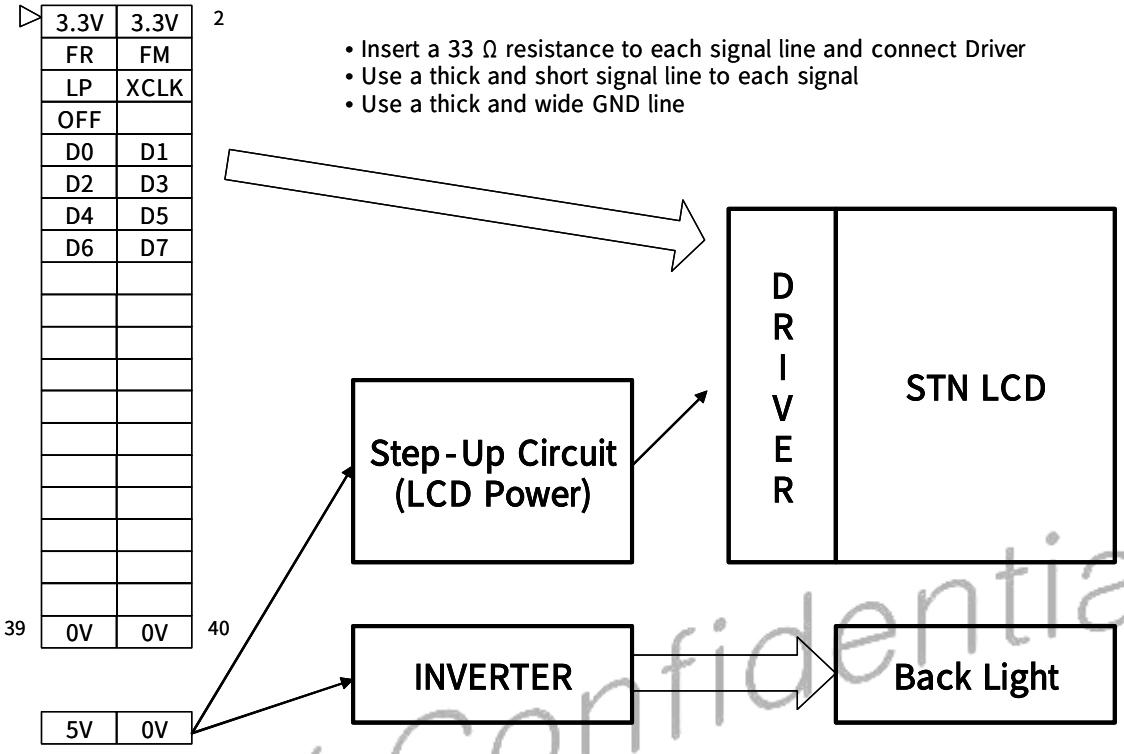


▶ Write Cycle

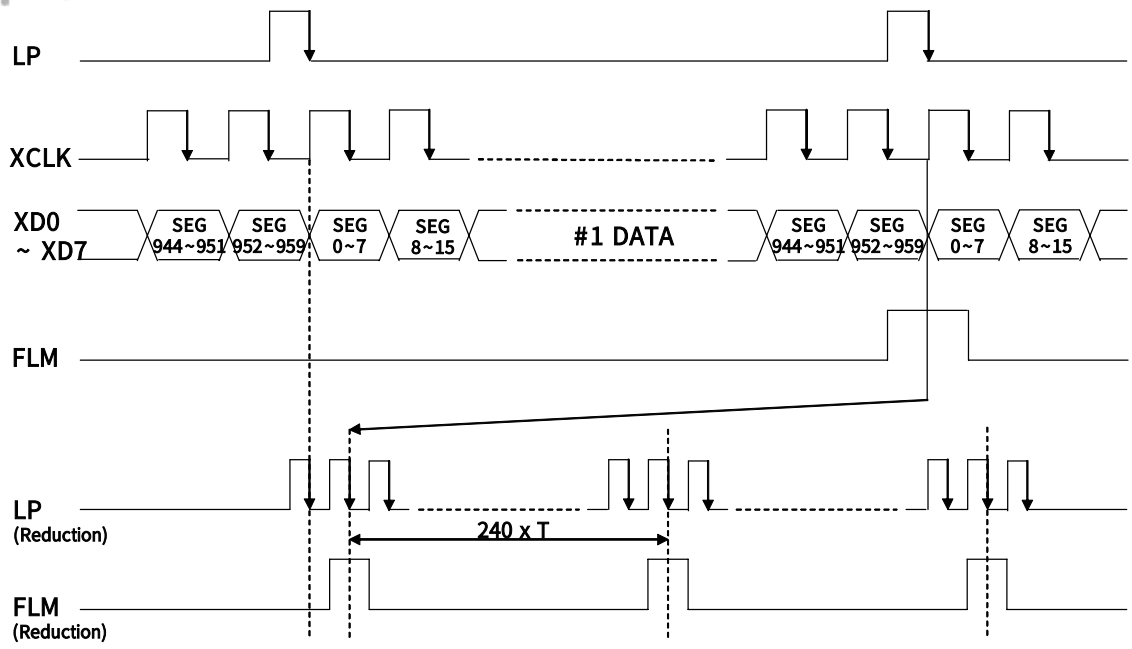
Parameter	Symbol	Min	Max	Unit
Write cycle time	t_{WC}	10	-	ns
Chip enable ($\overline{CS}$) to write end	t_{CW}	5	0	ns
Address setup to write end	t_{AW}	5	-	ns
Address setup time	t_{AS}	0	-	ns
Write pulse width ($\overline{RD}$=high)	t_{WP1}	5	-	ns
Write recovery time	t_{WR}	0	-	ns
Address hold from end of write	t_{AH}	0	-	ns
Data valid to write end	t_{DW}	5	-	ns
Data hold time	t_{DH}	0	-	ns
Write enable to output in High-Z	t_{WZ}	0	5	ns
Output active from write end	t_{OW}	5	-	ns

◆ LCD Interface Example

HIROSE HIF3F-40PA



◆ LCD Interface Timing Chart



■ CONTROL REGISTER DESCRIPTION

Addr	bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
0x00																MG
0x01									Rst							Inv
0x02	LPI 9	LPI 8	LPI 7	LPI 6	LPI 5	LPI 4	LPI 3	LPI 2	LPI 1	LPI 0	LPW 5	LPW 4	LPW 3	LPW 2	LPW 1	LPW 0
0x03	FMI 9	FMI 8	FMI 7	FMI 6	FMI 5	FMI 4	FMI 3	FMI 2	FMI 1	FMI 0	FMW 5	FMW 4	FMW 3	FMW 2	FMW 1	FMW 0
0x04									M7	M6	M5	M4	M3	M2	M1	M0
0x05																
0x06								XL8	XL7	XL6	XL5	XL4	XL3	XL2	XL1	XL0
0x07								YL8	YL7	YL6	YL5	YL4	YL3	YL2	YL1	YL0
0x08								X8	X7	X6	X5	X4	X3	X2	X1	X0
0x09								Y8	Y7	Y6	Y5	Y4	Y3	Y2	Y1	Y0
0x0A	R4	R3	R2	R1	R0	G5	G4	G3	G2	G1	G0	B4	B3	B2	B1	B0
0x0B																
0x0C																
0x0D																
0x0E																
0x0F																

Table 2-1 LCD Decoder Registers

- MG : M generator function enable
- Rst : Software Reset
- Inv : Set by 1, The color is turned over
  Set by 0, The color won't be changed
- Doff : Screen off
- M7~M0 : M Configuration
- XL8~XL0 : Point out the color LCD horizontal resolution
- YL8~YL0 : Point out the color LCD vertical resolution
- X0~8 : Column Data address of the main frame memory
- Y0~8 : Row Data address of the main frame memory (default)
- R4~R0, G5~G0, B4~B0 : RGB display data (5:6:5)bit

■ ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Limits	Unit
Power Supply Voltage	V_{DD}	-0.3 to 4.0	V
Input Voltage	V_I	-0.3 to VDD + 0.5[*1]	V
Output Voltage	V_O	-0.3 to VDD + 0.5[*1]	V
Output Current/Pin	I_{OUT}	±30	mA
Storage Temperature	T_{STG}	-65 to 150	˚C

*1: Possibles to use from -0.3V to 7.0V of N channel open drain bi-directional buffers, input buffer in the IDC and IDH systems and Fail Safe cells.

■ RECOMMENDED OPERATING CONDITIONS

Item	Symbol	Min.	Typ.	Max.	Unit
Power Supply Voltage	V_{DD}	3.00	3.30	3.60	V
Input Voltage	V_I	V_{SS}	—	V_{DD}[*1]	V
Ambient Temperature	Ta	0 -40	25 25	70[*2] 85[*3]	˚C
Normal Input Rising Time	t_{ri}	—	—	50	ns
Normal Input Falling Time	t_{fa}	—	—	50	ns
Schmitt Input Rising Time	t_{ri}	—	—	5	ms
Schmitt Input Falling Time	t_{fa}	—	—	5	ms

*1: Possible to use 5.25 or 5.50V of N channel open drain bi-directional buffers, input buffer in the IDC and IDH systems and Fail Safe cells.
*2: The ambient temperature range is recommended for Tj = 0 to 80˚C
*3: The ambient temperature range is recommented for Tj = -40 to 125˚C

■ ELECTRICAL CHARACTERISTICS

(VDD = 3.3V ± 0.3V, VSS = 0V, Ta = -40 to 85˚C)

Item	Symbol	Conditions		Min.	Typ.	Max.	Unit
Quiescent Current*1	I_{DDS}	Quiescent Conditions		—	—	170	μ
Input Leakage Current	I_{LI}	—		-1	—	1	μ
Off State Leakage Current	I_{OZ}	—		-1	—	1	μ
High Level Output Voltage	V_{OH}	I_{OH}=-0.1mA(Type S), -1mA(Type M) -2mA(Type 1), -6mA(Type 2) -12mA(Type 3) V_{DD}=Min.		V_{DD} -0.4	—	—	V
Low Level Output Voltage	V_{OL}	I_{OL}=0.1mA(Type S), 1mA(Type M) 2mA(Type 1), 6mA(Type 2) 12mA(Type 3) V_{DD}=Min.		—	—	0.4	V
High Level Input Voltage	V_{IH1}	LVTTL Level, V_{DD}=Max.		2.0	—	—	V
Low Level Input Voltage	V_{IL1}	LVTTL Level, V_{DD}=Min.		—	—	0.8	V
Positive Trigger Voltage	V_{T1+}	LVTTL Schmitt		1.1	—	2.4	V
Negative Trigger Voltage	V_{T1-}	LVTTL Schmitt		0.6	—	1.8	V
Hysteresis Voltage	V_{H1}	LVTTL Schmitt		0.1	—	—	V
High Level Input Voltage*3	V_{IH3}	PCI Level, V_{DD}=Max.		1.8	—	—	V
Low Level Input Voltage*3	V_{IL3}	PCI Level, V_{DD}=Min.		—	—	0.9	V
High Level Output Current*3	I_{OH3}	PCI Response V_{OH}=0.90V, V_{DD}=Min. V_{OL}=2.52V, V_{DD}=Max.		-36 —	— —	— -115	mA mA
Low Level Output Current*3	I_{OL3}	PCI Response V_{OH}=1.80V, V_{DD}=Min. V_{OL}=0.65V, V_{DD}=Max.		48 —	— —	— 137	mA mA
Pull Up Resistor*2	R_{PU}	V_I = 0V	Type 1	20	50	(100) 120	kΩ
			Type 2	40	100	(200) 240	
Pull Down Resistor*2	R_{PD}	V_I = V_{DD}	Type 1	20	50	(100) 120	kΩ
			Type 2	40	100	(200) 240	
High Level Maintenance Current	I_{BHH}	Bus Hold Response, V_{IN}=2.0V V_{DD}=Min.		—	—	-20	μ
Low Level Maintenance Current	I_{BHL}	Bus Hold Response, V_{IN}=0.8V V_{DD}=Min.		—	—	17	μ
High Level Reversal Current	I_{BHHO}	Bus Hold Response, V_{IN}=0.8V V_{DD}=Max.		-350	—	—	μ
Low Level Reversal Current	I_{BHLO}	Bus Hold Response, V_{IN}=2.0V V_{DD}=Max.		210	—	—	μ
Input Terminal Capacitance	C_I	f =1MHz, V_{DD}=0V		—	—	10	pF
Output Terminal Capacitance	C_O	f =1MHz, V_{DD}=0V		—	—	10	pF
Input/Output Terminal Capacitance	C_{IO}	f =1MHz, V_{DD}=0V		—	—	10	pF

*1: The quiescent current is a typical value (Tj=85˚C) for each master. For details, please see Tables 1-9 and 1-10.

*2: The values parenthesized means in case of Ta=0 to 70˚C. Values are doubled for V_{DD}=3.3V±-0.3V, V_{SS}=0V, and Ta=-40˚C to 85˚C.

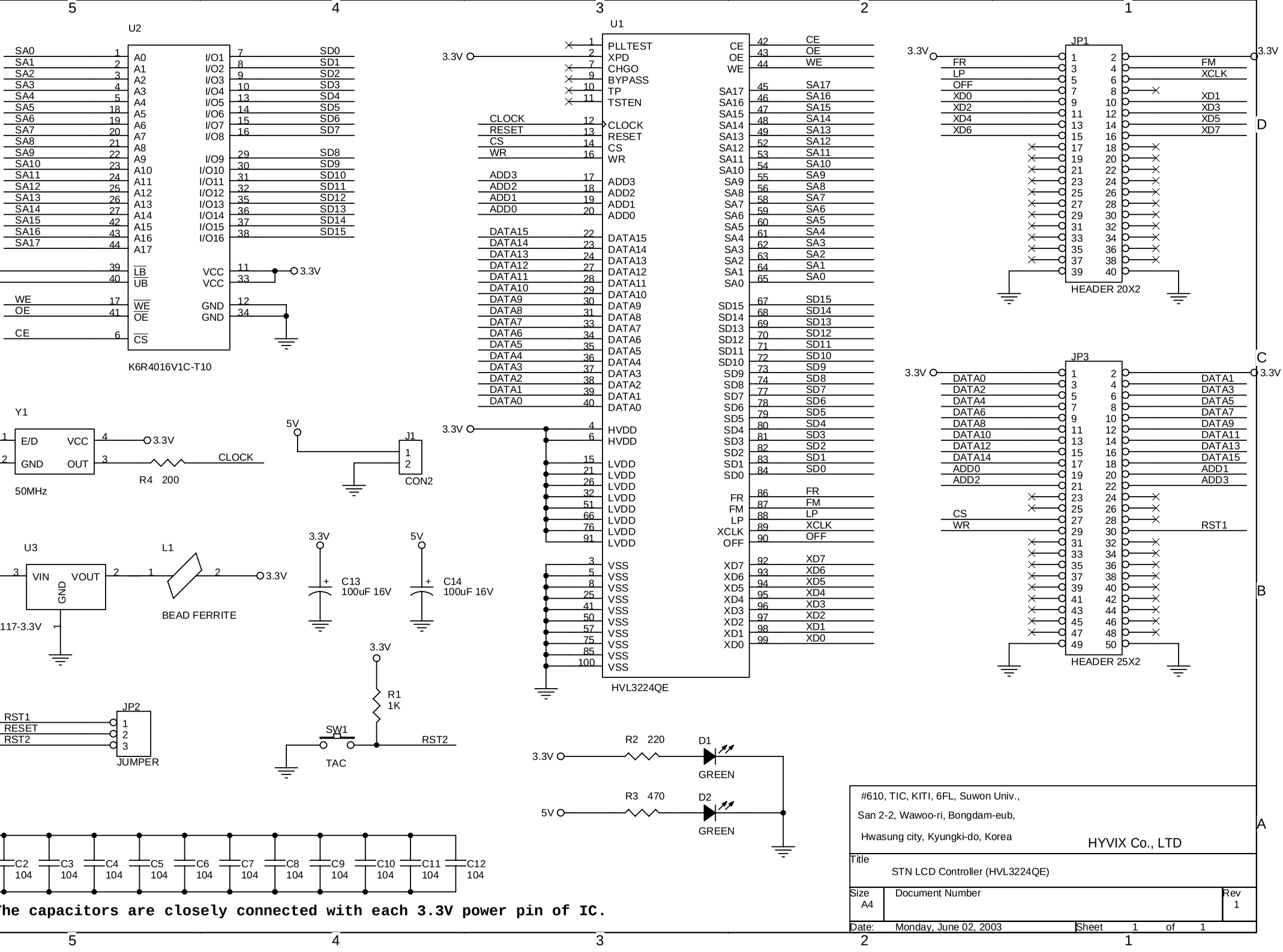
*3: Complies with Rev. 2.2 of PCI standard.

■ TYPICAL APPLICATION

▶ PART LIST

No.	Qty	Reference	Part	Mfg
1	12	C1, C2, C3, C4, C5, C6, C7, C8, C9, C10, C11, C12	104	
2	2	C13, C14	100uF 16V	
3	2	D1,D2	GREEN (LED)	
4	1	JP1	HEADER 20X2	
5	1	JP2	JUMPER 3X1	
6	1	JP3	HEADER 25X2	
7	1	J1	CON2	
8	1	L1	BEAD FERRITE	
9	1	R1	1K	
10	1	R2	220	
11	1	R3	470	
12	1	R4	200	
13	1	SW1	TAC	
14	1	U1	HVL3224QE	HYVIX
15	1	U2	K6R4016V1C-T10	SAMSUNG
16	1	U3	EZ1117-3.3V	SEMTECK
17	1	Y1	50MHz	

▶ SCHEMATIC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K6R4016V1C-T10
U1
HVL3224QE
JP1
HEADER 20X2
JP3
HEADER 25X2
Y1
50MHz
R4 200
J1
CON2
U3
117-3.3V
L1
BEAD FERRITE
C13 100uF 16V
C14 100uF 16V
JP2
JUMPER
R1 1K
SW1
TAC
R2 220
D1
GREEN
R3 470
D2
GREEN
C2 104
C3 104
C4 104
C5 104
C6 104
C7 104
C8 104
C9 104
C10 104
C11 104
C12 104
The capacitors are closely connected with each 3.3V power pin of IC.
#610, TIC, KITI, 6FL, Suwon Univ.,
San 2-2, Wawoo-ri, Bongdam-eub,
Hwasung city, Kyungki-do, Korea
HYVIX Co., LTD
Title
STN LCD Controller (HVL3224QE)
Size A4
Document Number
Rev 1
Date: Monday, June 02, 2003
Sheet 1 of 1