HYUNDAI 8Mx8 bit Synchronous DRAM Series

HY57V648010/ HY57V648020/ HY57V658010/ HY57V658020
HY57V648011/ HY57V648021/ HY57V658011/ HY57V658021

PRELIMINARY

DESCRIPTION

HY57V648010	4Mbit x 2bank x 8 I/O, LVTTL
HY57V648020	2Mbit x 4bank x 8 I/O, LVTTL
HY57V658010	4Mbit x 2bank x 8 I/O, LVTTL
HY57V658020	2Mbit x 4bank x 8 I/O, LVTTL
HY57V648011	4Mbit x 2bank x 8 I/O, SSTL
HY57V648021	2Mbit x 4bank x 8 I/O, SSTL
HY57V658011	4Mbit x 2bank x 8 I/O, SSTL
HY57V658021	2Mbit x 4bank x 8 I/O, SSTL

The HY57V648010, HY57V648020, HY57V658010, HY57V658020, HY57V648011, HY57V648021, HY57V658011, HY57V658021 are high speed 3.3V Synchronous DRAM`s and fabricated with the Hyundai CMOS process. Each bank shares the same chip inputs and outputs but can be independently operated. The Synchronous devices are compatible with the JEDEC functional description and pinout, offering fully synchronous operation. All address, data and control inputs are latched on the rising edge of the master clock input. The data paths are internally pipelined to achieve very high bandwidth.

Programmable options include the length of pipeline(Read latency of 1,2, or 3), the number of consecutive read or write cycles initiated by a single control command(Burst length of 1,2,4,8, or full page), and the burst count sequence(sequential or interleave). A burst of read or write cycles in progress can be terminated by a burst terminate command or can be interrupted and replaced by a new burst read or write command on any cycle.(This pipelined design is not restricted by a `2N` rule.)

The Synchronous DRAM also allows both auto refresh and self refresh. All input and output voltage levels are compatible with LVTTL or High speed I/O interface(SSTL).

FEATURES

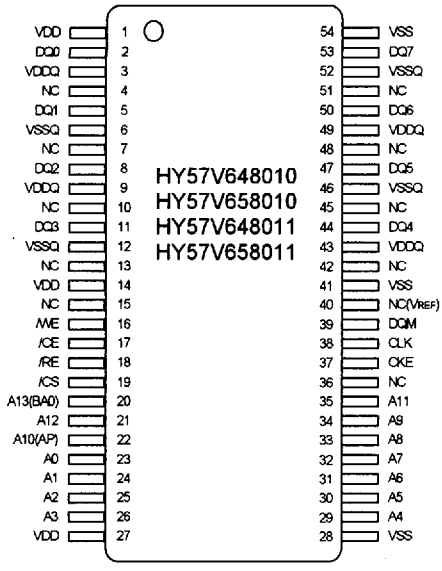
- Fully synchronous ; all inputs referenced to positive edge of system clock
- Internal 2 or 4 banks with single pulsed $\overline{RAS}$
- Auto Precharge/Precharge all banks by A10 flag
- Single 3.3V±0.3V power supply
- All device pins are compatible with LVTTL or High speed I/O interface(SSTL)
- 400mil 54pin TSOP(II) with 0.8mm of lead pitch (Lead-On-Chip)
- 4096 refresh cycles every 64ms or 8192 refresh cycles every 128ms
- Possible to assert random column address every clock cycle
- Programmable Burst lengths and Sequences
  - 1,2,4,8,full page for Sequential type
  - 1,2,4,8 for Interleave type
- Programmable $\overline{CAS}$ latency ; 1,2,3 clocks
- Support clock suspend/Power down mode by CKE
- Data mask function by DQM
- Mode register set programming
- Burst termination command
- Meet all the other JEDEC specifications
- Self refresh provides minimum power, full internal refresh control
- Interleaved Auto refresh mode

ORDERING INFORMATION

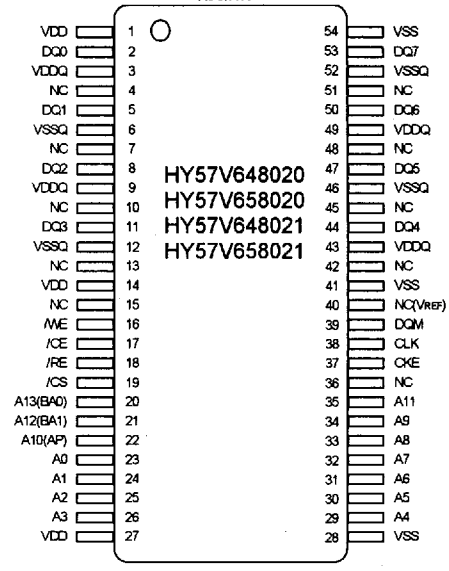
Part NO.	Max. Frequency	Package	Remark
HY57V648010TC - 10/12/15	100/83/66 MHz	400mil TSOP-II	x8, 2bank, 8K ref., LVTTL
HY57V648020TC - 10/12/15	100/83/66 MHz	400mil TSOP-II	x8, 4bank, 8K ref., LVTTL
HY57V658010TC - 10/12/15	100/83/66 MHz	400mil TSOP-II	x8, 2bank, 4K ref., LVTTL
HY57V658020TC - 10/12/15	100/83/66 MHz	400mil TSOP-II	x8, 4bank, 4K ref., LVTTL
HY57V648011TC - 7/8/10	150/125/100 MHz	400mil TSOP-II	x8, 2bank, 8K ref., SSTL
HY57V648021TC - 7/8/10	150/125/100 MHz	400mil TSOP-II	x8, 4bank, 8K ref., SSTL
HY57V658011TC - 7/8/10	150/125/100 MHz	400mil TSOP-II	x8, 2bank, 4K ref., SSTL
HY57V658021TC - 7/8/10	150/125/100 MHz	400mil TSOP-II	x8, 4bank, 4K ref., SSTL

PIN CONNECTION

2bank



4bank

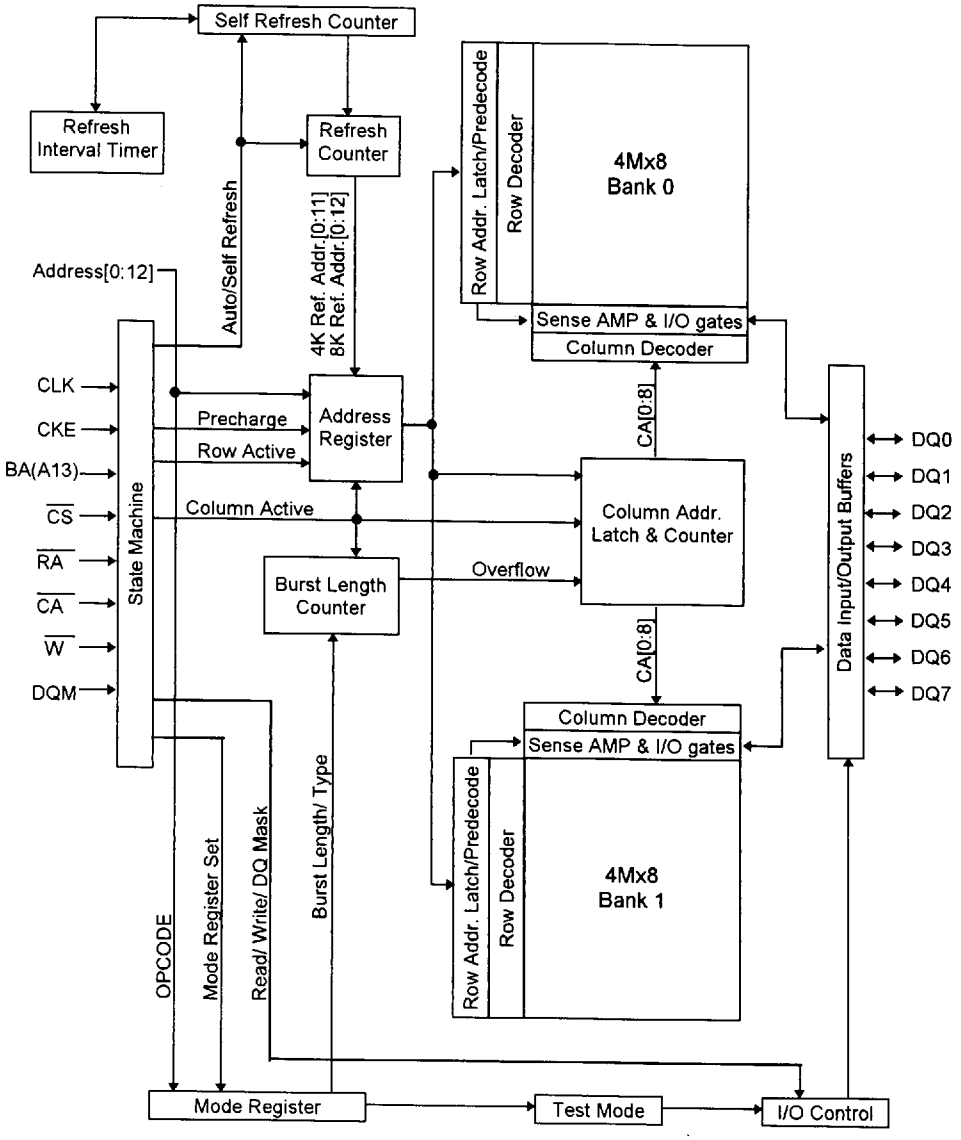


PIN DESCRIPTION

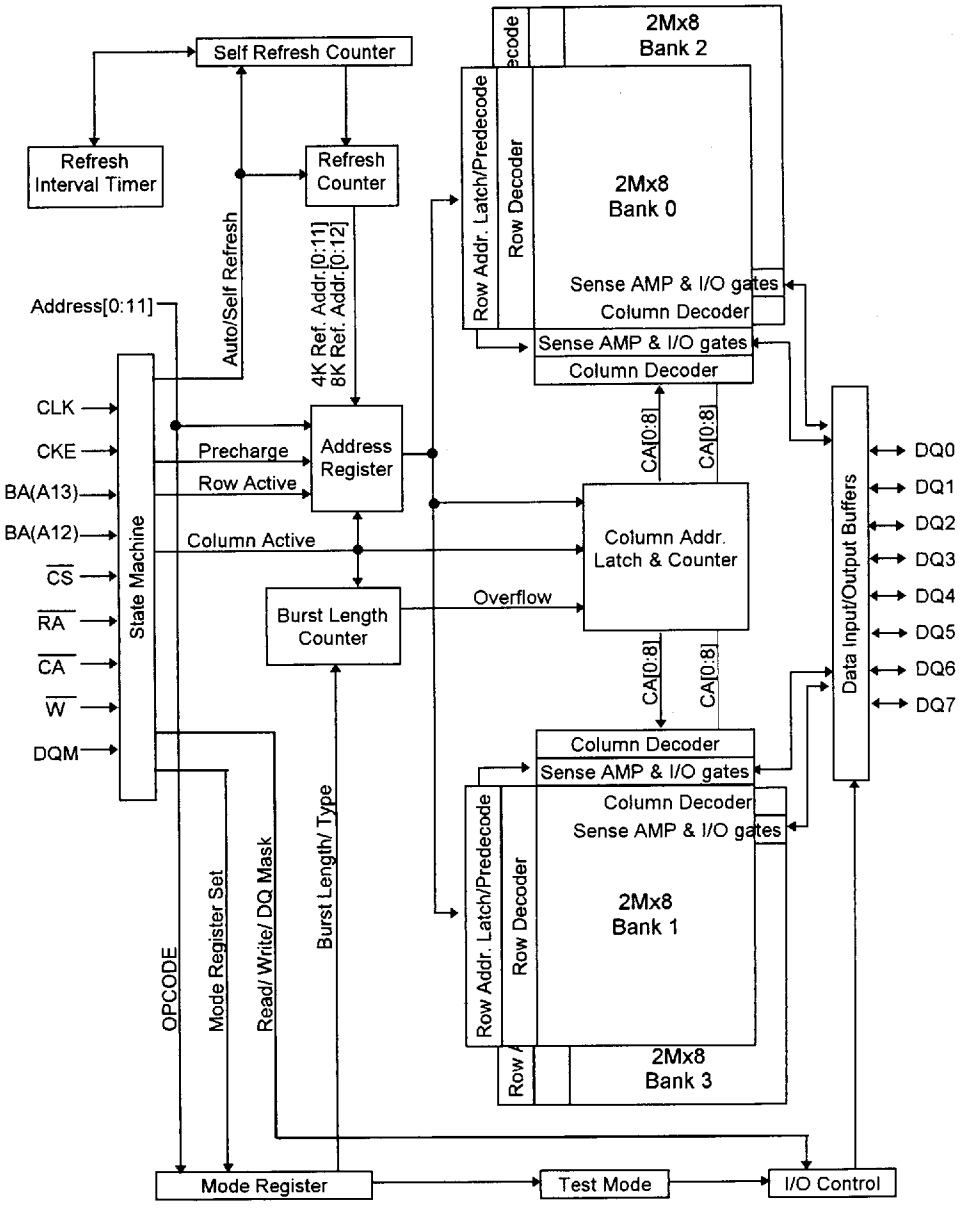
Pin Numbers	Pin Name	Type	Description
38	CLK	Input	System Clock Input; All other inputs except CKE are registered to the SDRAM on the rising edge of CLK.
37	CKE	Input	Clock Enable; Controls internal clock signal and when deactivated, the SDRAM will be one of the states among power down, suspend, or self refresh.
2bank: 20 4bank: 20,21	A13 A13, A12	Input	Bank select address(BA) ; Select either one of dual banks during both $\overline{RAS}$ and $\overline{CAS}$ activity.
2bank: 21-26, 29-35 4bank: 22-26, 29-35	A0-A12 A0-A11	Input	Address Inputs; Row&Column address : A0-A8 Row address only : 2bank[A9-A12], 4bank[A9-A11] Precharge flag : A10 Opcode for mode register set : A0-A13
19	$\overline{CS}$	Input	Chip Select; Functions command mask(NOP).
18	$\overline{RAS}$	1nput	Row Enable; See functional truth table for details.
17	$\overline{CAS}$	Input	Column Enable; See functional truth table for details.
16	$\overline{W}$	Input	Write Enable; See functional truth table for details.
39	DQM	Input	Data Input / Output Mask
2,5,8,11, 44,47,50,53	DQ0-DQ7	Input / Output	Data Input / Output; Include inputs, outputs, or Hi-Z state.
3,9,43,49 6,12,46,52	VDDQ VSSQ	Supply for DQ	DQ Power Supplies
1,27	VDD	Supply	Power Supplies; 3.3V±0.3V
28,54	VSS	Supply	Ground

FUNCTIONAL BLOCK DIAGRAM

4Mbit x 2bank x 8 I/O Synchronous DRAM



2Mbit x 4bank x 8 I/O Synchronous DRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Rating	Unit
T_A	Ambient Temperature	0 to 70	℃
T_{STG}	Storage Temperature	-55 to 125	℃
V_{IN}, V_{OUT}	Voltage on Any Pin relative to Vss	-1.0 to 4.6	V
V_{DD}	Voltage on V_{DD} relative to Vss	-1.0 to 4.6	V
I_{OS}	Short Circuit Output Current	50	mA
P_D	Power Dissipation	1	W
T_{SOLDER}	Soldering Temperature · Time	260 · 10	℃ · sec

Note : Operation at above Absolute Maximum Ratings can adversely affect device reliability.

RECOMMENDED DC OPERATING CONDITIONS*

(T_A=0℃ to 70℃)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Note
V_{DD}, V_{DDQ}	Power Supply Voltage	3.0	3.3	3.6	V	
Vss, V_{SSQ}	Power Supply Voltage	0	0	0	V	
V_{IH}	Input High Voltage	2.0	-	V_{DD} + 0.4	V	LVTTL
		V_{REF} + 0.2	-	V_{DD} + 0.3	V	SSTL
V_{IL}	Input Low Voltage	-0.3	-	0.8	V	LVTTL
		-0.3	-	V_{REF} - 0.2	V	SSTL
V_{REF}	Reference Voltage	-	V_{DDQ} x 0.45	-	V	SSTL
R_T	Termination Resistor	-	50	-	Ω	SSTL
Rs	Series Resistor	-	20	-	Ω	SSTL

RECOMMENDED AC OPERATING CONDITIONS*

(T_A=0℃ to 70℃, V_{DD}=3.3V±10%, V_{SS}=0V)

Symbol	Parameter	Value	Unit	Note
V_{IH} / V_{IL}	AC Input High/Low Level Voltage	2.4/0.4	V	LVTTL
		V_{REF}+0.3/V_{REF}-0.3		SSTL
Vtrip	Input Timing Measurement Reference Level Voltage	1.4	V	LVTTL
		V_{REF}		SSTL
tr / tf	Input Rise/Fall Time	1	ns	
Voutref	Output Reference Voltage	1.4	V	LVTTL
		V_{REF}		SSTL
C_L	Output Load Capacitance for Access Time Measurement	Note	pF	

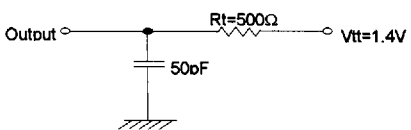
Note : Output load to measure access times is equivalent to two TTL gates and one capacitance(50pF).

CAPACITANCE

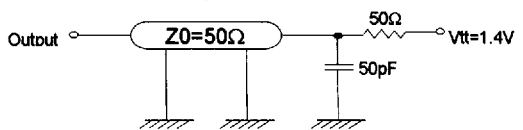
(T_A=25℃, f=1MHz)

Symbol	Parameter	Pin	Max.	Unit
C_{I1}	Input Capacitance	A0-A13	5	pF
C_{I2}	Input Capacitance	CLK, CKE, $\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, DQM	5	pF
C_O	Data Input/Output Capacitance	DQ0-DQ7	7	pF

Note: * DC Output Load Circuit



AC Output Load Circuit



DC CHARACTERISTICS(I)

(T_A=0℃ to 70℃, V_{DD}=3.3V±10%, V_{SS}=0V)

Symbol	Parameter	Test Condition	Min.	Max.	Unit	Note
I_{LI}	Input Leakage Current	V_I=0 to 3.6V, All other pins not undertest=0V	-1	1	μA	
I_{LO}	Output Leakage Current	D_{OUT} is disabled, V_O=0 to 3.6V	-1	1	μA	
I_{REF}	V_{REF} Current	-	-1	1	μA	
V_{OL}	Output Low Voltage	I_O=2.0mA	-	0.4	V	LVTTL
		I_O=16mA	-	V_{TT}-0.4	V	SSTL
V_{OH}	Output High Voltage	I_O=-2.0mA	2.4	-	V	LVTTL
		I_O=-16mA	V_{TT}+0.4	-	V	SSTL

DC CHARACTERISTICS(II)

(T_A=0℃ to 70℃, V_{DD}=3.3V±10%, V_{SS}=0V)

Symbol	Parameter	Test Condition		Max.	Unit	Note
I_{DD1}	Operating current	Burst Length=1, One bank active, $t_{RAS} \geq t_{RAS}$(min), $t_{RP} \geq t_{RP}$(min), I_O=0mA	7ns	100	mA	Note 2
			8ns	85		
			10ns	85		
			12ns	70		
			15ns	60		
I_{DD2P}	Precharge Standby Current in Power Down Mode	CKE≤V_{IL}(max)		2	mA	
I_{DD2N}	Precharge Standby Current in Non Power Down Mode	CKE≥V_{IH}(min), All other pins≥V_{DD}-0.2V or ≤0.2V		12	mA	LVTTL[1]
		CKE=V_{REF}+0.2V, All other pins≥V_{REF}+0.2V or ≤V_{REF}-0.2V		12	mA	SSTL
I_{DD3P}	Active Standby Current in Power Down Mode	CKE≤V_{IL}(max), All bank active		3	mA	
I_{DD3N}	Active Standby Current in Non Power Down Mode	CKE≥V_{IH}(min), All other pins≥V_{DD}-0.2V or ≤0.2V, All bank active		35	mA	LVTTL[1]
		CKE=V_{REF}+0.2V, All other pins≥V_{REF}+0.2V or ≤V_{REF}-0.2V, All bank active		35	mA	SSTL
I_{DD4}	Operating Current (Burst Mode)	$t_{CLK} \geq t_{CLK}$(min), $t_{RAS} \geq t_{RAS}$(min), I_O=0mA, $\overline{CAS}$ Latency=3	7ns	200	mA	Note 2
			8ns	180		
			10ns	150		
			12ns	120		
			15ns	100		
I_{DD5}	Refresh Current	$t_{RC} \geq t_{RC}$(min), Two bank active (8K/128ms)	7ns	125	mA	Note 2
			8ns	110		
			10ns	110		
			12ns	90		
			15ns	75		
		$t_{RC} \geq t_{RC}$(min), Four bank active (4K/64ms)	7ns	180	mA	Note 2
			8ns	160		
			10ns	160		
			12ns	130		
			15ns	105		
I_{DD6}	Self Refresh Current	CKE≤0.2V		2	mA	
				500	μA	L-part

Note :

1. It depends on the number of each pin`s transition. It is assumed there is no transition to measure this current.
2. I_{DD1} depends on output loading and cycle rates. Specified values are obtained with the output open. In addition this I_{DD1} is measured on condition that addresses are changed only one time during t_{CLK}(Min.)

AC CHARACTERISTICS

Synchronous Characteristics(I)

Parameter	150MHz (7ns)			125MHz (8ns)			100MHz (10ns)			83MHz (12ns)			66MHz (15ns)			Unit
$\overline{CAS}$ Latency	3	2	1	3	2	1	3	2	1	3	2	1	3	2	1	Latency
Frequency	150	83	33	125	83	33	100	83	33	83	66	33	-	66	33	MHz
Clock Cycle Time	7	12	30	8	12	30	10	12	30	12	15	30	-	15	30	ns
tRCD	3	2	1	3	2	1	3	2	1	3	2	1	-	2	1	CLK(s)
tRAS	6	4	2	6	4	2	5	4	2	4	4	2	-	4	2	CLK(s)
tRP	4	3	1	3	3	1	3	3	1	3	2	1	-	2	1	CLK(s)
tRC	10	7	3	10	7	3	8	7	3	7	6	3	-	6	3	CLK(s)
tRRD	3	2	1	3	2	1	3	2	1	2	2	2	-	2	2	CLK(s)
tDPL	1	1	1	1	1	1	1	1	1	1	1	1	-	1	1	CLK(s)
tDAL	5	3	2	4	3	2	4	3	2	3	3	2	-	3	2	CLK(s)
tSRE	1	1	1	1	1	1	1	1	1	1	1	1	-	1	1	CLK(s)
tT	1			1			1			1			1			ns
Refresh Cycle	8K/128ms, 4K/64ms															Cycles
Asynchronous Characteristic	50ns Part															ns

Note : tRRD -Bank Active to Active Command
tDPL -DIN to Precharge Command
tDAL -DIN to Active(Ref.) Command (After Write with Autoprecharge)
tSRE -Self Refresh Exit Time

Synchronous Characteristics(II)

[LVTTL Part]

Symbol	Parameter		-10		-12		-15		Unit	Note
			Min.	Max.	Min.	Max.	Min.	Max.		
tAC	Access Time from CLK	$\overline{CAS}$ Lat.=3	-	8	-	9	-	10	ns	
		$\overline{CAS}$ Lat.=2	-	-	-	-	-	10	ns	
tCH	CLK High Level Width		3.5	-	3.5	-	3.5	-	ns	
tCL	CLK Low Level Width		3.5	-	3.5	-	3.5	-	ns	
tOH	Data-out Hold Time		3	-	3	-	3	-	ns	
tOLZ	Data-out Low-Impedance Time		3	-	3	-	3	-	ns	
tOHZ	Data-out High-Impedance Time		0	8	0	9	0	10	ns	
tDS	Data-in Set-up Time		3	-	3	-	3	-	ns	
tDH	Data-in Hold Time		1	-	1	-	1	-	ns	
tAS	Address Set-up Time		3	-	3	-	3	-	ns	
tAH	Address Hold Time		1	-	1	-	1	-	ns	
tCKS	CKE Set-up Time		3	-	3	-	3	-	ns	
tCKH	CKE Hold Time		1	-	1	-	1	-	ns	
tCS	Command Set-up Time		3	-	3	-	3	-	ns	
tCH	Command Hold Time		1	-	1	-	1	-	ns	
tPDE	Power Down Exit Set-up Time		3	-	3	-	3	-	ns	

[SSTL Part]

Symbol	Parameter	-7		-8		-10		Unit	Note
		Min.	Max.	Min.	Max.	Min.	Max.		
tAC	Access Time from CLK ($\overline{CAS}$ Lat.=3	-	5	-	6	-	8	ns	
	$\overline{CAS}$ Lat.=2	-	-	-	-	-	-	ns	
tCH	CLK High Level Width	2.5	-	3	-	3.5	-	ns	
tCL	CLK Low Level Width	2.5	-	3	-	3.5	-	ns	
tOH	Data-out Hold Time	2	-	2	-	3	-	ns	
tOLZ	Data-out Low-Impedance Time	2	-	2	-	3	-	ns	
tOHZ	Data-out High-Impedance Time	0	5	0	6	0	8	ns	
tDS	Data-in Set-up Time	2	-	2	-	3	-	ns	
tDH	Data-in Hold Time	1	-	1	-	1	-	ns	
tAS	Address Set-up Time	2	-	2	-	3	-	ns	
tAH	Address Hold Time	1	-	1	-	1	-	ns	
tCKS	CKE Set-up Time	2	-	2	-	3	-	ns	
tCKH	CKE Hold Time	1	-	1	-	1	-	ns	
tCS	Command Set-up Time	2	-	2	-	3	-	ns	
tCH	Command Hold Time	1	-	1	-	1	-	ns	
tPDE	Power Down Exit Set-up Time	2	-	2	-	3	-	ns	

Latency

Symbol	Parameter		Latency
tCKED	CKE to CLK Suspend / Power Down Mode Entry		1
tDQMOZ	DQM to Data Output in Hi-z		2
tDQMIM	DQM to Data Input Mask		0
tWTL	Write Command to Data Input Valid		0
tPROZ	Precharge Command to Data Output in Hi-z	$\overline{CAS}$ Latency=1	1
		$\overline{CAS}$ Latency=2	2
		$\overline{CAS}$ Latency=3	3
tMRD	Mode Register Set to New Command		1
tCCD	Min. Column Address to Column Address Delay		1
tPPD	Min. Precharge to Precharge Time		1

Notes:
1. All voltage referenced Vss(Ground).
2. An initial pause of 100 μS is required after power-on followed by Power On Sequence & Auto Refresh before proper device operation is achieved.
3. AC measurements assume tT=1ns.
4. Reference level for measuring timing of input signals is 1.40V for LVTTL and VREF for SSTL. Transition times are measured between VIH and VIL.
5. An access time is measured at 1.40V for LVTTL and VREF for SSTL.

STATE AND FUNCTIONAL TRUTH TABLE, OPERATIONS INVOLVING ALL BANKS

Current State	CLK ↑									Action
	CKE		$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	BA	A10	A0-A9 A11/A12[2]	
	Prev.	Curr.								
Power Down	L	L	X	X	X	X	X	X	X	Maintain Power Down
	L	H	L	H	H	H	X	X	X	Exit Power Down → Idle
	L	H	H	X	X	X	X	X	X	Exit Power Down → Idle
Self Refresh[1]	L	L	X	X	X	X	X	X	X	Maintain Self Refresh
	L	H	L	H	H	H	X	X	X	Exit Self Refresh → Idle
	L	H	H	X	X	X	X	X	X	
All Banks Idle	H	L	L	H	H	H	X	X	X	Enter Power Down
	H	L	H	X	X	X	X	X	X	Enter Power Down
	H	L	L	L	L	H	X	X	X	Enter Self Refresh
	H	H	L	H	H	H	X	X	X	NOP
	H	H	H	X	X	X	X	X	X	Deselect
	H	H	L	L	L	L	OPCODE			Mode Register Access
	H	H	L	L	L	H	X	X	X	Auto Refresh
CLK Suspend	L	L	X	X	X	X	X	X	X	Maintain CLK Suspend
	L	H	X	X	X	X	X	X	X	Exit CLK Suspend
Auto Refresh	H	H	L	H	H	H	X	X	X	NOP→All Banks Idle After tRC
	H	H	H	X	X	X	X	X	X	Deselect
Any state other than above	H	L	X	X	X	X	X	X	X	Suspend Clock, next Cycle → Clock Suspend
DQM	H	X	X	X	X	X	X	X	X	Write DQM Latency is 0, Read DQM Latency is 2.

Note: 1. Exiting Self Refresh occurs by asynchronously bringing CKE from low to high.
2. In case of 2bank : A0-A9, A11,A12
In case of 4bank : A0-A9, A11

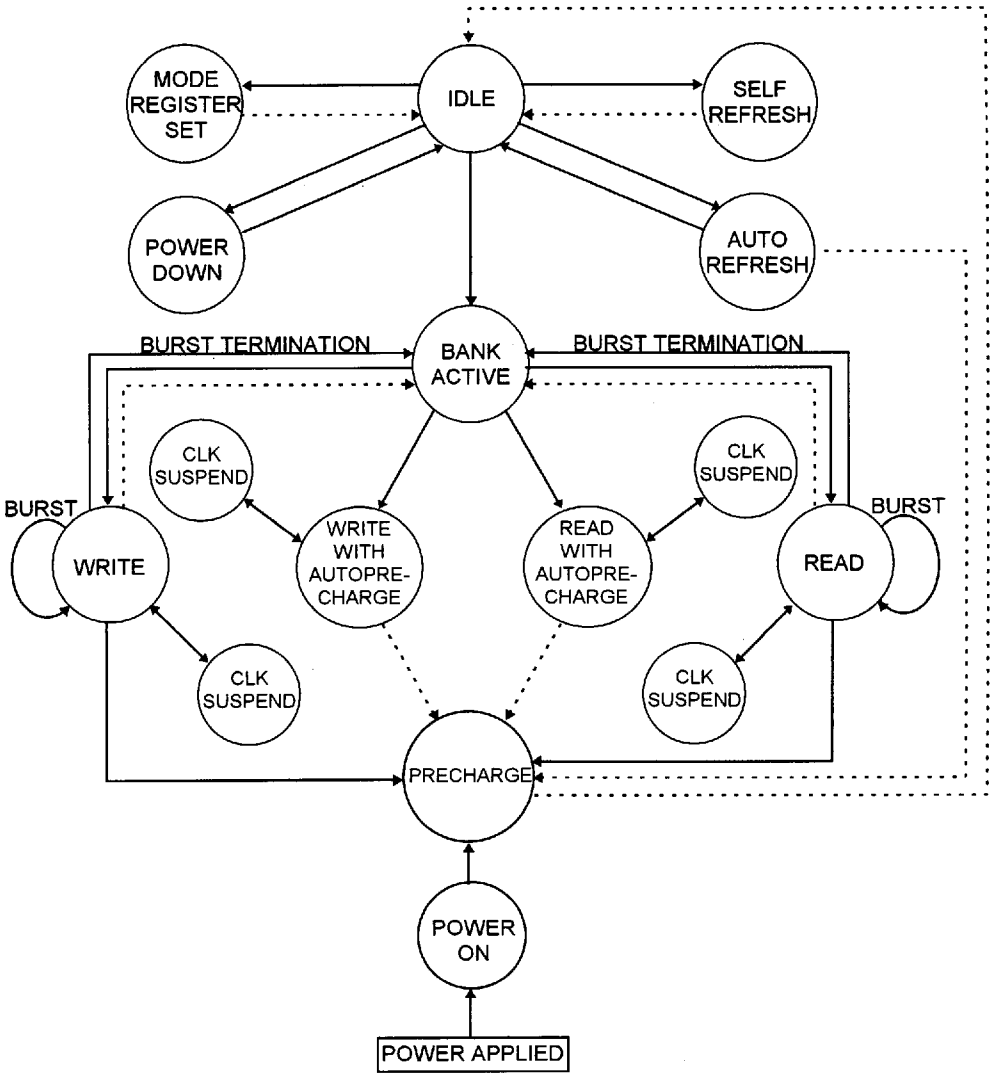
STATE AND FUNCTIONAL TRUTH TABLE, SELECTED BANK[1]

Current State of Selected Bank	CLK ↑							Action to Selected Bank (Unless otherwise noted)
	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	BA	A10	A0-A9, A11/A12[5]	
Idle	L	L	L	L	OPCODE			Mode Register Access
	L	H	H	H	X	X	X	NOP
	H	X	X	X	X	X	X	Deselect
	L	L	H	L	BA	X	X	NOP
	L	L	L	H	X	X	X	Auto or Self Refresh
	L	L	H	H	BA	RA	RA	Activate Row
Row Active	L	L	L	X	X	X	X	ILLEGAL
	L	H	H	H	X	X	X	NOP
	H	X	X	X	X	X	X	Deselect
	L	L	H	L	BA	L	X	Precharge Selected Bank
	L	L	H	L	X	H	X	Precharge All Banks
	L	H	L	L	BA	L	CA	Begin Write
	L	H	L	L	BA	H	CA	Begin Write/Auto Precharge
	L	H	L	H	BA	L	CA	Begin Read
	L	H	L	H	BA	H	CA	Begin Read/Auto Precharge
Read	L	H	H	H	X	X	X	NOP(Continue burst to end → Row Active)
	H	X	X	X	X	X	X	Deselect
	L	L	H	L	BA	L	X	Precharge Selected Bank
	L	L	H	L	X	H	X	Precharge All banks
	L	L	L	X	X	X	X	ILLEGAL
	L	H	L	L	BA	L	CA	Begin Write[2]
	L	H	L	L	BA	H	CA	Begin Write/Auto Precharge[2]
	L	H	L	H	BA	L	CA	Begin New Read
	L	H	L	H	BA	H	CA	Begin New Read/Auto Precharge
	L	H	H	L	X	X	X	Term Burst → Row Active
Write	L	H	H	H	X	X	X	NOP(Continue burst to end → Row Active)
	H	X	X	X	X	X	X	Deselect
	L	L	H	L	BA	L	X	Precharge Selected Bank
	L	L	H	L	X	H	X	Precharge All banks
	L	L	L	X	X	X	X	ILLEGAL
	L	H	L	L	BA	L	CA	Begin New Write
	L	H	L	L	BA	H	CA	Begin New Write/Auto Precharge
	L	H	L	H	BA	L	CA	Begin New Read
	L	H	L	H	BA	H	CA	Begin New Read/Auto Precharge
	L	H	H	L	X	X	X	Term Burst → Row Active
Read with Auto Precharging	L	H	H	H	X	X	X	NOP, Continue burst to end → Precharge[3]
	H	X	X	X	X	X	X	Deselect
	L	L	H	L	BA	L	X	ILLEGAL
	L	L	H	L	X	H	X	ILLEGAL
	L	H	L	L	BA	L	CA	ILLEGAL
	L	H	L	L	BA	H	CA	ILLEGAL
	L	H	L	H	BA	L	CA	ILLEGAL
	L	H	L	H	BA	H	CA	ILLEGAL
	L	H	H	L	X	X	X	ILLEGAL
	L	L	L	X	X	X	X	ILLEGAL

Current State of Selected Bank	CLK↑							Action to Selected Bank (Unless otherwise noted)
	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	BA	A10	A0-A9,A11/A12[5]	
Write with Auto Precharging	L	H	H	H	X	X	X	NOP, Continue burst to end → Precharge[3]
	H	X	X	X	X	X	X	Deselect
	L	L	H	L	BA	L	X	ILLEGAL
	L	L	H	L	X	H	X	ILLEGAL
	L	H	L	L	BA	L	CA	ILLEGAL
	L	H	L	L	BA	H	CA	ILLEGAL
	L	H	L	H	BA	L	CA	ILLEGAL
	L	H	L	H	BA	H	CA	ILLEGAL
	L	H	H	L	X	X	X	ILLEGAL
	L	L	L	X	X	X	X	ILLEGAL
Precharging	L	H	H	H	X	X	X	NOP → Idle after tRP
	H	X	X	X	X	X	X	Deselect
	L	L	H	L	BA	L	X	NOP
	L	L	H	L	X	H	X	NOP
	L	H	L	L	BA	L	CA	ILLEGAL
	L	H	L	L	BA	H	CA	ILLEGAL
	L	H	L	H	BA	L	CA	ILLEGAL
	L	H	L	H	BA	H	CA	ILLEGAL
	L	H	H	L	X	X	X	ILLEGAL
Row Activating	L	H	H	H	X	X	X	NOP→ Row active after tRCD
	H	X	X	X	X	X	X	Deselect
	L	L	H	L	BA	L	X	ILLEGAL
	L	L	H	L	X	H	X	ILLEGAL
	L	H	L	L	BA	X	CA	ILLEGAL
	L	H	L	H	BA	X	CA	ILLEGAL
	L	H	H	L	X	X	X	ILLEGAL
	L	L	L	X	X	X	X	ILLEGAL
Mode Register Accessing	L	H	H	H	X	X	X	NOP
	H	X	X	X	X	X	X	Deselect
	L	L	H	H	X	X	X	ILLEGAL
	L	H	L	H	X	X	X	ILLEGAL
	L	H	L	L	X	X	X	ILLEGAL
	L	H	H	L	X	X	X	ILLEGAL

Notes:
1. Assume CKE high on the previous and current clock cycles.
2. Read burst must terminate one cycle before the start of a write sequence. This can be accomplished in one of two ways.
   First, if the last bit of the burst is output two cycles before the start of the write sequence, the burst will terminate. And the output will tristate, the internal read pipeline will be flushed during the cycle before the write command is issued.
   Second, the burst can be terminated by bringing DQM high and issuing a terminate burst command two cycles before the write command. This will also guarantee that the output will tristate and the read pipeline will be flushed during the cycle before the write command is issued.
3. While either bank is executing a Read or Write burst sequence with Auto Precharge selected, no Read or Write commands are allowed to the opposite bank.
4. X=Don't care, L=Low, H=High, BA=Bank Address, RA= Row Address, CA=Column Address, Opcode=Operand Code, NOP=No Operation
5. In case of 2bank : A0-A9, A11,A12
   In case of 4bank : A0-A9, A11

STATE DIAGRAM(SIMPLIFIED)



Notes: ——→ By command Input
·····→ Automatic sequence after finishing the command

PROGRAMMABLE MODE REGISTER

MODE REGISTER SET(WRITE)

A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
0	0	0	0	0	0	0	$\overline{CAS}$ Latency			BT	Burst Length		

A3	Burst Type
0	Sequential (Wrap round, Binary-up)
1	Interleave (Wrap round)

A6	A5	A4	$\overline{CAS}$ Latency
0	0	0	Reserved
0	0	1	1
0	1	0	2
0	1	1	3
1	0	0	Reserved
1	0	1	Reserved
1	1	0	Reserved
1	1	1	Reserved

A2	A1	A0	Burst Length
0	0	0	1
0	0	1	2
0	1	0	4
0	1	1	8
1	0	0	Reserved
1	0	1	Reserved
1	1	0	Reserved
1	1	1	Full page[1]

Note : 1. Full page burst supports only sequential type.

TEST MODE

A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0	Address
0	0	0	0	1	X	X	X	X	X	X	X	Refresh Counter Test

Note: Test Mode - Used to test the counter of Auto Refresh.
- Exit test mode using `Precharge All bank .

BURTS LENGTH AND SEQUENCE

Burst Length	Initial Address	Burst Type	
	A2 A1 A0	Sequential	Interleave
2	X X 0	0,1	0,1
	X X 1	1,0	1,0
4	X 0 0	0,1,2,3	0,1,2,3
	X 0 1	1,2,3,0	1,0,3,2
	X 1 0	2,3,0,1	2,3,0,1
	X 1 1	3,0,1,2	3,2,1,0
8	0 0 0	0,1,2,3,4,5,6,7	0,1,2,3,4,5,6,7
	0 0 1	1,2,3,4,5,6,7,0	1,0,3,2,5,4,7,6
	0 1 0	2,3,4,5,6,7,0,1	2,3,0,1,6,7,4,5
	0 1 1	3,4,5,6,7,0,1,2	3,2,1,0,7,6,5,4
	1 0 0	4,5,6,7,0,1,2,3	4,5,6,7,0,1,2,3
	1 0 1	5,6,7,0,1,2,3,4	5,4,7,6,1,0,3,2
	1 1 0	6,7,0,1,2,3,4,5	6,7,4,5,2,3,0,1
	1 1 1	7,0,1,2,3,4,5,6	7,6,5,4,3,2,1,0
Full page	Note	0,1,2,3,4,……,m 1,2,3,4,5,……,0 : : m,0,1,2,3,……,m-1	Not supported

Table 1. Address sequence for different burst lengths

Note : 8Mbit x 2bank x 4I/O - Initial address: A9-A0, Page length: 1024, m=1023
4Mbit x 4bank x 4I/O - Initial address: A9-A0, Page length: 1024, m=1023

PACKAGE INFORMATION

400mil 54pin Thin Small Outline Package

Unit : mm(Inch)