Document Title

128K x16 bit 1.8V Super Low Power Full CMOS Slow SRAM

Revision History

Revision No	History	Draft Date	Remark
05	Divide output load into two factors - tCLZ,tOLZ,tBLZ,tCHZ,tOHZ,tBHZ,tWHZ,tOW - Others Add marking information	Dec.10. 2000	Final
06	Change AC Characteristic - tBLZ	Mar. 24. 2002	

DESCRIPTION

The HY62SF16201A is a high speed, low power and 2M bit full CMOS SRAM organized as 131,072 words by 16bit. The HY62SF16201A uses high performance full CMOS process technology and designed for high speed low power circuit technology. It is particularly well suited for used in high density low power system application. This device has a data retention mode that guarantees data to remain valid at a minimum power supply voltage of 1.2V.

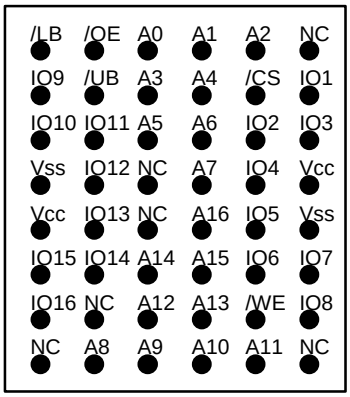
FEATURES

- Fully static operation and Tri-state output
- TTL compatible inputs and outputs
- Battery backup(LL-part)
  -. 1.2V(min) data retention
- Standard pin configuration
  -. 48-FBGA

Product No.	Voltage (V)	Speed (ns)	Operation Current/Icc(mA)	Standby Current(uA)		Temperature (°C)
				LL	SL	
HY62SF16201A	1.7~2.3V	85/100/120	3	3	1	0~70
HY62SF16201A-I	1.7~2.3V	85/100/120	3	3	1	-40~85(I)

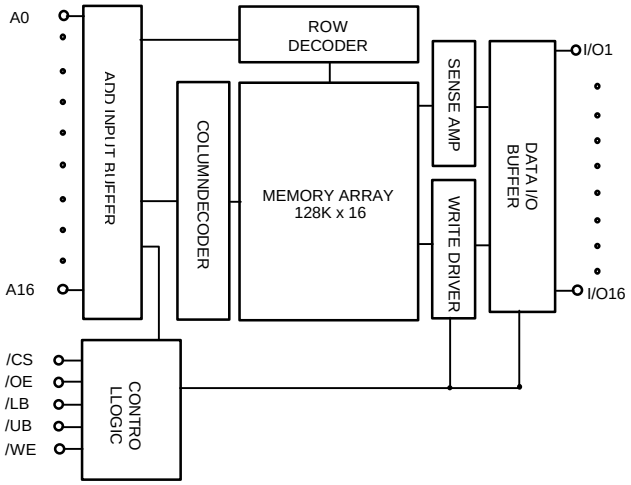
Notes :
1. Blank : Commercial, I : Industrial
2. Current value is max.

PIN CONNECTION



48-FBGA(Top View)

BLOCK DIAGRAM



PIN DESCRIPTION

Pin Name	Pin Function	Pin Name	Pin Function
/CS	Chip Select	I/O1~I/O16	Data Inputs / Outputs
/WE	Write Enable	A0~A16	Address Inputs
/OE	Output Enable	Vcc	Power(1.7V ~ 2.3V)
/LB	Lower Byte Control(I/O1~I/O8)	Vss	Ground
/UB	Upper Byte Control(I/O9~I/O16)	NC	No Connection

ORDERING INFORMATION

Part No.	Speed	Power	Temp.	Package
HY62SF16201ALLF	85/100/120	LL-part		FBGA
HY62SF16201ALLF	85/100/120	SL-part		FBGA
HY62SF16201ALLF-I	85/100/120	LL-part	I	FBGA
HY62SF16201ALLF-I	85/100/120	SL-part	I	FBGA

Note :
1. Blank : Commercial, I : Industrial

ABSOLUTE MAXIMUM RATING (1)

Symbol	Parameter	Rating	Unit	Remark
V_{IN}, V_{OUT}	Input/Output Voltage	-0.2 to 3.6	V	
Vcc	Power Supply	-0.2 to 4.6	V	
T_A	Operating Temperature	0 to 70	°C	HY62SF16201A
		-40 to 85	°C	HY62SF16201A-I
T_{STG}	Storage Temperature	-55 to 150	°C	
P_D	Power Dissipation	1.0	W	
T_{SOLDER}	Ball Soldering Temperature & Time	260 • 10	°C • sec	

Note :
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is stress rating only and the functional operation of the device under these or any other conditions above those indicated in the operation of this specification is not implied. Exposure to the absolute maximum rating conditions for extended period may affect reliability.

TRUTH TABLE

/CS	/WE	/OE	/LB	/UB	Mode	I/O		Power
						I/O1~I/O8	I/O9~I/O16	
H	X	X	X	X	Deselected	High-Z	High-Z	Standby
X	X	X	H	H	Deselected	High-Z	High-Z	Standby
L	H	H	L	X	Output Disabled	High-Z	High-Z	Active
L	H	H	X	L	Output Disabled	High-Z	High-Z	Active
L	H	L	L	H	Read	D_{OUT}	High-Z	Active
			H	L		High-Z	D_{OUT}	
			L	L		D_{OUT}	D_{OUT}	
L	L	X	L	H	Write	D_{IN}	High-Z	Active
			H	L		High-Z	D_{IN}	
			L	L		D_{IN}	D_{IN}	

Note :
1. H=V_{IH}, L=V_{IL}, X=don't care
2. UB, LB(Upper, Lower Byte enable)
   These active LOW inputs allow individual bytes to be written or read.
   When LB is LOW, data is written or read to the lower byte, I/O 1 -I/O 8.
   When UB is LOW, data is written or read to the Upper byte, I/O 9 -I/O 16.

RECOMMENDED DC OPERATING CONDITION

Symbol	Parameter	Min.	Typ.	Max.	Unit
Vcc	Supply Voltage	1.7	1.8	2.3	V
Vss	Ground	0	0	0	V
V_{IH}	Input High Voltage	1.4	-	Vcc+0.3	V
V_{IL}	Input Low Voltage	-0.3(1)	-	0.4	V

Note :
1. VIL = -1.5V for pulse width less than 30ns
2. Typical values is not 100% tested

DC ELECTRICAL CHARACTERISTICS

Vcc = 1.7V~2.3V, T_A = 0°C to 70°C/-40°C to 85°C (I)

Symbol	Parameter	Test Condition		Min.	Typ.	Max.	Unit
I_{LI}	Input Leakage Current	Vss ≤ V_{IN} ≤ Vcc		-1	-	1	uA
I_{LO}	Output Leakage Current	Vss ≤ V_{OUT} ≤ Vcc, /CS = V_{IH} or /OE = V_{IH} or /WE = V_{IL}, /UB = /LB = V_{IH}		-1	-	1	uA
Icc	Operating Power Supply Current	/CS = V_{IL}, V_{IN} = V_{IH} or V_{IL}, $I_{I/O}$ = 0mA		-	-	3	mA
I_{CC1}	Average Operating Current	Cycle Time=Min.100% duty, /CS = V_{IL},V_{IN} = V_{IH} or V_{IL}, $I_{I/O}$ = 0mA,		-	-	20	mA
		Cycle time = 1us, /CS ≤ 0.2V, V_{IN}<0.2V, $I_{I/O}$ = 0mA,				3	mA
I_{SB}	Standby Current (TTL Input)	/CS = V_{IH} or /UB = /LB = V_{IH}, V_{IN} = V_{IH} or V_{IL}		-	-	0.15	mA
I_{SB1}	Standby Current (CMOS Input)	/CS ≥ Vcc - 0.2V or /UB = /LB ≥ Vcc - 0.2V,	SL	-	-	1	uA
		V_{IN} ≥ Vcc - 0.2V or V_{IN} ≤ Vss + 0.2V	LL	-	0.5	3	uA
V_{OL}	Output Low Voltage	I_{OL} = 0.1mA		-	-	0.2	V
V_{OH}	Output High Voltage	I_{OH} = -0.1mA		1.6	-	-	V

Notes :
1. Typical values are at Vcc = 1.8V, T_A = 25°C
2. Typical values are sampled and not 100% tested

CAPACITANCE

(Temp = 25°C, f= 1.0MHz)

Symbol	Parameter	Condition	Max.	Unit
C_{IN}	Input Capacitance(Add, /CS, /WE, /UB, /LB, /OE)	V_{IN} = 0V	8	pF
C_{OUT}	Output Capacitance(I/O)	$V_{I/O}$ = 0V	10	pF

Note :
1. These parameters are sampled and not 100% tested

AC CHARACTERISTICS

Vcc = 1.7V~2.3V, T_A = 0°C to 70°C/ -40°C to 85°C(I), unless otherwise specified

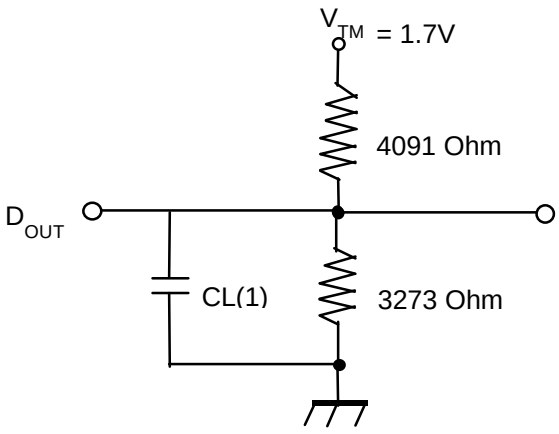
#	Symbol	Parameter	-85		-10		-12		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	
	READ CYCLE								
1	tRC	Read Cycle Time	85	-	100	-	120	-	ns
2	tAA	Address Access Time	-	85	-	100	-	120	ns
3	tACS	Chip Select Access Time	-	85	-	100	-	120	ns
4	tOE	Output Enable to Output Valid	-	40	-	50	-	60	ns
5	tBA	/LB, /UB Access Time	-	85	-	100	-	120	ns
6	tCLZ	Chip Select to Output in Low Z	10	-	20	-	20	-	ns
7	tOLZ	Output Enable to Output in Low Z	5	-	5	-	10	-	ns
8	tBLZ	/LB, /UB Enable to Output in Low Z	10	-	20	-	20	-	ns
9	tCHZ	Chip Deselection to Output in High Z	0	30	0	30	0	40	ns
10	tOHZ	Out Disable to Output in High Z	0	30	0	30	0	40	ns
11	tBHZ	/LB, /UB Disable to Output in High Z	0	30	0	30	0	40	ns
12	tOH	Output Hold from Address Change	10	-	15	-	15	-	ns
	WRITE CYCLE								
13	tWC	Write Cycle Time	85	-	100	-	120	-	ns
14	tCW	Chip Selection to End of Write	70	-	80	-	100	-	ns
15	tAW	Address Valid to End of Write	70	-	80	-	100	-	ns
16	tBW	/LB, /UB Valid to End of Write	70	-	80	-	100	-	ns
17	tAS	Address Set-up Time	0	-	0	-	0	-	ns
18	tWP	Write Pulse Width	55	-	75	-	85	-	ns
19	tWR	Write Recovery Time	0	-	0	-	0	-	ns
20	tWHZ	Write to Output in High Z	0	30	0	35	0	40	ns
21	tDW	Data to Write Time Overlap	35	-	45	-	50	-	ns
22	tDH	Data Hold from Write Time	0	-	0	-	0	-	ns
23	tOW	Output Active from End of Write	5	-	10	-	10	-	ns

AC TEST CONDITIONS

T_A = 0°C to 70°C (Normal) /-40°C to 85°C (I), unless otherwise specified

Parameter		Value
Input Pulse Level		0.4V to 1.6V
Input Rise and Fall Time		5ns
Input and Output Timing Reference Level		0.9V
Output Load	tCLZ,tOLZ,tBLZ,tCHZ,tOHZ,tBHZ,tWHZ,tOW	CL = 5pF + 1TTL Load
	Others	CL = 30pF + 1TTL Load

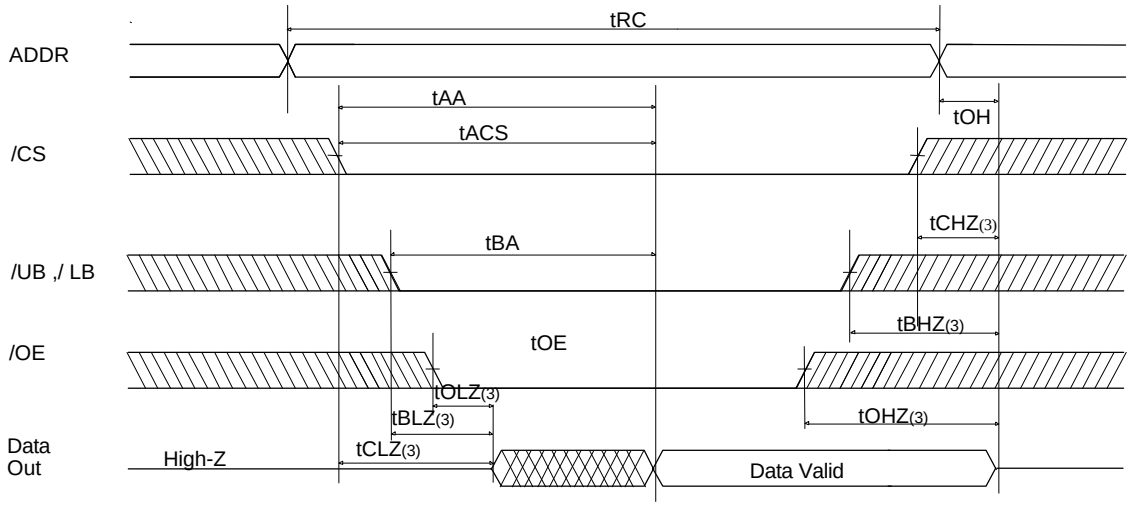
AC TEST LOADS



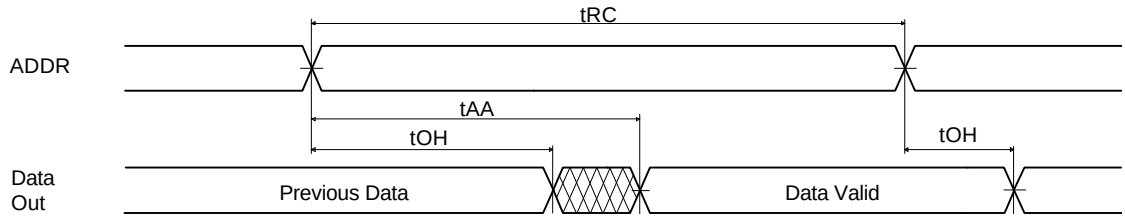
Note :
1. Including jig and scope capacitance

TIMING DIAGRAM

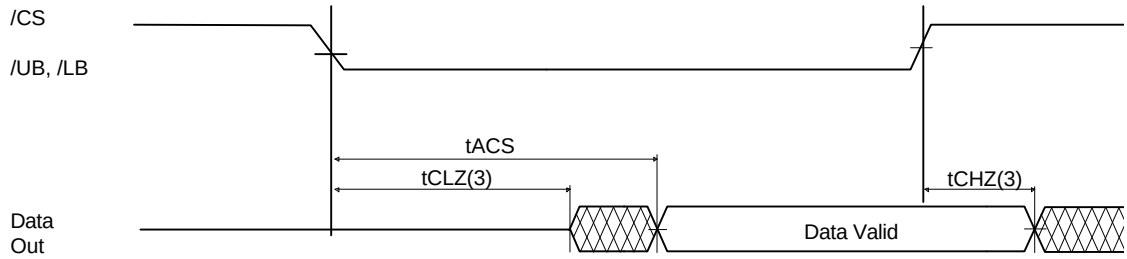
READ CYCLE 1(Note 1,4)



READ CYCLE 2(Note 2,3,4)

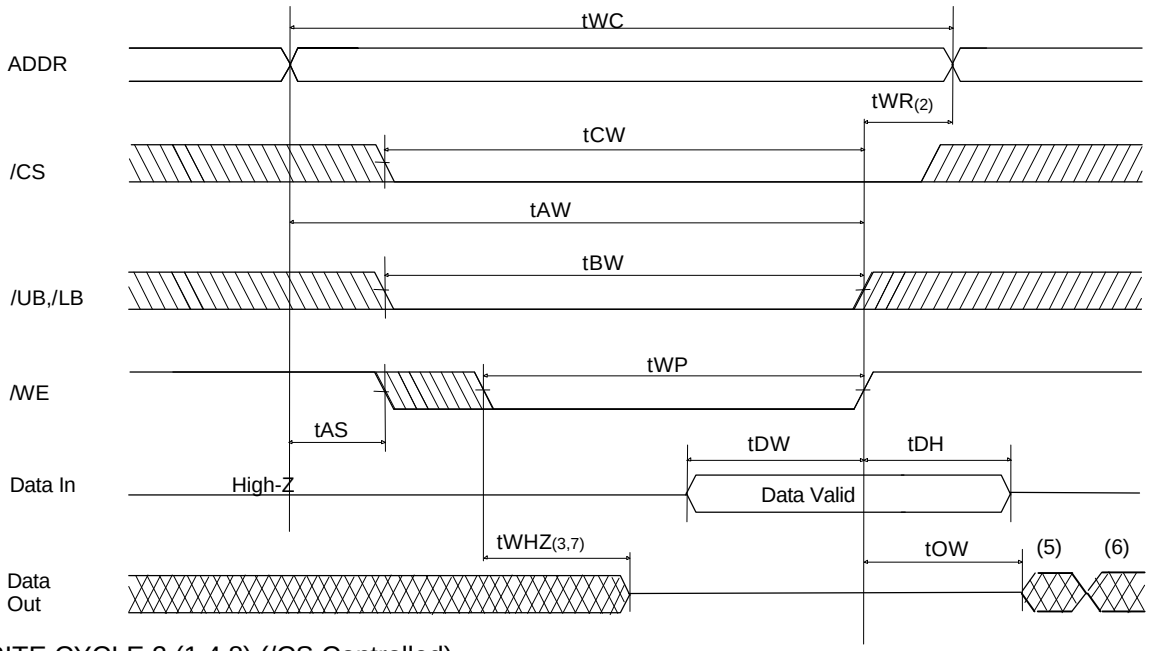


READ CYCLE 3(Note 1,2,4)

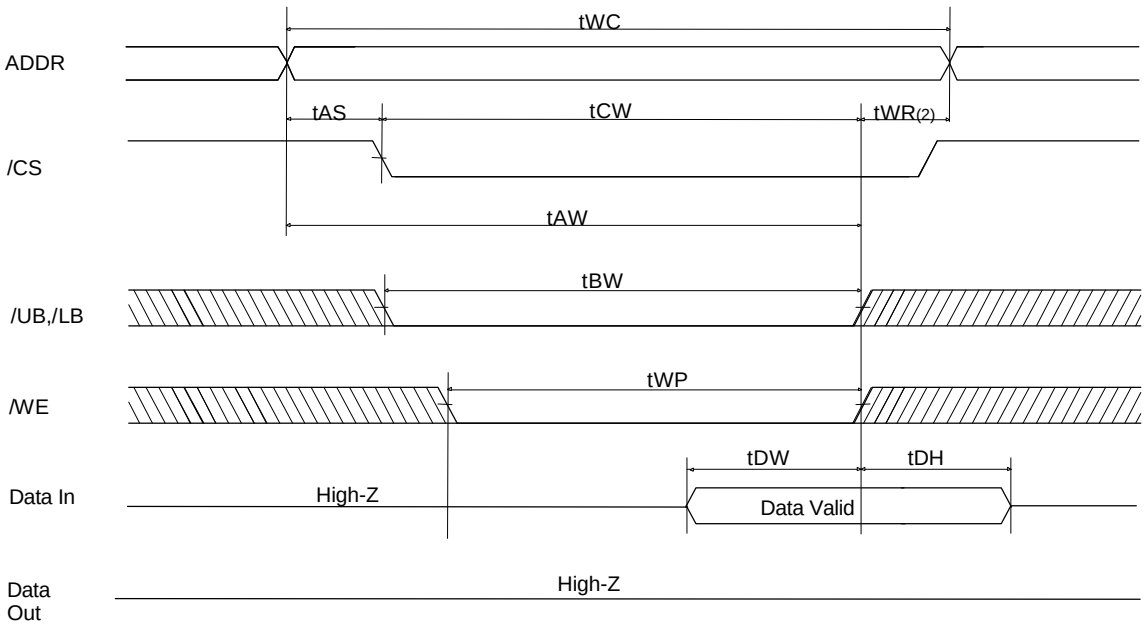


Notes:
A read occurs during the overlap of a low /OE, a high /WE, a low /CS1 and low /UB and/or /LB.
2. /OE = V_{IL}
3. Transition is measured ± 200mV from steady state voltage.
   This parameter is sampled and not 100% tested.
4. /CS in high for the standby, low for active
   /UB and /LB in high for the standby, low for active

WRITE CYCLE 1 (1,4,8) (/WE Controlled)



WRITE CYCLE 2 (1,4,8) (/CS Controlled)



Notes:

1. A write occurs during the overlap of a low /WE, a low /CS1 and low /UB and/or /LB.
2. tWR is measured from the earlier of /CS, /LB, /UB, or /WE going high to the end of write cycle.
3. During this period, I/O pins are in the output state so that the input signals of opposite phase to the output must not be applied.
4. If the /CS, /LB and /UB low transition occur simultaneously with the /WE low transition or after the /WE transition, outputs remain in a high impedance state.
5. Q(data out) is the same phase with the write data of this write cycle.
6. Q(data out) is the read data of the next address.
7. Transition is measured +200mV from steady state.
   This parameter is sampled and not 100% tested.
8. /CS in high for the standby, low for active
   /UB and /LB in high for the standby, low for active

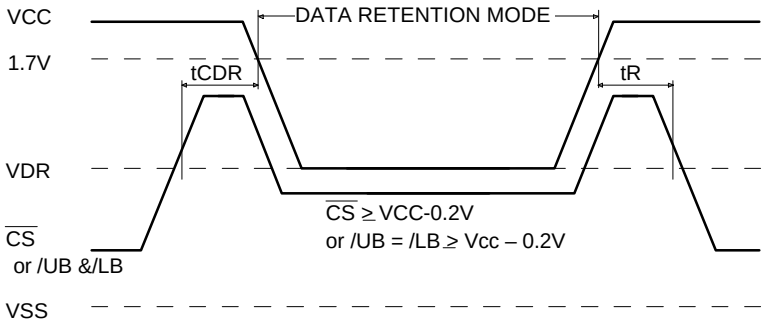
DATA RETENTION ELECTRIC CHARACTERISTIC

T_A = 0°C to 70°C /-40°C to 85°C (I)

Symbol	Parameter	Test Condition		Min.	Typ.	Max.	Unit
V_{DR}	Vcc for Data Retention	/CS ≥ Vcc - 0.2V or /UB = /LB ≥ Vcc-0.2V, V_{IN} ≥ Vcc - 0.2V or V_{IN} ≤ Vss + 0.2V		1.2	-	2.3	V
I_{CCDR}	Data Retention Current	Vcc=1.5V, /CS ≥ Vcc - 0.2V or /UB = /LB ≥ Vcc-0.2V, V_{IN} ≥ Vcc - 0.2V or V_{IN} ≤ Vss + 0.2V	LL	-	-	3	uA
			SL	-	-	1	uA
tCDR	Chip Deselect to Data Retention Time	See Data Retention Timing Diagram		0	-	-	ns
tR	Operating Recovery Time			tRC(3)	-	-	ns

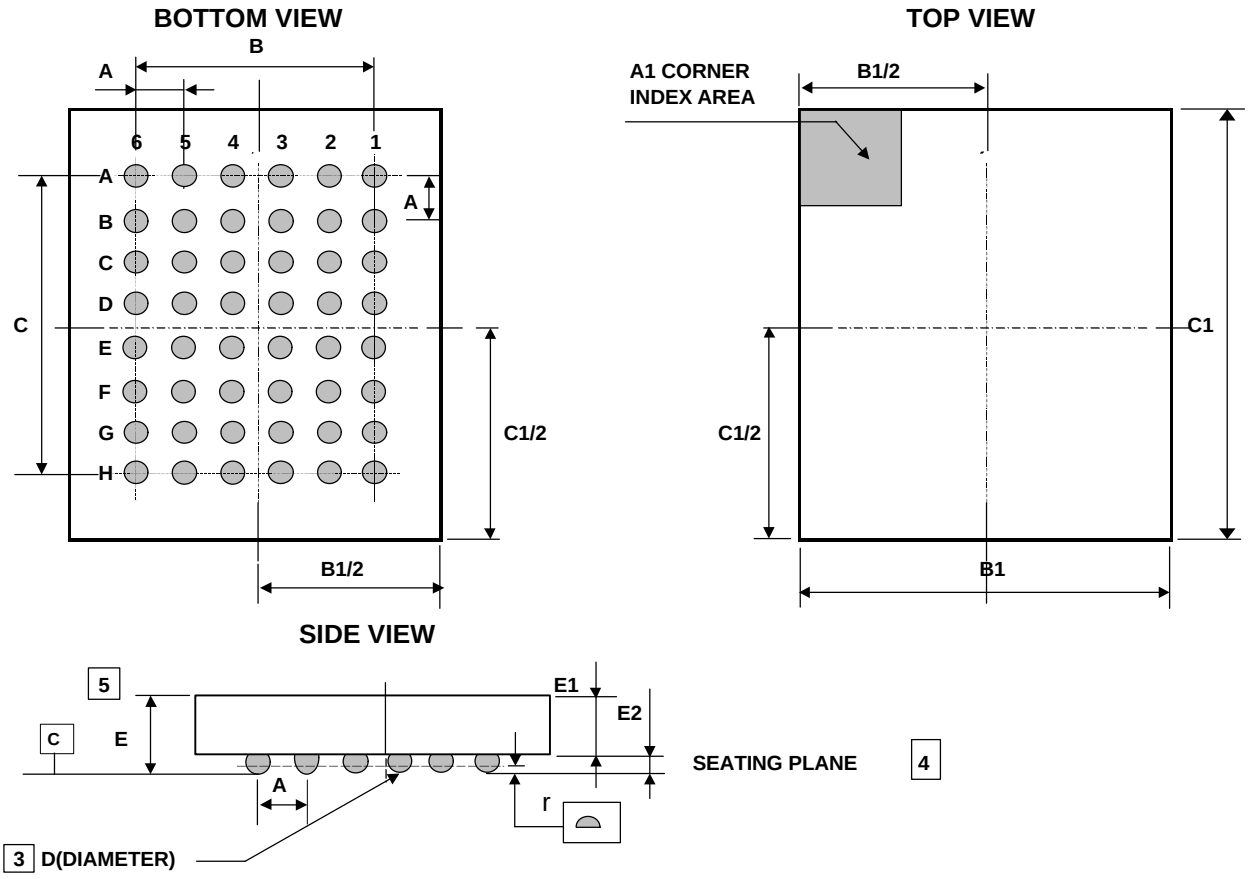
Notes:
1. Typical values are under the condition of T_A = 25°C.
2. Typical Values are sampled and not 100% tested
3. tRC is read cycle time.

DATA RETENTION TIMING DIAGRAM



PACKAGE INFORMATION

48ball Fine Pitch Ball Grid Array Package(F)

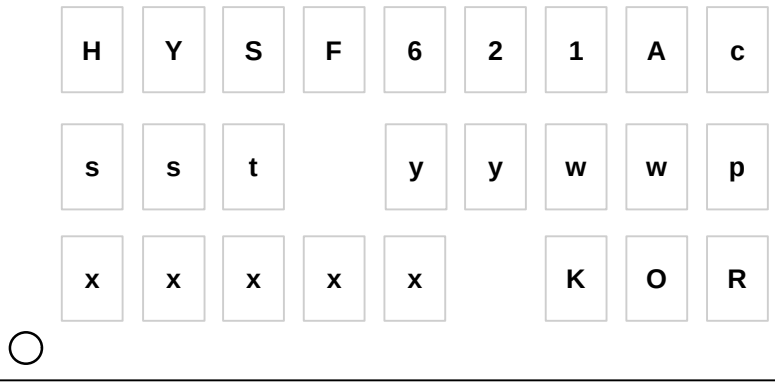


Symbol	Min.	Typ.	Max.
A	-	0.75	-
B	-	3.75	-
B1	6.9	7.0	7.1
C	-	5.25	-
C1	7.9	8.0	8.1
D	0.3	0.35	0.4
E	-	1.0	1.1
E1	0.74	0.78	0.82
E2	0.17	0.22	0.27
r	-	-	0.08

Note

1. DIMENSIONING and TOLERANCING PER ASME Y14. 5M-1994.
2. ALL DIMENSIONS ARE MILLIMETERS.
3. DIMENSION “D” IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER IN A PLANE PARALLEL TO DATUM C.
4. PRIMARY DATUM C(SEATING PLANE) IS DEFINED BY THE CROWN OF THE SOLDER BALLS.
5. THIS IS A CONTROLLING DIMENSION.

MARKING INSTRUCTION

Package	Marking Example
FBGA	

Index

- **HYSF621Ac** : Part Name
  c : Power Consumption
  - L : Low Low Power
  - S : Super Low Power
- **ss** : Speed
  - 85 : 85ns
  - 10 : 100ns
  - 12 : 120ns
- **t** : Temperature
  - C : Industrial (-0 ~ 70 °C)
  - I : Industrial (-40 ~ 85 °C)
- **yy** : Year (ex : 00 = year 2000, 01= year 2001)
- **ww** : Work Week (ex : 12 = work week 12)
- **p** : Process Code
- **xxxxx** : Lot No.
- **KOR** : Origin Country

Note
- Capital Letter : Fixed Item
- Small Letter : Non-fixed Item