Preliminary

CAT24WC03/05/09/17

2K/4K/8K/16K-Bit Serial E²PROM

FEATURES

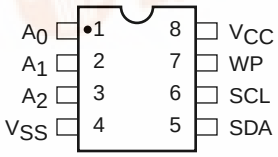
- 400 KHZ I²C Bus Compatible*
- 1.8 to 6.0Volt Operation
- Low Power CMOS Technology
- Write Protect Feature
  –Top 1/2 Array Protected When WP at V_{IH}
- 16-Byte Page Write Buffer
- Self-Timed Write Cycle with Auto-Clear
- 1,000,000 Program/Erase Cycles
- 100 Year Data Retention
- 8-pin DIP, 8-pin SOIC and 8-pin TSSOP Package
- Commercial, Industrial and Automotive Temperature Ranges

DESCRIPTION

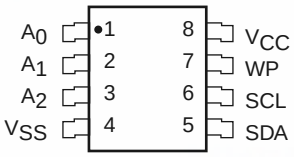
The CAT24WC03/05/09/17 is a 2K/4K/8K/16K-bit Serial CMOS E²PROM internally organized as 256/512/1024/2048 words of 8 bits each. Catalyst's advanced CMOS technology substantially reduces device power requirements. The CAT24WC03/05/09/17 features a 16-byte page write buffer. The device operates via the I²C bus serial interface, has a special write protection feature, and is available in 8-pin DIP or 8-pin SOIC

PIN CONFIGURATION

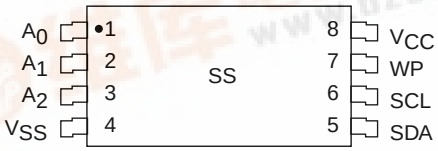
DIP Package (P)



SOIC Package (J)



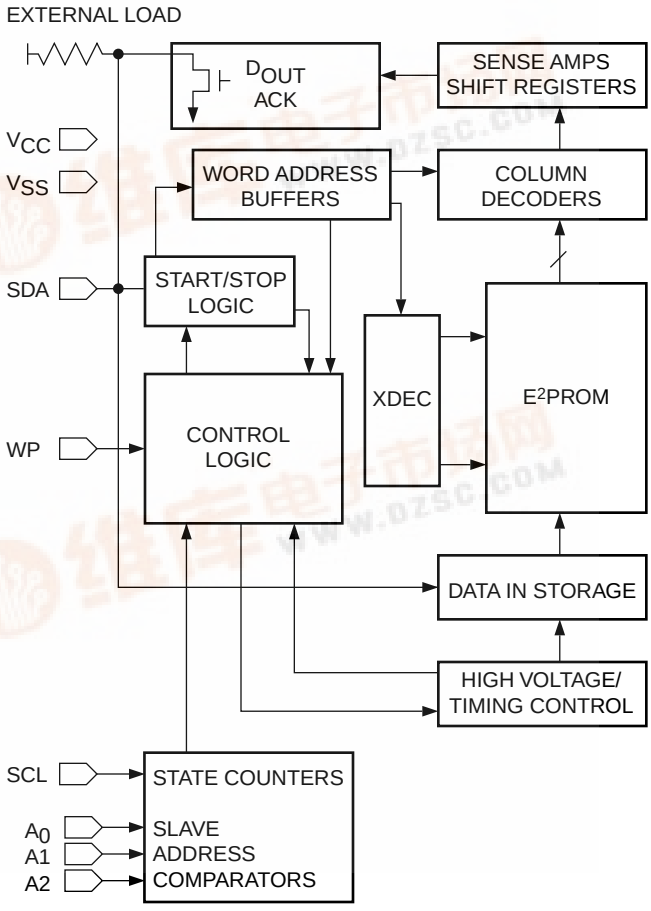
TSSOP Package (U)
(** Available for 24WC03 only)



PIN FUNCTIONS

Pin Name	Function
A0, A1, A2	Device Address Inputs
SDA	Serial Data/Address
SCL	Serial Clock
WP	Write Protect
V_{CC}	+1.8V to +6.0V Power Supply
V_{SS}	Ground

BLOCK DIAGRAM



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*Catalyst Semiconductor is licensed by Philips Corporation to carry the I²C Bus Protocol.

ABSOLUTE MAXIMUM RATINGS*

Temperature Under Bias ..... –55°C to +125°C
Storage Temperature ..... –65°C to +150°C
Voltage on Any Pin with
Respect to Ground(1) ..... –2.0V to +V_{CC} + 2.0V
V_{CC} with Respect to Ground ..... –2.0V to +7.0V
Package Power Dissipation
Capability (Ta = 25°C) 1.0W
Lead Soldering Temperature (10 secs) ..... 300°C
Output Short Circuit Current(2) 100mA

*COMMENT

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions outside of those listed in the operational sections of this specification is not implied. Exposure to any absolute maximum rating for extended periods may affect device performance and reliability.

RELIABILITY CHARACTERISTICS

Symbol	Parameter	Min.	Max.	Units	Reference Test Method
N_{END}(3)	Endurance	1,000,000		Cycles/Byte	MIL-STD-883, Test Method 1033
T_{DR}(3)	Data Retention	100		Years	MIL-STD-883, Test Method 1008
V_{ZAP}(3)	ESD Susceptibility	2000		Volts	MIL-STD-883, Test Method 3015
I_{LTH}(3)(4)	Latch-up	100		mA	JEDEC Standard 17

D.C. OPERATING CHARACTERISTICS

V_{CC} = +1.8V to +6.0V, unless otherwise specified.

Symbol	Parameter	Limits			Units	Test Conditions
		Min.	Typ.	Max.		
I_{CC}	Power Supply Current			3	mA	f_{SCL} = 100 KHz
I_S(5)	Standby Current (V_{CC} = 5.0V)			0	µA	V_{IN} = GND or V_{CC}
I_{LI}	Input Leakage Current			10	µA	V_{IN} = GND to V_{CC}
I_{LO}	Output Leakage Current			10	µA	V_{OUT} = GND to V_{CC}
V_{IL}	Input Low Voltage	–1		V_{CC} x 0.3	V	
V_{IH}	Input High Voltage	V_{CC} x 0.7		V_{CC} + 0.5	V	
V_{OL1}	Output Low Voltage (V_{CC} = 3.0V)			0.4	V	I_{OL} = 3 mA
V_{OL2}	Output Low Voltage (V_{CC} = 1.8V)			0.5	V	I_{OL} = 1.5 mA

CAPACITANCE T_A = 25°C, f = 1.0 MHz, V_{CC} = 5V

Symbol	Test	Max.	Units	Conditions
$C_{I/O}$(3)	Input/Output Capacitance (SDA)	8	pF	$V_{I/O}$ = 0V
C_{IN}(3)	Input Capacitance (A0, A1, A2, SCL, WP)	6	pF	V_{IN} = 0V

Note:
(1) The minimum DC input voltage is –0.5V. During transitions, inputs may undershoot to –2.0V for periods of less than 20 ns. Maximum DC voltage on output pins is V_{CC} +0.5V, which may overshoot to V_{CC} + 2.0V for periods of less than 20ns.
(2) Output shorted for no more than one second. No more than one output shorted at a time.
(3) This parameter is tested initially and after a design or process change that affects the parameter.
(4) Latch-up protection is provided for stresses up to 100 mA on address and data pins from –1V to V_{CC} +1V.
(5) Standby Current (I_{SB}) = 0µA (<900nA).

A.C. CHARACTERISTICS

V_{CC} = +1.8V to +6.0V, unless otherwise specified.

Read & Write Cycle Limits

Symbol	Parameter	1.8V, 2.5V		4.5V-5.5V		Units
		Min.	Max.	Min.	Max.	
F_{SCL}	Clock Frequency		100		400	kHz
T_I(1)	Noise Suppression Time Constant at SCL, SDA Inputs		200		200	ns
t_{AA}	SCL Low to SDA Data Out and ACK Out		3.5		1	µs
t_{BUF}(1)	Time the Bus Must be Free Before a New Transmission Can Start	4.7		1.2		µs
$t_{HD:STA}$	Start Condition Hold Time	4		0.6		µs
t_{LOW}	Clock Low Period	4.7		1.2		µs
t_{HIGH}	Clock High Period	4		0.6		µs
$t_{SU:STA}$	Start Condition Setup Time (for a Repeated Start Condition)	4.7		0.6		µs
$t_{HD:DAT}$	Data In Hold Time	0		0		ns
$t_{SU:DAT}$	Data In Setup Time	50		50		ns
t_R(1)	SDA and SCL Rise Time		1		0.3	µs
t_F(1)	SDA and SCL Fall Time		300		300	ns
$t_{SU:STO}$	Stop Condition Setup Time	4		0.6		µs
t_{DH}	Data Out Hold Time	100		100		ns

Power-Up Timing(1)(2)

Symbol	Parameter	Max.	Units
t_{PUR}	Power-up to Read Operation	1	ms
t_{PUW}	Power-up to Write Operation	1	ms

Write Cycle Limits

Symbol	Parameter	Min.	Typ.	Max	Units
t_{WR}	Write Cycle Time			10	ms

The write cycle time is the time from a valid stop condition of a write sequence to the end of the internal program/erase cycle. During the write cycle, the bus interface circuits are disabled, SDA is allowed to remain high, and the device does not respond to its slave address.

Note:
(1) This parameter is tested initially and after a design or process change that affects the parameter.
(2) t_{PUR} and t_{PUW} are the delays required from the time V_{CC} is stable until the specified operation can be initiated.

FUNCTIONAL DESCRIPTION

The CAT24WC03/05/09/17 supports the I^2C Bus data transmission protocol. This Inter-Integrated Circuit Bus protocol defines any device that sends data to the bus to be a transmitter and any device receiving data to be a receiver. Data transfer is controlled by the Master device which generates the serial clock and all START and STOP conditions for bus access. The CAT24WC03/05/09/17 operates as a Slave device. Both the Master and Slave devices can operate as either transmitter or receiver, but the Master device controls which mode is activated. A maximum of 8 devices (24WC03), 4 devices (24WC05), 2 devices (24WC09) and 1 device (24WC17) may be connected to the bus as determined by the device address inputs A0, A1, and A2.

PIN DESCRIPTIONS

SCL: Serial Clock
The CAT24WC03/05/09/17 serial clock input pin is used to clock all data transfers into or out of the device. This is an input pin.

SDA: Serial Data/Address
The CAT24WC03/05/09/17 bidirectional serial data/address pin is used to transfer data into and out of the device. The SDA pin is an open drain output and can be wire-ORed with other open drain or open collector outputs.

A0, A1, A2: Device Address Inputs
These inputs set device address when cascading multiple devices. When these pins are left floating the default values are zeros.

A maximum of eight devices can be cascaded when using 24WC03 device. All three address pins are used

Figure 1. Bus Timing

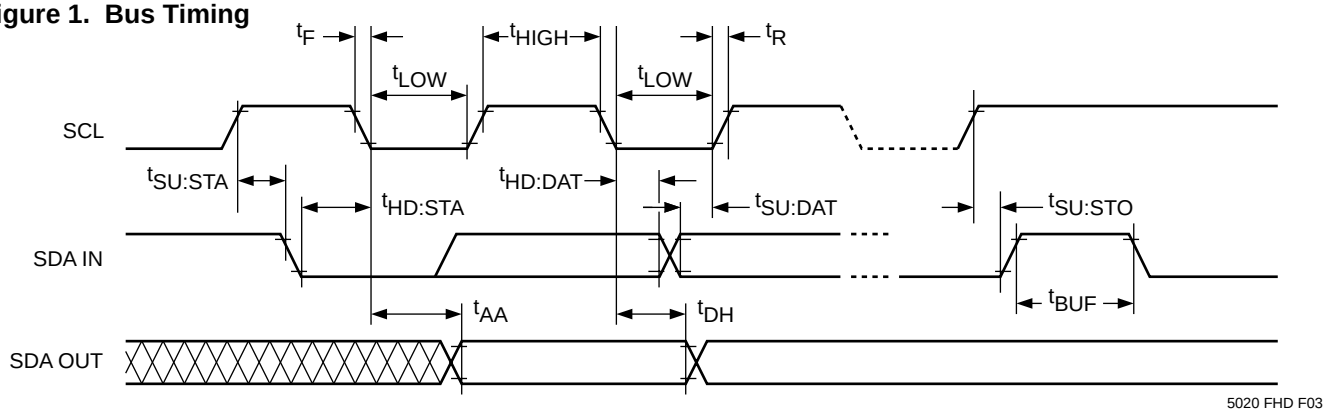

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Figure 2. Write Cycle Timing

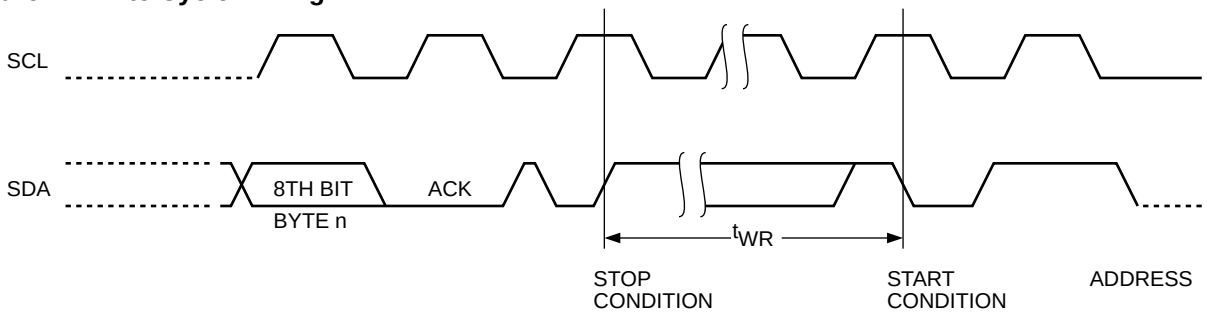

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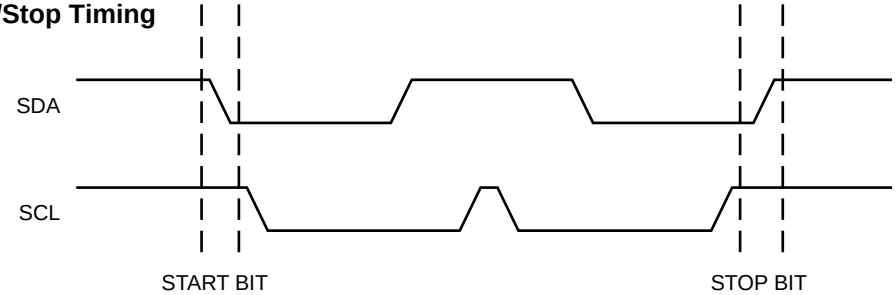
Figure 3. Start/Stop Timing



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for 24WC03. If only one 24WC03 is addressed on the bus, all three address pins (A0, A1, and A2) can be left floating or connected to V_{SS}

A total of four devices can be addressed on a single bus when using 24WC05 device. Only A1 and A2 address pins are used with this device. The A0 address pin is a no connect pin and can be tied to V_{SS} or left floating. If only one 24WC05 is being addressed on the bus, the address pins (A1 and A2) can be left floating or connected to V_{SS}.

Only two devices can be cascaded when using 24WC09. The only address pin used with this device is A2. The A0 and A1address pins are no connect pins and can be tied to V_{SS} or left floating. If only one 24WC09 is being addressed on the bus, the address pin (A2) can be left floating or connected to V_{SS}.

The 24WC17 is a stand alone device. In this case, all address pins (A0, A1and A2) are no connect pins and can be tied to V_{SS} or left floating.

WP: Write Protect
If the WP pin is tied to V_{CC} the upper half of memory array becomes Write Protected (READ only)(locations 80H to FFH for 24WC03, locations 100H to 1FFH for 24WC05, locations 200H to 3FFH for 24WC09, locations 400H to 7FFH for 24WC17). When the WP pin is tied to V_{SS} or left floating normal read/write operations are allowed to the device.

I²C BUS PROTOCOL

The following defines the features of the I²C bus protocol:

(1) Data transfer may be initiated only when the bus is not busy.

(2) During a data transfer, the data line must remain stable whenever the clock line is high. Any changes in the data line while the clock line is high will be interpreted as a START or STOP condition.

START Condition

The START Condition precedes all commands to the device, and is defined as a HIGH to LOW transition of SDA when SCL is HIGH. The CAT24WC03/05/09/17 monitor the SDA and SCL lines and will not respond until this condition is met.

STOP Condition

A LOW to HIGH transition of SDA when SCL is HIGH determines the STOP condition. All operations must end with a STOP condition.

DEVICE ADDRESSING

The bus Master begins a transmission by sending a START condition. The Master then sends the address of the particular slave device it is requesting. The four

Figure 4. Acknowledge Timing

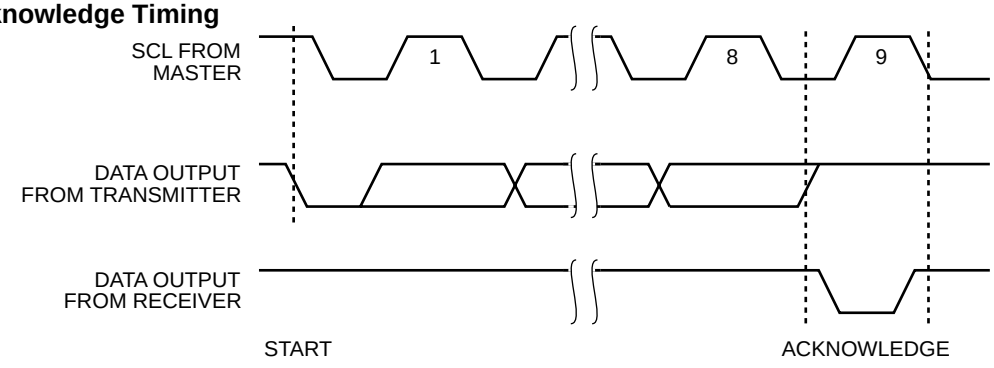

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Figure 5. Slave Address Bits

24WC03	1	0	1	0	A2	A1	A0	R/$\overline{W}$
24WC05	1	0	1	0	A2	A1	a8	R/$\overline{W}$
24WC09	1	0	1	0	A2	a9	a8	R/$\overline{W}$
24WC17	1	0	1	0	a10	a9	a8	R/$\overline{W}$

* A0, A1 and A2 correspond to pin 1, pin 2 and pin 3 of the device.
** a8, a9 and a10 correspond to the address of the memory array address word.
***A0, A1 and A2 must compare to its corresponding hard wired input pins (pins 1, 2 and 3).

most significant bits of the 8-bit slave address are fixed as 1010 for the CAT24WC03/05/09/17 (see Fig. 5). The next three significant bits (A2, A1, A0) are the device address bits and define which device or which part of the device the Master is accessing. Up to eight CAT24WC03, four CAT24WC05, two CAT24WC09, and one CAT24WC17 may be individually addressed by the system. The last bit of the slave address specifies whether a Read or Write operation is to be performed. When this bit is set to 1, a Read operation is selected, and when set to 0, a Write operation is selected.

After the Master sends a START condition and the slave address byte, the CAT24WC03/05/09/17 monitors the bus and responds with an acknowledge (on the SDA line) when its address matches the transmitted slave address. The CAT24WC03/05/09/17 then performs a Read or Write operation depending on the state of the R/$\overline{W}$ bit.

Acknowledge

After a successful data transfer, each receiving device is required to generate an acknowledge. The Acknowledging device pulls down the SDA line during the ninth clock cycle, signaling that it received the 8 bits of data.

The CAT24WC03/05/09/17 responds with an acknowledge after receiving a START condition and its slave address. If the device has been selected along with a write operation, it responds with an acknowledge after receiving each 8-bit byte.

When the CAT24WC03/05/09/17 is in a READ mode it transmits 8 bits of data, releases the SDA line, and monitors the line for an acknowledge. Once it receives this acknowledge, the CAT24WC03/05/09/17 will continue to transmit data. If no acknowledge is sent by the Master, the device terminates data transmission and waits for a STOP condition.

WRITE OPERATIONS

Byte Write

In the Byte Write mode, the Master device sends the START condition and the slave address information (with the R/$\overline{W}$ bit set to zero) to the Slave device. After the Slave generates an acknowledge, the Master sends the byte address that is to be written into the address pointer of the CAT24WC03/05/09/17. After receiving another acknowledge from the Slave, the Master device transmits the data byte to be written into the addressed memory location. The CAT24WC03/05/09/17 acknowledge once more and the Master generates the STOP condition, at which time the device begins its internal programming cycle to nonvolatile memory. While this internal cycle is in progress, the device will not respond to any request from the Master device.

Page Write

The CAT24WC03/05/09/17 writes up to 16 bytes of data in a single write cycle, using the Page Write operation. The Page Write operation is initiated in the same manner as the Byte Write operation, however instead of terminating after the initial word is transmitted, the Master is allowed to send up to 15 additional bytes. After each byte has been transmitted the CAT24WC03/05/09/17 will respond with an acknowledge, and internally increment

Figure 6. Byte Write Timing

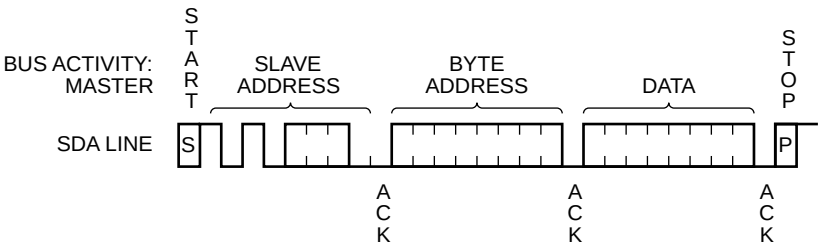

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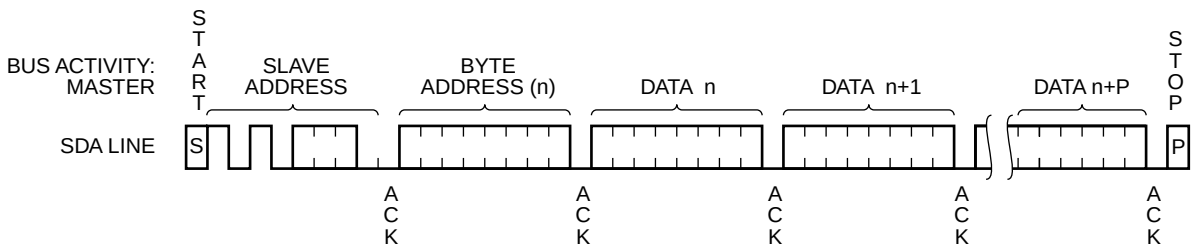
Figure 7. Page Write Timing



NOTE: IN THIS EXAMPLE n = XXXX 0000(B); X = 1 or 0

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the low order address bits by one. The high order bits remain unchanged.

If the Master transmits more than 16 bytes prior to sending the STOP condition, the address counter 'wraps around', and previously transmitted data will be overwritten.

Once all 16 bytes are received and the STOP condition has been sent by the Master, the internal programming cycle begins. At this point all received data is written to the CAT24WC03/05/09/17 in a single write cycle.

Acknowledge Polling

The disabling of the inputs can be used to take advantage of the typical write cycle time. Once the stop condition is issued to indicate the end of the host's write operation, the CAT24WC03/05/09/17 initiates the internal write cycle. ACK polling can be initiated immediately. This involves issuing the start condition followed by the slave address for a write operation. If the CAT24WC03/05/09/17 is still busy with the write operation, no ACK will be returned. If the CAT24WC03/05/09/17 has completed the write operation, an ACK will be returned and the host can then proceed with the next read or write operation.

WRITE PROTECTION

The Write Protection feature allows the user to protect against inadvertent programming of the memory array. If the WP pin is tied to V_{CC}, the upper half (locations 80H to FFH for 24WC03, locations 100H to 1FFH for 24WC05, locations 200H to 3FFH for 24WC09, locations 400H to 7FFH for 24WC17) of the memory array is protected and becomes read only. The CAT24WC03/05/09/17 will accept both slave and byte addresses, but the memory location accessed is protected from programming by the device's failure to send an acknowledge after the first byte of data is received.

READ OPERATIONS

The READ operation for the CAT24WC03/05/09/17 is initiated in the same manner as the write operation with the one exception that the R/$\overline{W}$ bit is set to a one. Three different READ operations are possible: Immediate Address READ, Selective READ and Sequential READ.

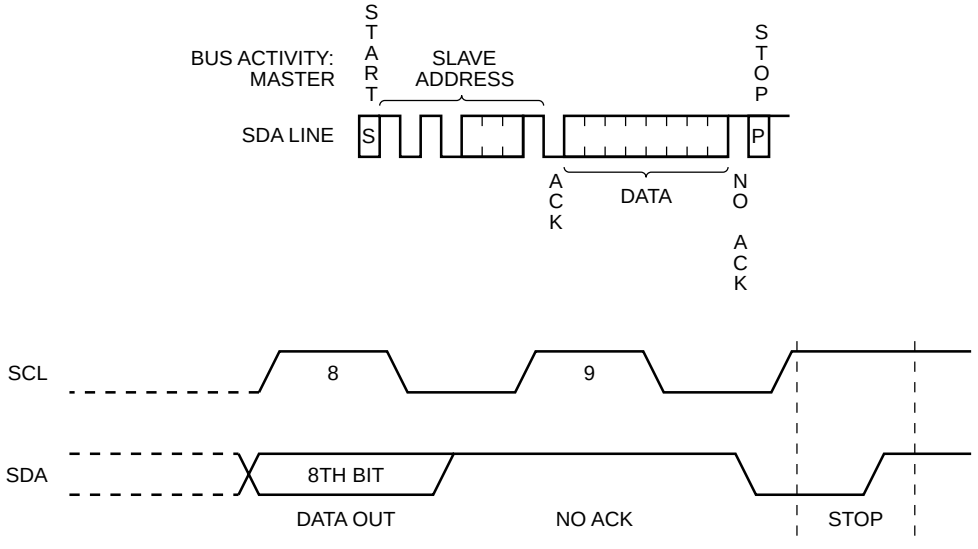
Immediate Address Read

The CAT24WC03/05/09/17's address counter contains the address of the last byte accessed, incremented by one. In other words, if the last READ or WRITE access was to address N, the READ immediately following would access data from address N+1. If N=E (where E = 255 for 24WC03, 511 for 24WC05, 1023 for 24WC09, and 2047 for 24WC17), then the counter will 'wrap around' to address 0 and continue to clock out data. After the CAT24WC03/05/09/17 receives its slave address information (with the R/$\overline{W}$ bit set to one), it issues an acknowledge, then transmits the 8-bit byte requested. The master device does not send an acknowledge but will generate a STOP condition.

Selective Read

Selective READ operations allow the Master device to select at random any memory location for a READ operation. The Master device first performs a 'dummy' write operation by sending the START condition, slave address and byte address of the location it wishes to read. After the CAT24WC03/05/09/17 acknowledge the word address, the Master device resends the START condition and the slave address, this time with the R/$\overline{W}$ bit set to one. The CAT24WC03/05/09/17 then responds with its acknowledge and sends the 8-bit byte requested.

Figure 8. Immediate Address Read Timing



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The master device does not send an acknowledge but will generate a STOP condition.

Sequential Read

The Sequential READ operation can be initiated by either the Immediate Address READ or Selective READ operations. After the CAT24WC03/05/09/17 sends the initial 8-bit byte requested, the Master will respond with an acknowledge which tells the device it requires more data. The CAT24WC03/05/09/17 will continue to output an 8-bit byte for each acknowledge sent by the Master. The operation is terminated when the Master fails to respond with an acknowledge, thus sending the STOP condition.

The data being transmitted from the CAT24WC03/05/09/17 is outputted sequentially with data from address N followed by data from address N+1. The READ operation address counter increments all of the CAT24WC03/05/09/17 address bits so that the entire memory array can be read during one operation. If more than the E (where E = 255 for 24WC03, 511 for 24WC05, 1023 for 24WC09, and 2047 for 24WC17) bytes are read out, the counter will "wrap around" and continue to clock out data bytes.

Figure 9. Selective Read Timing

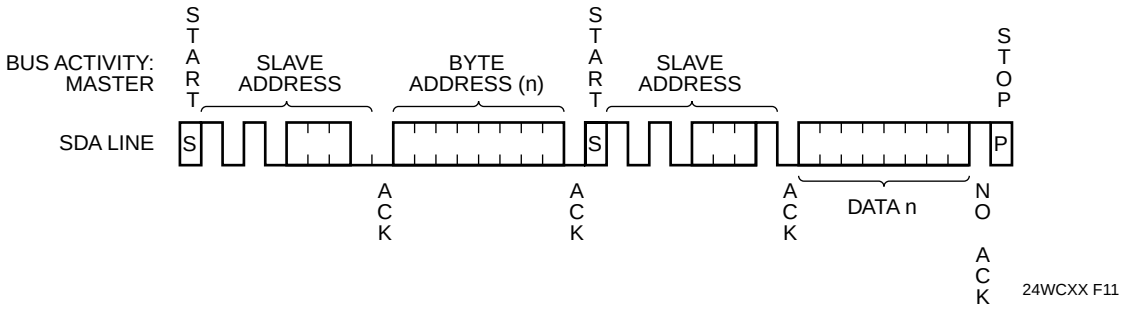
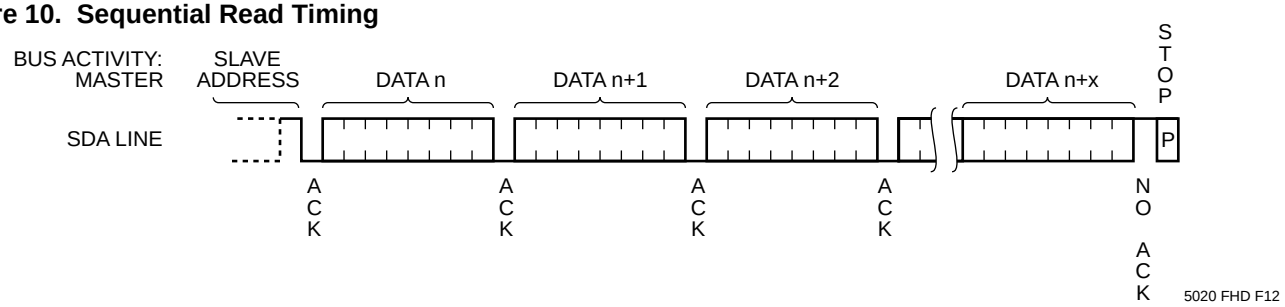
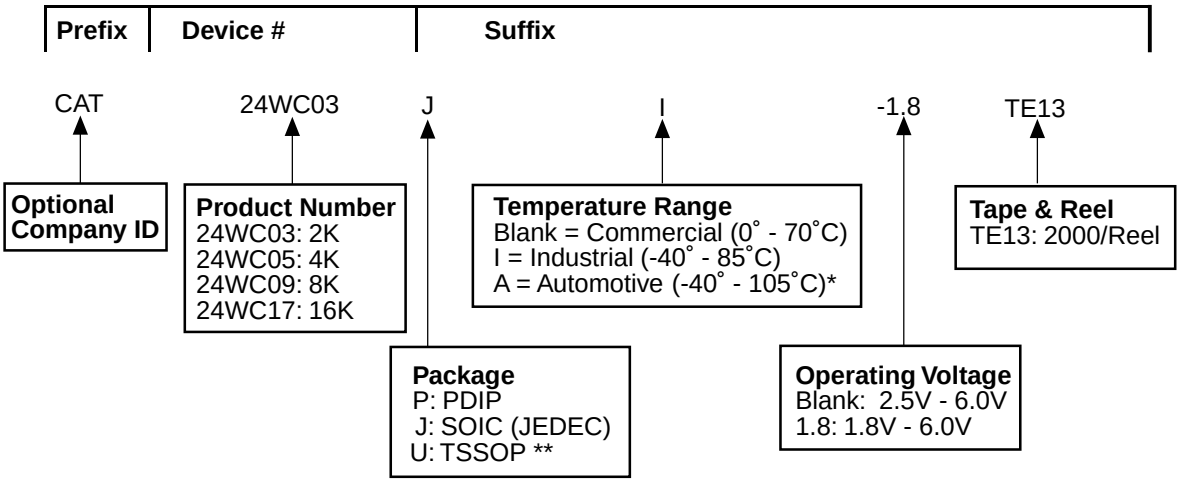


Figure 10. Sequential Read Timing



ORDERING INFORMATION



* -40˚ to +125˚C is available upon request

** Available for 24WC03

Notes:

(1) The device used in the above example is a 24WC03JI-1.8TE13 (SOIC, Industrial Temperature, 1.8 Volt to 6 Volt Operating Voltage, Tape & Reel)