



New Product

Si4464DY
Vishay Siliconix

N-Channel 200-V (D-S) MOSFET

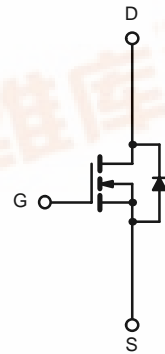
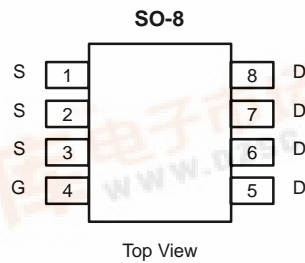
PRODUCT SUMMARY		
V_{DS} (V)	$r_{DS(on)}$ (Ω)	I_D (A)
200	0.240 @ $V_{GS} = 10$ V	2.2
	0.260 @ $V_{GS} = 6.0$ V	2.1

FEATURES

- TrenchFET® Power MOSFET
- PWM Optimized for (Lowest Q_g and Low R_G)

APPLICATIONS

- Primary Side Switch



ABSOLUTE MAXIMUM RATINGS ($T_A = 25^\circ\text{C}$ UNLESS OTHERWISE NOTED)					
Parameter	Symbol	10 secs	Steady State	Unit	
Drain-Source Voltage	V_{DS}	200		V	
Gate-Source Voltage	V_{GS}	± 20			
Continuous Drain Current ($T_J = 150^\circ\text{C}$) ^a	I_D	$T_A = 25^\circ\text{C}$	2.2	1.7	A
		$T_A = 70^\circ\text{C}$	1.7	1.3	
Pulsed Drain Current	I_{DM}	8			
Single Avalanche Current	I_{AS}	3		mJ	
Single Avalanche Energy	E_{AS}	0.45			
Continuous Source Current (Diode Conduction) ^a	I_S	2.1	1.2	A	
Maximum Power Dissipation ^a	P_D	$T_A = 25^\circ\text{C}$	2.5	1.5	W
		$T_A = 70^\circ\text{C}$	1.6	0.9	
Operating Junction and Storage Temperature Range	T_J, T_{stg}	-55 to 150		$^\circ\text{C}$	

THERMAL RESISTANCE RATINGS					
Parameter	Symbol	Typical	Maximum	Unit	
Maximum Junction-to-Ambient ^a	R_{thJA}	$t \leq 10$ sec	37	50	$^\circ\text{C/W}$
		Steady State	68	85	
Maximum Junction-to-Foot (Drain)	R_{thJF}	17	21		

Notes:
a. Surface Mounted on 1" x 1" FR4 Board.

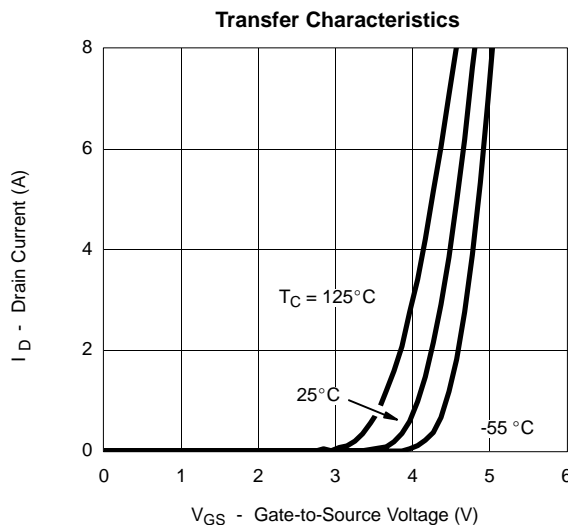
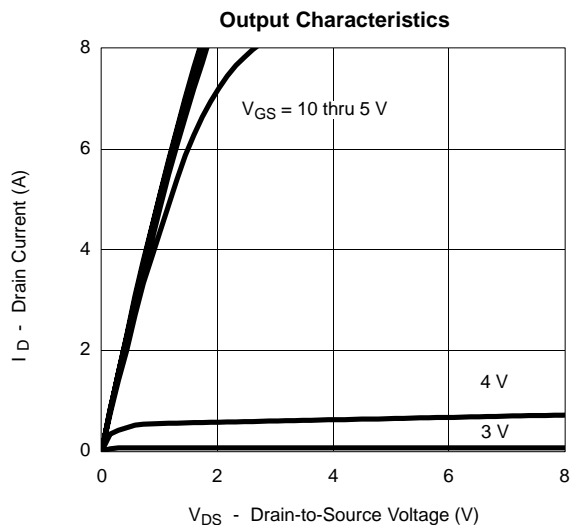


SPECIFICATIONS (T _J = 25 °C UNLESS OTHERWISE NOTED)						
Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Static						
Gate Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = 250 μA	2.0		4	V
Gate-Body Leakage	I _{GSS}	V _{DS} = 0 V, V _{GS} = ± 20 V			± 100	nA
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = 160 V, V _{GS} = 0 V			1	μA
		V _{DS} = 160 V, V _{GS} = 0 V, T _J = 55 °C			5	
On-State Drain Current ^a	I _{D(on)}	V _{DS} ≥ 5 V, V _{GS} = 10 V	8			A
Drain-Source On-State Resistance ^a	r _{DS(on)}	V _{GS} = 10 V, I _D = 2.2 A		0.195	0.240	Ω
		V _{GS} = 6.0 V, I _D = 2.1 A		0.210	0.260	
Forward Transconductance ^a	g _{fs}	V _{DS} = 15 V, I _D = 2.2 A		8.0		S
Diode Forward Voltage ^a	V _{SD}	I _S = 2.1 A, V _{GS} = 0 V		0.8	1.2	V
Dynamic^b						
Total Gate Charge	Q _g	V _{DS} = 100 V, V _{GS} = 10 V, I _D = 2.2 A		12	18	nC
Gate-Source Charge	Q _{gs}			2.5		
Gate-Drain Charge	Q _{gd}			3.8		
Gate Resistance	R _G			2.5		Ω
Turn-On Delay Time	t _{d(on)}	V _{DD} = 100 V, R _L = 100 Ω I _D ≅ 1.0 A, V _{GEN} = 10 V, R _G = 6 Ω		10	15	ns
Rise Time	t _r			12	20	
Turn-Off Delay Time	t _{d(off)}			15	25	
Fall Time	t _f			15	25	
Source-Drain Reverse Recovery Time	t _{rr}	I _F = 2.1 A, di/dt = 100 A/μs		60	90	

Notes

- a. Pulse test; pulse width ≤ 300 μs, duty cycle ≤ 2%.
- b. Guaranteed by design, not subject to production testing.

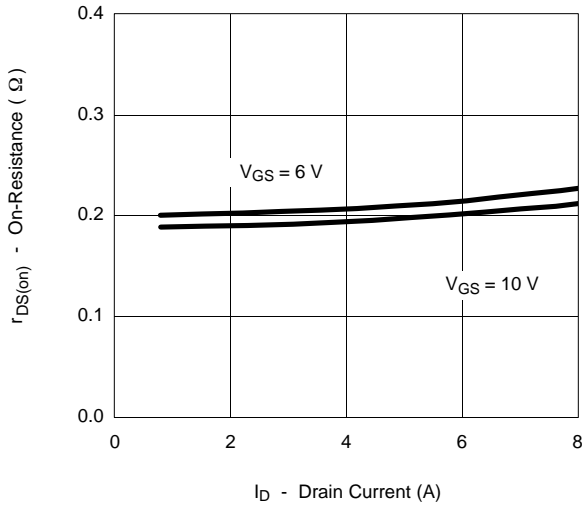
TYPICAL CHARACTERISTICS (25 °C UNLESS NOTED)



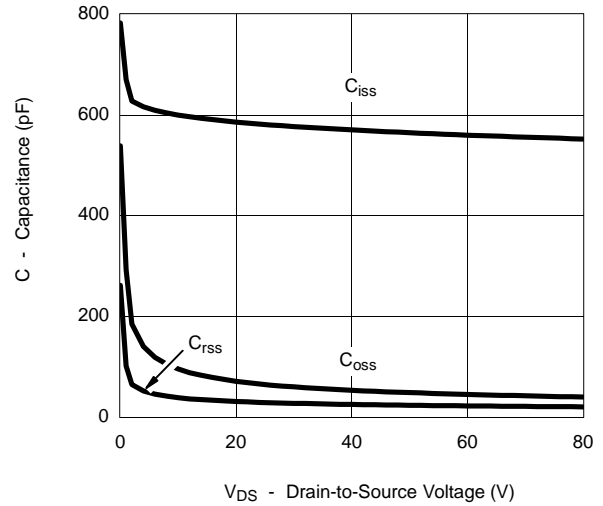


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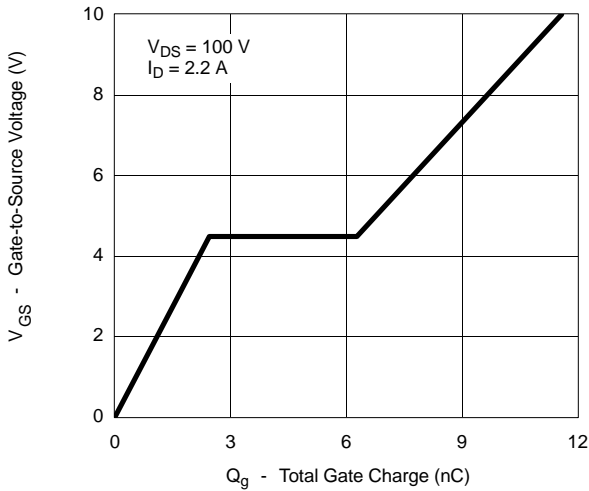
On-Resistance vs. Drain Current



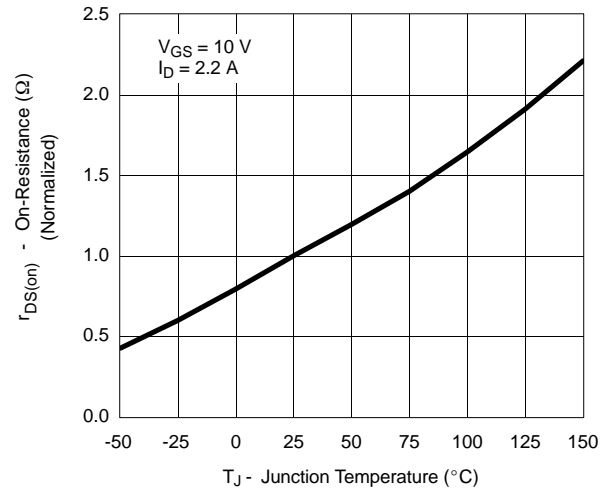
Capacitance



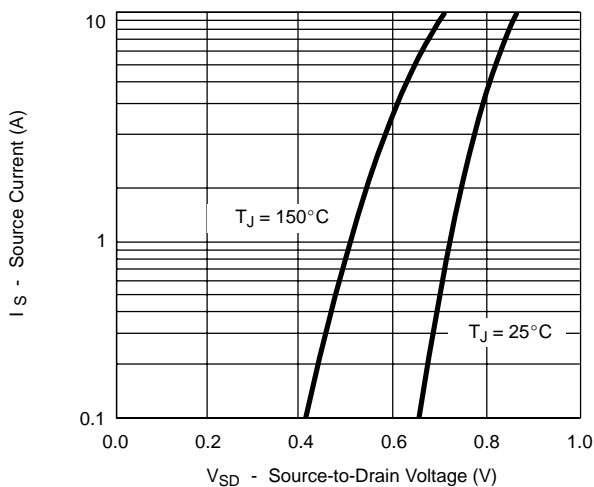
Gate Charge



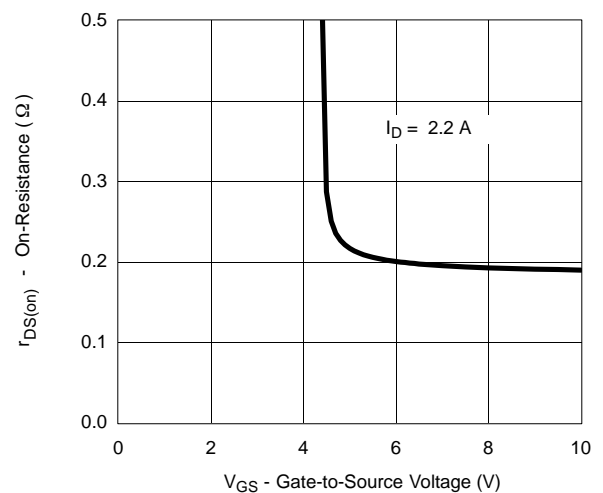
On-Resistance vs. Junction Temperature



Source-Drain Diode Forward Voltage

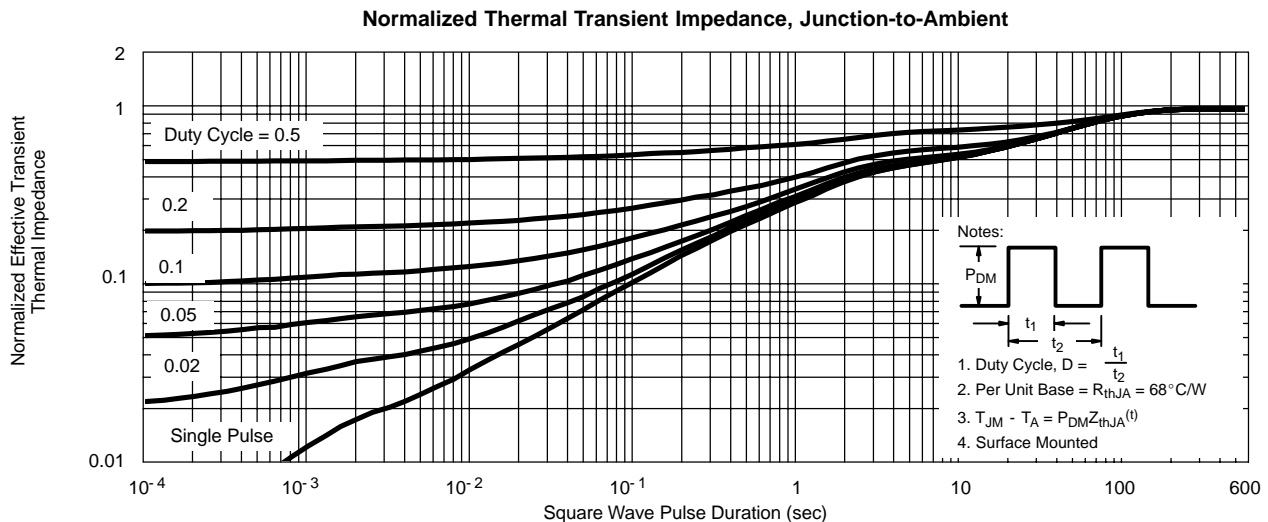
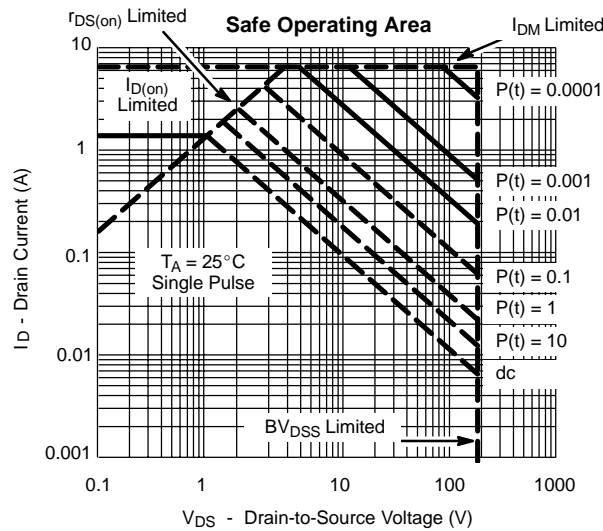
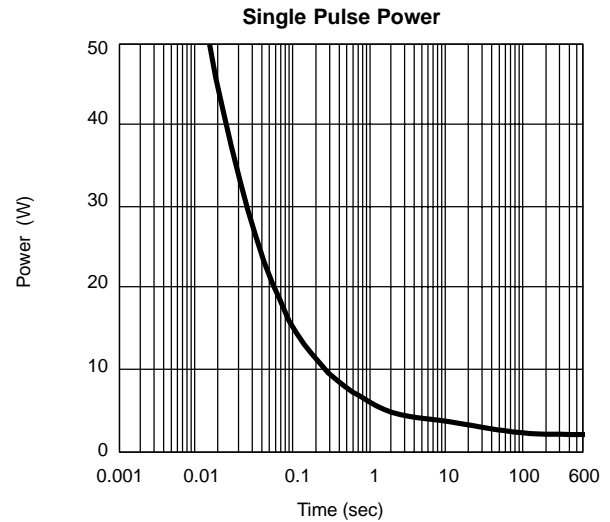
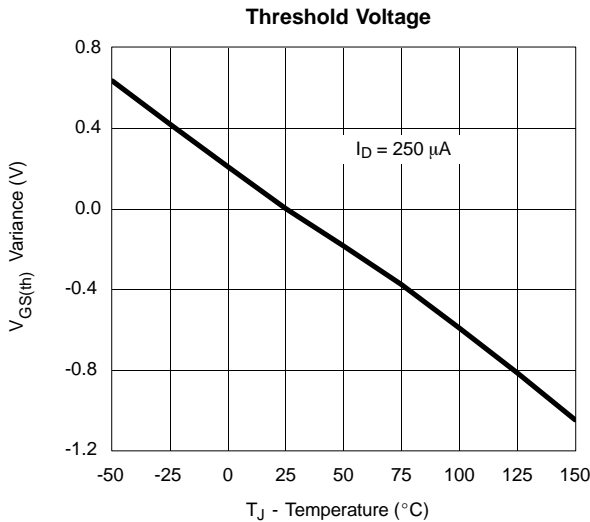


On-Resistance vs. Gate-to-Source Voltage





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