

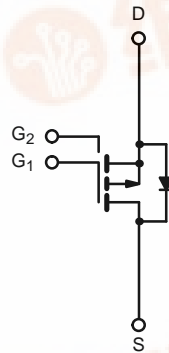
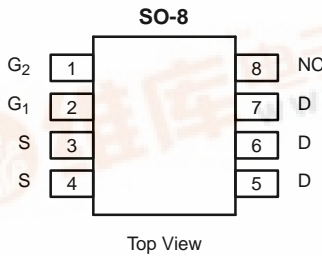


**Si4807DY**  
Vishay Siliconix

**P-Channel 30:1 Ratio Dual-Gate 30-V (D-S) MOSFET**

**TrenchFET<sup>®</sup>**  
Power MOSFETs

PRODUCT SUMMARY			
	$V_{DS}$ (V)	$r_{DS(ON)}$ ( $\Omega$ )	$I_D$ (A)
Gate 1	-30	0.035 @ $V_{GS} = -10$ V	$\pm 6$
		0.054 @ $V_{GS} = -4.5$ V	$\pm 4.8$
Gate 2		1.3 @ $V_{GS} = -10$ V	$\pm 0.9$
		2.2 @ $V_{GS} = -4.5$ V	$\pm 0.7$



P-Channel MOSFET

ABSOLUTE MAXIMUM RATINGS ( $T_A = 25^\circ\text{C}$ UNLESS OTHERWISE NOTED)					
Parameter		Symbol	Gate 1	Gate 2	Unit
Drain-Source Voltage		$V_{DS}$	-30		V
Gate-Source Voltage		$V_{GS}$	$\pm 20$		
Continuous Drain Current ( $T_J = 150^\circ\text{C}$ ) <sup>a</sup>	$T_A = 25^\circ\text{C}$	$I_D$	$\pm 6$	$\pm 0.9$	A
	$T_A = 70^\circ\text{C}$		$\pm 4.8$	$\pm 0.7$	
Pulsed Drain Current		$I_{DM}$	$\pm 30$	$\pm 1.5$	
Continuous Source Current (Diode Conduction) <sup>a</sup>		$I_S$	-1.25		
Maximum Power Dissipation <sup>a</sup>	$T_A = 25^\circ\text{C}$	$P_D$	2.3		W
	$T_A = 70^\circ\text{C}$		1.0		
Operating Junction and Storage Temperature Range		$T_J, T_{stg}$	-55 to 150		$^\circ\text{C}$

THERMAL RESISTANCE RATINGS			
Parameter	Symbol	Limit	Unit
Maximum Junction-to-Ambient <sup>a</sup>	$R_{thJA}$	55	$^\circ\text{C/W}$

Notes:  
a. Surface Mounted on FR4 Board,  $t \leq 10$  sec.

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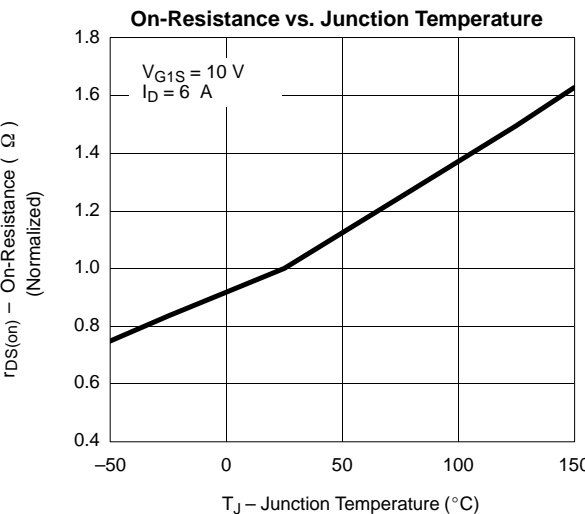
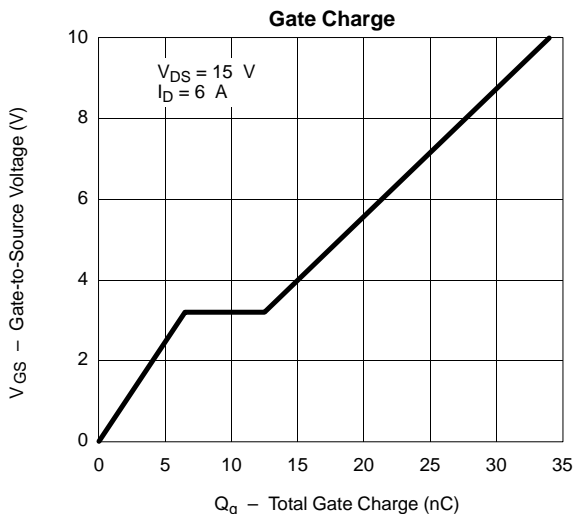
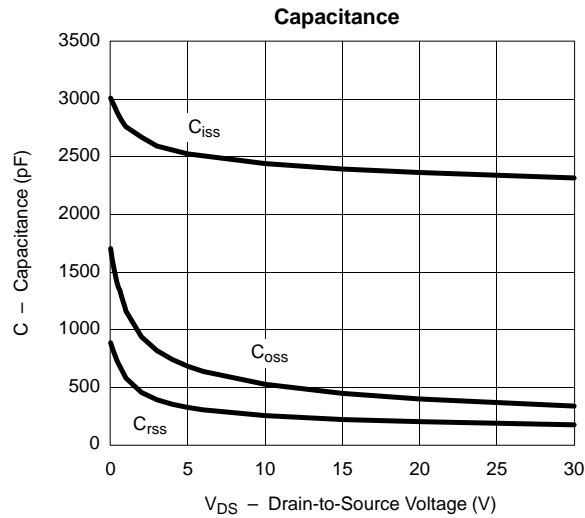
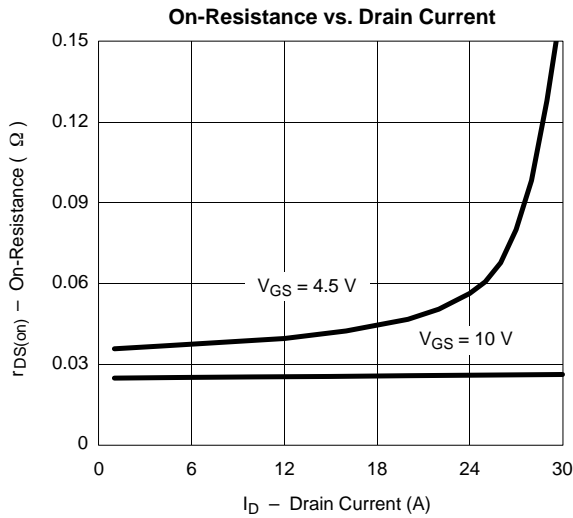
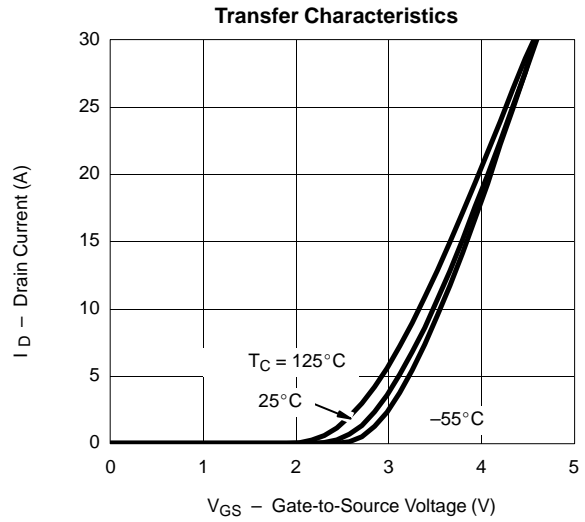
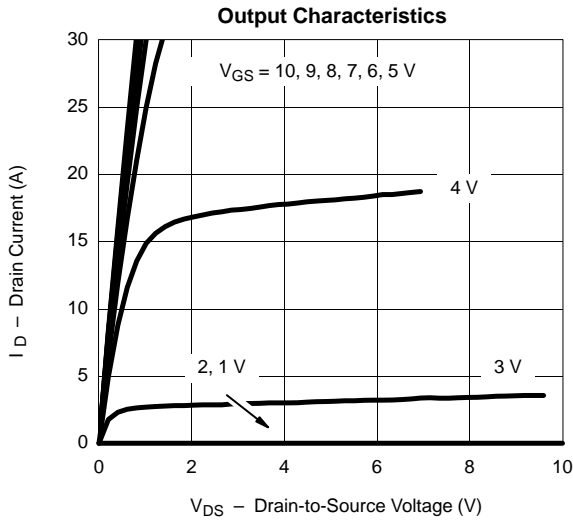
SPECIFICATIONS (T <sub>J</sub> = 25 °C UNLESS OTHERWISE NOTED)							
Parameter	Symbol	Test Condition	Min	Typ	Max	Unit	
<b>Static</b>							
Gate Threshold Voltage	V <sub>GS(th)</sub>	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = -250 μA	-1			V	
Gate-Body Leakage	I <sub>GSS</sub>	V <sub>DS</sub> = 0 V, V <sub>GS</sub> = ±20 V			±100	nA	
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	V <sub>DS</sub> = -30 V, V <sub>GS</sub> = 0 V			-1	μA	
		V <sub>DS</sub> = -30 V, V <sub>GS</sub> = 0 V, T <sub>J</sub> = 55 °C			-5		
On-State Drain Current <sup>a</sup>	I <sub>D(on)</sub>	(G <sub>1</sub> = G <sub>2</sub> ) V <sub>DS</sub> = -5 V, V <sub>GS</sub> = -10 V	-20			A	
Drain-Source On-State Resistance <sup>a</sup>	r <sub>DS1(on)</sub>	(G <sub>1</sub> = G <sub>2</sub> ) V <sub>GS</sub> = -10 V, I <sub>D</sub> = -6 A		0.028	0.035	Ω	
		(G <sub>1</sub> = G <sub>2</sub> ) V <sub>GS</sub> = -4.5 V, I <sub>D</sub> = -4.8 A		0.041	0.054		
	r <sub>DS2(on)</sub>	V <sub>G1S</sub> = 0 V, V <sub>G2S</sub> = -10 V, I <sub>D</sub> = -0.15 A		1.05	1.3		
		V <sub>G1S</sub> = 0 V, V <sub>G2S</sub> = -4.5 V, I <sub>D</sub> = -0.1 A		1.65	2.2		
Forward Transconductance <sup>a</sup>	g <sub>fs</sub>	V <sub>DS</sub> = -15 V, I <sub>D</sub> = -6 A		13		S	
Diode Forward Voltage <sup>a</sup>	V <sub>SD</sub>	I <sub>S</sub> = -1.25 A, V <sub>GS</sub> = 0 V		0.7	-1.1	V	
<b>Dynamic<sup>b</sup></b>							
Total Gate Charge	Q <sub>g</sub>	Gate 1 V <sub>DS</sub> = -15 V, V <sub>GS(1,2)</sub> = -10 V I <sub>D</sub> = -6 A  Gate 2 V <sub>DS</sub> = -15 V, V <sub>GS(1)</sub> = -0 V V <sub>GS(2)</sub> = -10 V, I <sub>D</sub> = -0.15 A	Gate 1		34	60	nC
			Gate 2		2.0	5	
Gate-Source Charge	Q <sub>gs</sub>		Gate 1		6.5		
			Gate 2		0.5		
Gate-Drain Charge	Q <sub>gd</sub>		Gate 1		6.0		
			Gate 2		0.2		
Turn-On Delay Time	t <sub>d(on)</sub>	V <sub>DD</sub> = -15 V, R <sub>L</sub> = 15 Ω I <sub>D</sub> ≅ -1 A, V <sub>GEN</sub> = -10 V, R <sub>G</sub> = 6 Ω		15	25	ns	
Rise Time	t <sub>r</sub>			11	20		
Turn-Off Delay Time	t <sub>d(off)</sub>			52	80		
Fall Time	t <sub>f</sub>			20	35		
Source-Drain Reverse Recovery Time	t <sub>rr</sub>	I <sub>F</sub> = -1.25 A, di/dt = -100 A/μs		30	60		

**Notes**

- a. Pulse test; pulse width ≤ 300 μs, duty cycle ≤ 2%.
- b. Guaranteed by design, not subject to production testing.

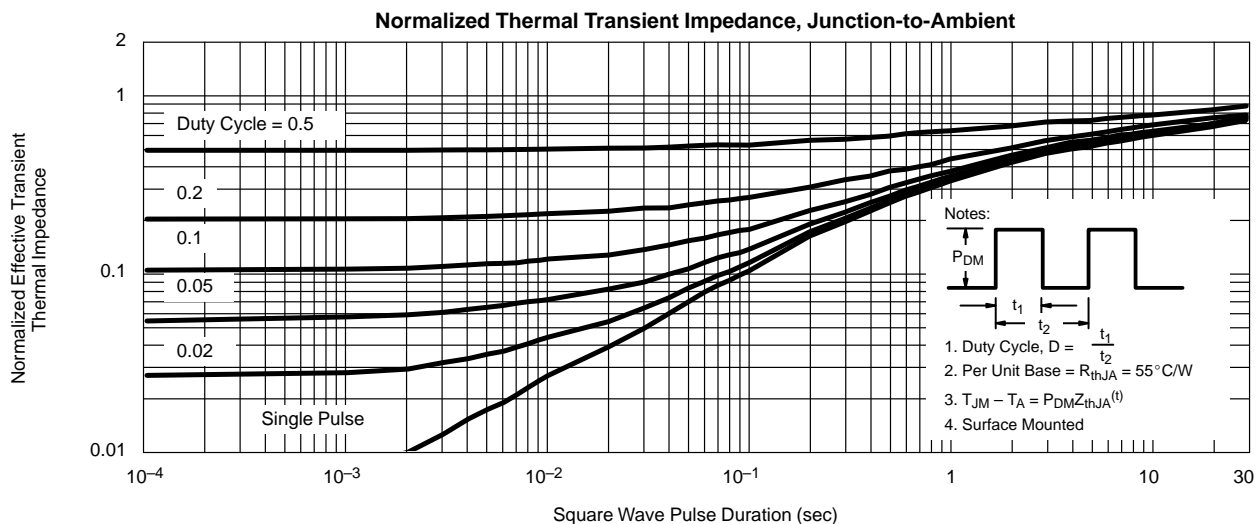
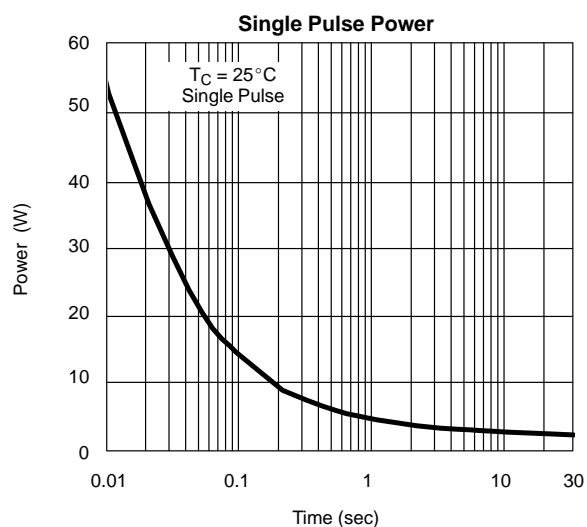
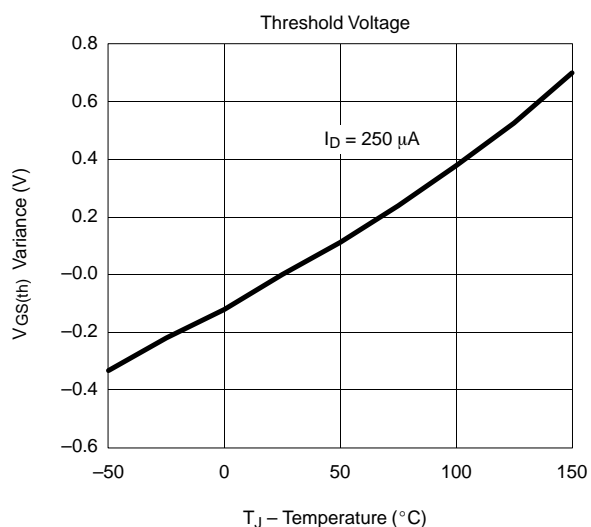
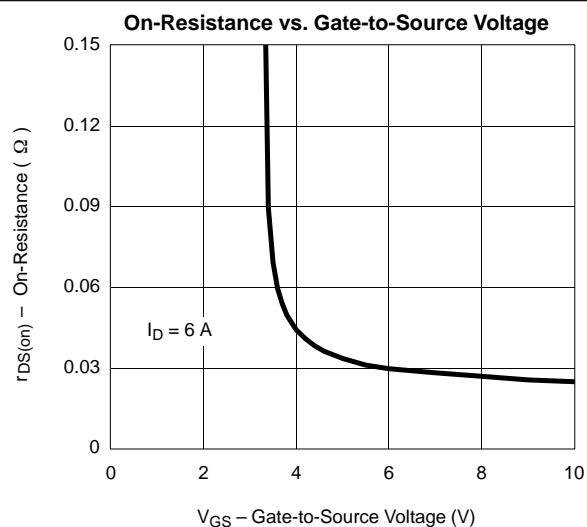
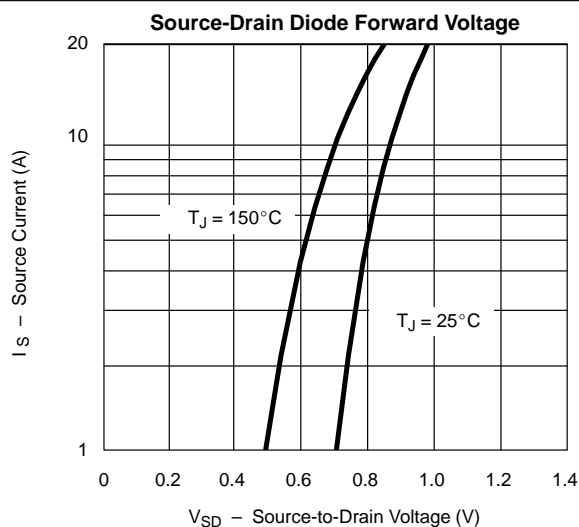


**TYPICAL CHARACTERISTICS ( $V_{G1} = V_{G2}$ , 25°C UNLESS NOTED)**





### TYPICAL CHARACTERISTICS ( $V_{G1} = V_{G2}$ , 25°C UNLESS NOTED)





**TYPICAL CHARACTERISTICS ( $V_{G1} = 0\text{ V}$ ,  $25^\circ\text{C}$  UNLESS NOTED)**

