



New Product

Si4933DY
Vishay Siliconix

Dual P-Channel 12-V (D-S) MOSFET

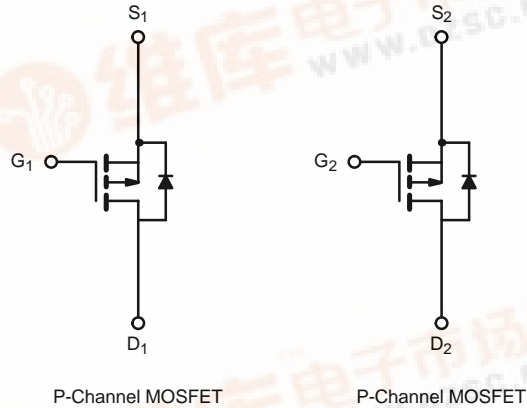
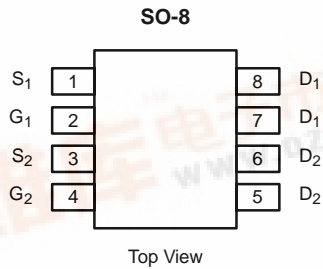
PRODUCT SUMMARY		
V_{DS} (V)	$r_{DS(on)}$ (Ω)	I_D (A)
-12	0.014 @ $V_{GS} = -4.5$ V	-9.8
	0.017 @ $V_{GS} = -2.5$ V	-8.9
	0.022 @ $V_{GS} = -1.8$ V	-7.8

FEATURES

- TrenchFET® Power MOSFET
- Advanced High Cell Density Process

APPLICATIONS

- Load Switching



ABSOLUTE MAXIMUM RATINGS ($T_A = 25^\circ\text{C}$ UNLESS OTHERWISE NOTED)				
Parameter	Symbol	10 secs	Steady State	Unit
Drain-Source Voltage	V_{DS}	-12		V
Gate-Source Voltage	V_{GS}	± 8		
Continuous Drain Current ($T_J = 150^\circ\text{C}$) ^a	I_D	$T_A = 25^\circ\text{C}$	-9.8	-7.4
		$T_A = 70^\circ\text{C}$	-7.8	-5.9
Pulsed Drain Current	I_{DM}	-30		A
continuous Source Current (Diode Conduction) ^a	I_S	-1.7	-0.9	
Maximum Power Dissipation ^a	P_D	$T_A = 25^\circ\text{C}$	2.0	1.1
		$T_A = 70^\circ\text{C}$	1.3	0.7
Operating Junction and Storage Temperature Range	T_J, T_{stg}	-55 to 150		$^\circ\text{C}$

THERMAL RESISTANCE RATINGS				
Parameter	Symbol	Typical	Maximum	Unit
Maximum Junction-to-Ambient ^a	R_{thJA}	$t \leq 10$ sec	45	62.5
		Steady State	85	110
Maximum Junction-to-Foot (Drain)	R_{thJF}	26	35	$^\circ\text{C/W}$

^a Surface Mounted on 1" x 1" FR4 Board.



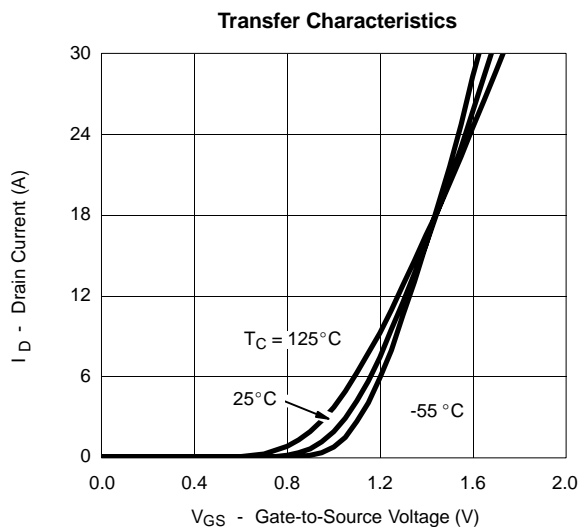
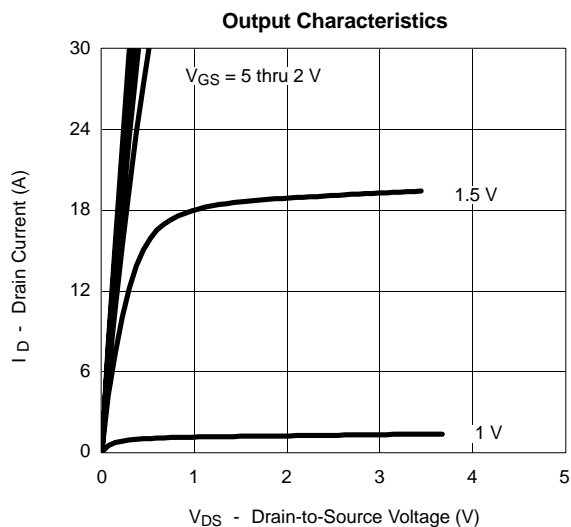
SPECIFICATIONS (T_J = 25 °C UNLESS OTHERWISE NOTED)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Static						
Gate Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = -500 μA	-0.40		-1.0	V
Gate-Body Leakage	I _{GSS}	V _{DS} = 0 V, V _{GS} = ±8 V			±100	nA
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = -9.6 V, V _{GS} = 0 V			-1	μA
		V _{DS} = -9.6 V, V _{GS} = 0 V, T _J = 55 °C			-5	
On-State Drain Current ^a	I _{D(on)}	V _{DS} = -5 V, V _{GS} = -4.5 V	-30			A
Drain-Source On-State Resistance ^a	r _{DS(on)}	V _{GS} = -4.5 V, I _D = -9.8 A		0.0115	0.014	Ω
		V _{GS} = -2.5 V, I _D = -8.9 A		0.014	0.017	
		V _{GS} = -1.8 V, I _D = -5.0 A		0.018	0.022	
Forward Transconductance ^a	g _{fs}	V _{DS} = -10 V, I _D = -9.8 A		40		S
Diode Forward Voltage ^a	V _{SD}	I _S = -1.7 A, V _{GS} = 0 V		-0.7	-1.2	V
Dynamic^b						
Total Gate Charge	Q _g	V _{DS} = 6 V, V _{GS} = -4.5 V, I _D = -9.8 A		46	70	nC
Gate-Source Charge	Q _{gs}			6.0		
Gate-Drain Charge	Q _{gd}			13		
Turn-On Delay Time	t _{d(on)}	V _{DD} = 6 V, R _L = 6 Ω I _D ≅ -1 A, V _{GEN} = -4.5 V, R _G = 6 Ω		35	55	ns
Rise Time	t _r			47	70	
Turn-Off Delay Time	t _{d(off)}			320	480	
Fall Time	t _f			260	390	
Source-Drain Reverse Recovery Time	t _{rr}		I _F = -1.7 A, di/dt = 100 A/μs		210	

Notes

- a. Pulse test; pulse width ≤ 300 μs, duty cycle ≤ 2%.
- b. Guaranteed by design, not subject to production testing.

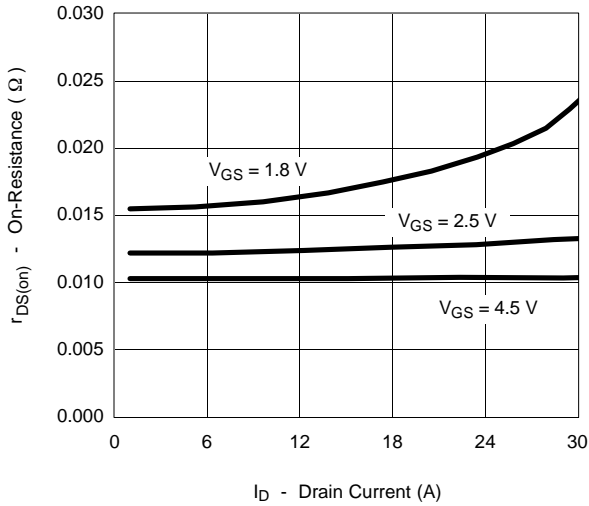
TYPICAL CHARACTERISTICS (25 °C UNLESS NOTED)



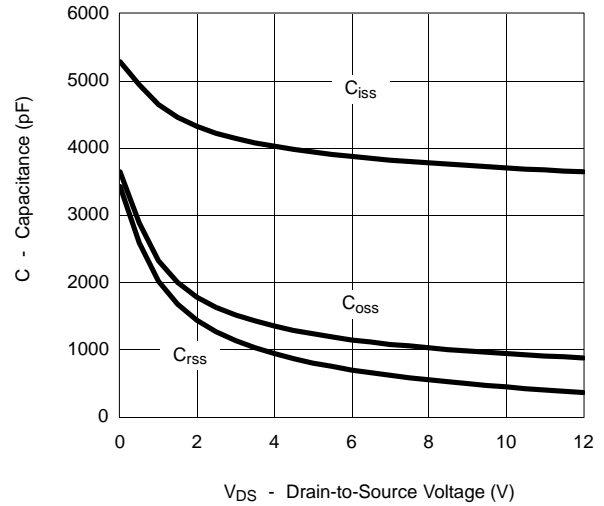


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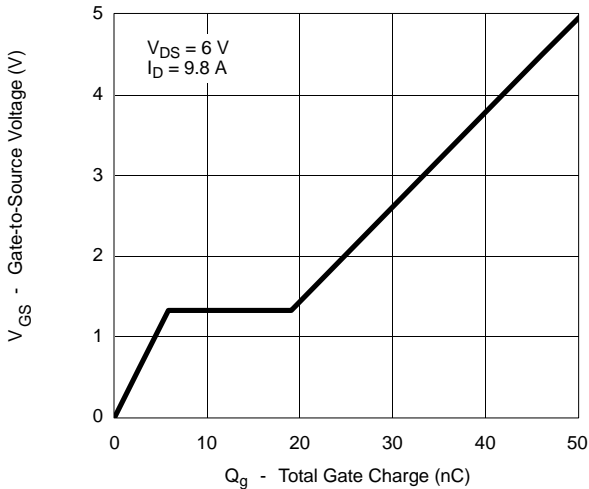
On-Resistance vs. Drain Current



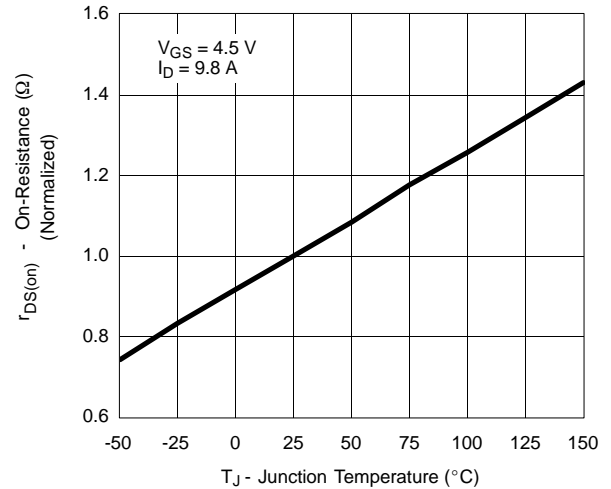
Capacitance



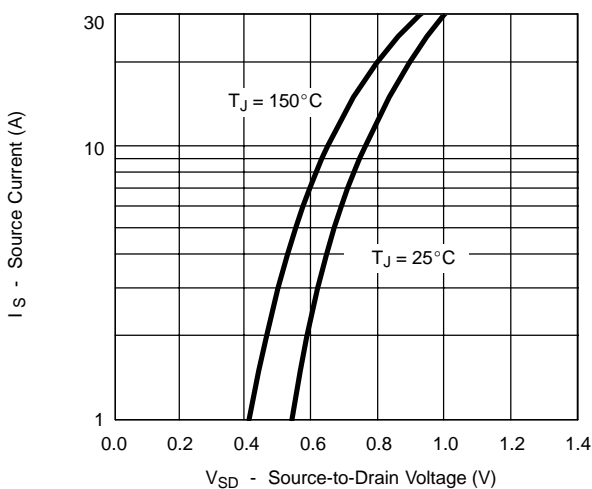
Gate Charge



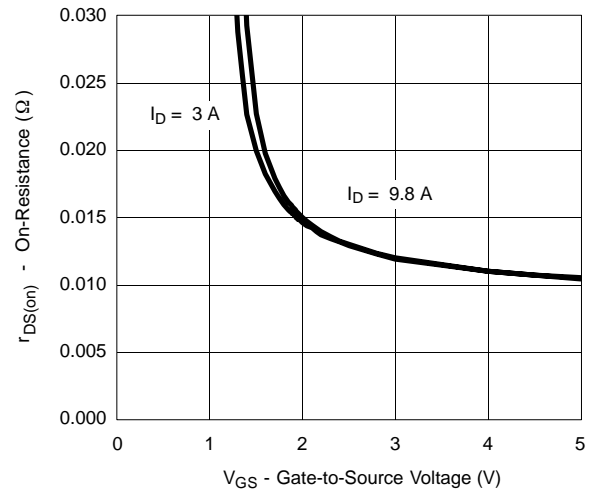
On-Resistance vs. Junction Temperature



Source-Drain Diode Forward Voltage

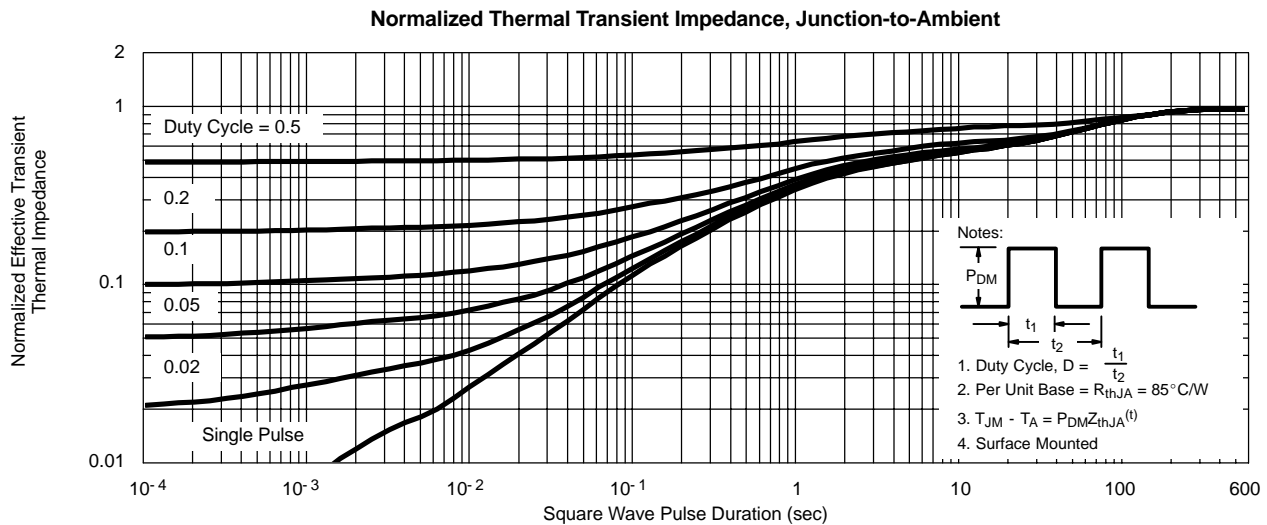
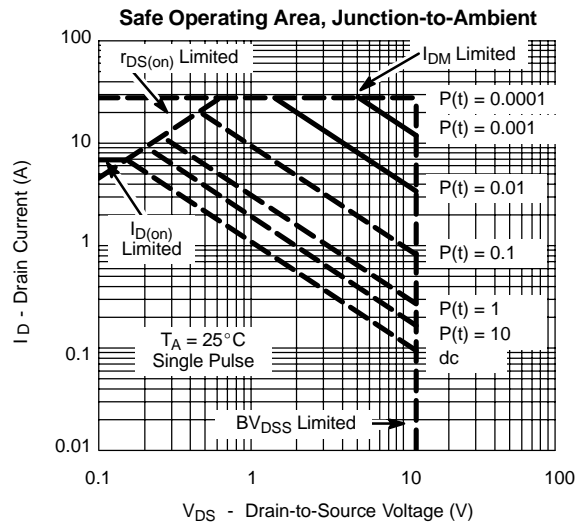
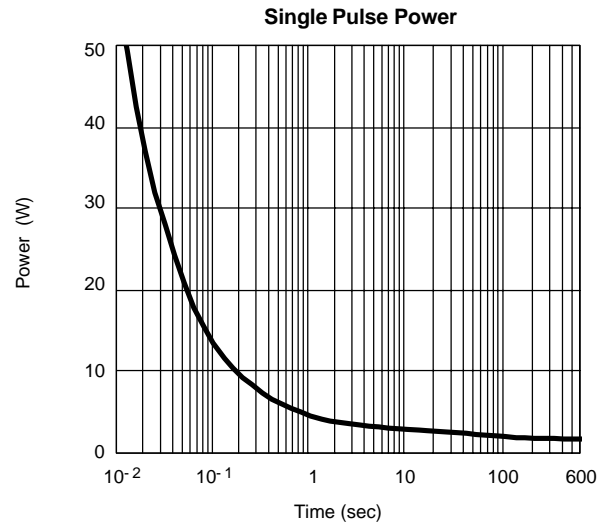
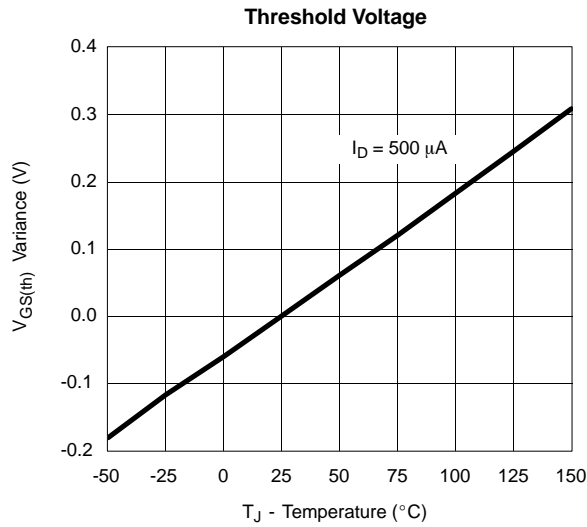


On-Resistance vs. Gate-to-Source Voltage





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