



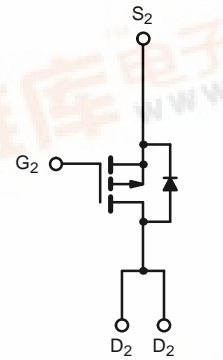
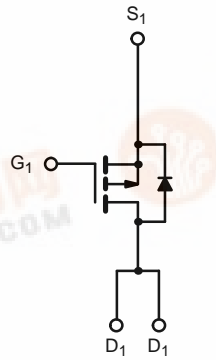
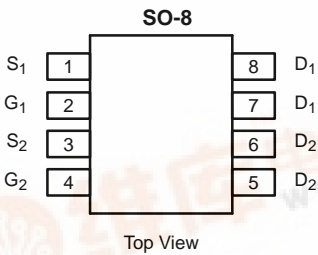
Si4948EY

Vishay Siliconix

Dual P-Channel 60-V (D-S), 175°C MOSFET

PRODUCT SUMMARY		
V_{DS} (V)	$r_{DS(on)}$ (Ω)	I_D (A)
-60	0.120 @ $V_{GS} = -10$ V	± 3.1
	0.150 @ $V_{GS} = -4.5$ V	± 2.8

175°C Rated
Maximum Junction Temperature
TrenchFET®
Power MOSFETs



ABSOLUTE MAXIMUM RATINGS ($T_A = 25^\circ\text{C}$ UNLESS OTHERWISE NOTED)			
Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V_{DS}	-60	V
Gate-Source Voltage	V_{GS}	± 20	
Continuous Drain Current ($T_J = 175^\circ\text{C}$) ^a	I_D	$T_A = 25^\circ\text{C}$	± 3.1
		$T_A = 70^\circ\text{C}$	± 2.6
Pulsed Drain Current	I_{DM}	± 30	A
Continuous Source Current (Diode Conduction) ^a	I_S	-2.0	
Maximum Power Dissipation ^a	P_D	$T_A = 25^\circ\text{C}$	2.4
		$T_A = 70^\circ\text{C}$	1.7
Operating Junction and Storage Temperature Range	T_J, T_{stg}	-55 to 175	$^\circ\text{C}$

THERMAL RESISTANCE RATINGS			
Parameter	Symbol	Limit	Unit
Maximum Junction-to-Ambient ^a	R_{thJA}	62.5	$^\circ\text{C/W}$

Notes:
a. Surface Mounted on FR4 Board, $t \leq 10$ sec.

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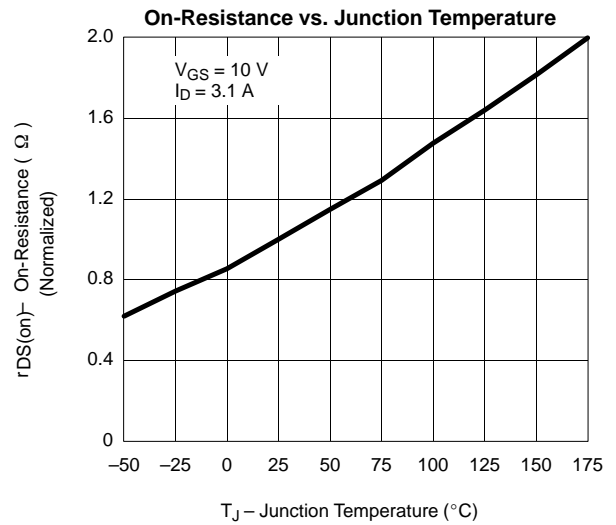
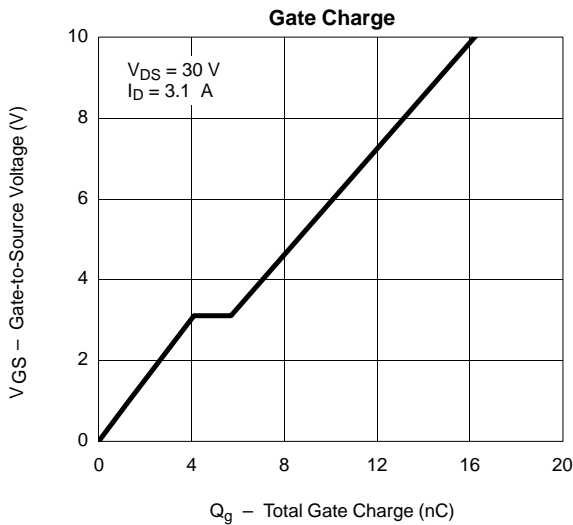
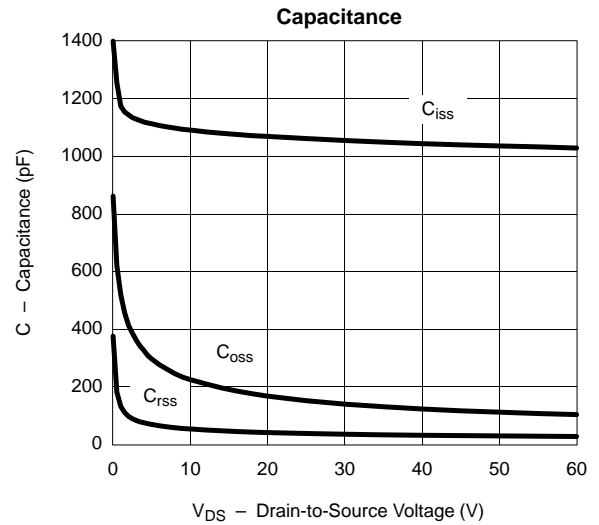
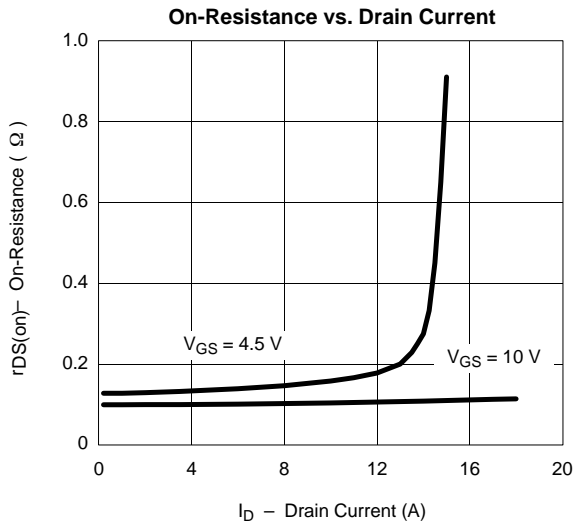
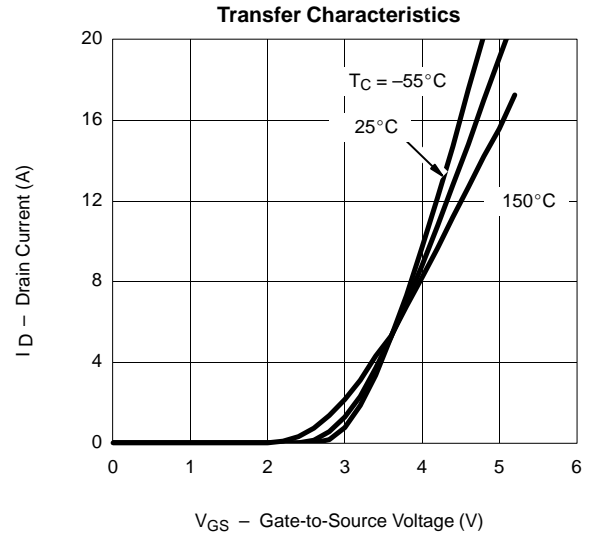
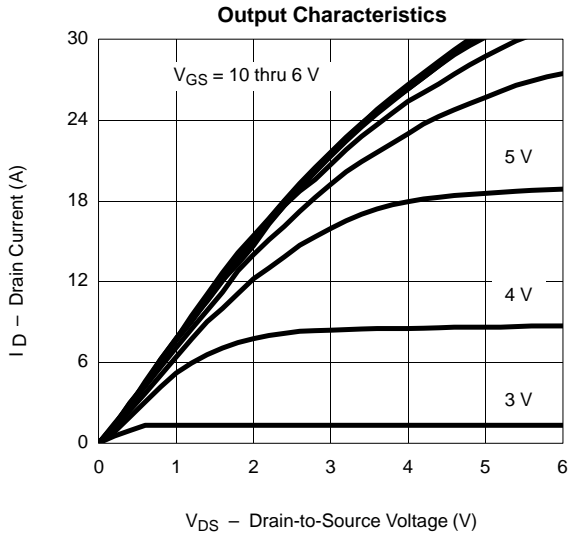
SPECIFICATIONS (T _J = 25 °C UNLESS OTHERWISE NOTED)						
Parameter	Symbol	Test Condition	Min	Typ ^a	Max	Unit
Static						
Gate Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = -250 μA	-1			V
Gate-Body Leakage	I _{GSS}	V _{DS} = 0 V, V _{GS} = ±20 V			±100	nA
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = -60 V, V _{GS} = 0 V			-2	μA
		V _{DS} = -60 V, V _{GS} = 0 V, T _J = 55 °C			-25	
On-State Drain Current ^b	I _{D(on)}	V _{DS} ≤ -5 V, V _{GS} = -10 V	-20			A
Drain-Source On-State Resistance ^b	r _{DS(on)}	V _{GS} = -10 V, I _D = -3.1 A		0.100	0.120	Ω
		V _{GS} = -4.5 V, I _D = -2.8 A		0.125	0.150	
Forward Transconductance ^b	g _{fs}	V _{DS} = -15 V, I _D = -3.1 A		7.5		S
Diode Forward Voltage ^b	V _{SD}	I _S = -2.0 A, V _{GS} = 0 V		-0.8	-1.2	V
Dynamic^a						
Total Gate Charge	Q _g	V _{DS} = -30 V, V _{GS} = -10 V, I _D = -3.1 A		16	25	nC
Gate-Source Charge	Q _{gs}			4		
Gate-Drain Charge	Q _{gd}			1.6		
Turn-On Delay Time	t _{d(on)}	V _{DD} = -30 V, R _L = 30 Ω I _D ≈ -1 A, V _{GEN} = -10 V, R _G = 6 Ω		8	15	ns
Rise Time	t _r			10	20	
Turn-Off Delay Time	t _{d(off)}			35	50	
Fall Time	t _f			12	25	
Source-Drain Reverse Recovery Time	t _{rr}	I _F = -2.0 A, di/dt = 100 A/μs		60	90	

Notes

- a. Guaranteed by design, not subject to production testing.
- b. Pulse test; pulse width ≤ 300 μs, duty cycle ≤ 2%.



TYPICAL CHARACTERISTICS (25°C UNLESS NOTED)





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