



January 2001

SI9426DY

Single N-Channel, 2.5V Specified MOSFET

General Description

This N-Channel 2.5V specified MOSFET is produced using Fairchild Semiconductor's high cell density DMOS technology process that has been especially tailored to minimize on-state resistance and yet maintain low gate charge for superior switching performance.

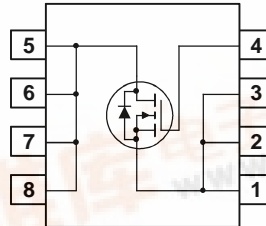
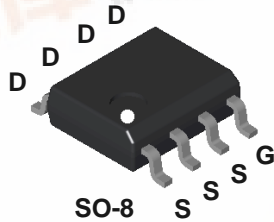
These devices have been designed to offer exceptional power dissipation in a very small footprint package.

Applications

- DC/DC converter
- Load switch

Features

- 10.5 A, 20 V. $R_{DS(ON)} = 13.5\text{ m}\Omega @ V_{GS} = 4.5\text{ V}$
 $R_{DS(ON)} = 16\text{ m}\Omega @ V_{GS} = 2.7\text{ V}$
- High cell density for extremely low $R_{DS(ON)}$
- High power and current handling capability in a widely used surface mount package



Absolute Maximum Ratings T_A=25°C unless otherwise noted

Symbol	Parameter	Ratings	Units
V _{DSS}	Drain-Source Voltage	20	V
V _{GSS}	Gate-Source Voltage	±8	V
I _D	Drain Current – Continuous (Note 1a)	10.5	A
	– Pulsed	30	
P _D	Power Dissipation for Single Operation (Note 1a)	2.5	W
	(Note 1b)	1.2	
	(Note 1c)	1	
T _J , T _{STG}	Operating and Storage Junction Temperature Range	-55 to +150	°C

Thermal Characteristics

R _{θJA}	Thermal Resistance, Junction-to-Ambient (Note 1a)	50	°C/W
R _{θJC}	Thermal Resistance, Junction-to-Case (Note 1)	25	°C/W

Package Marking and Ordering Information

Device Marking	Device	Reel Size	Tape width	Quantity
9426	SI9426DY	13"	12mm	2500 units



Electrical Characteristics

$T_A = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
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Off Characteristics

BV_{DSS}	Drain-Source Breakdown Voltage	$V_{GS} = 0\text{ V}, I_D = 250\mu\text{A}$	20			V
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = 16\text{ V}, V_{GS} = 0\text{ V}$ $V_{DS} = 16\text{ V}, V_{GS} = 0\text{ V}, T_J = 55^\circ\text{C}$			1 10	μA
I_{GSSF}	Gate-Body Leakage, Forward	$V_{GS} = 8\text{ V}, V_{DS} = 0\text{ V}$			100	nA
I_{GSSR}	Gate-Body Leakage, Reverse	$V_{GS} = -8\text{ V}, V_{DS} = 0\text{ V}$			-100	nA

On Characteristics (Note 2)

$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_D = 250\mu\text{A}$ $V_{DS} = V_{GS}, I_D = 250\mu\text{A}, T_J = 125^\circ\text{C}$	0.4 0.3	0.6 0.5	1.5 0.8	V
$R_{DS(on)}$	Static Drain-Source On-Resistance	$V_{GS} = 4.5\text{ V}, I_D = 10.5\text{ A}$ $V_{GS} = 4.5\text{ V}, I_D = 10.5\text{ A}, T_J = 125^\circ\text{C}$ $V_{GS} = 2.7\text{ V}, I_D = 10\text{ A}$		12 17 14	13.5 24 16	m Ω
$I_{D(on)}$	On-State Drain Current	$V_{GS} = 4.5\text{ V}, V_{DS} = 5\text{ V}$	30			A
g_{FS}	Forward Transconductance	$V_{DS} = 5\text{ V}, I_D = 10.5\text{ A}$		43		S

Dynamic Characteristics

C_{iss}	Input Capacitance	$V_{DS} = 10\text{ V}, V_{GS} = 0\text{ V},$ $f = 1.0\text{ MHz}$		2150		pF
C_{oss}	Output Capacitance			890		pF
C_{riss}	Reverse Transfer Capacitance			165		pF

Switching Characteristics (Note 2)

$t_{d(on)}$	Turn-On Delay Time	$V_{DS} = 5\text{ V}, I_D = 1\text{ A},$ $V_{GS} = 4.5\text{ V}, R_{GEN} = 6\Omega$		11	30	ns
t_r	Turn-On Rise Time			26	55	ns
$t_{d(off)}$	Turn-Off Delay Time			145	220	ns
t_f	Turn-Off Fall Time			40	100	ns
Q_g	Total Gate Charge	$V_{DS} = 10\text{ V}, I_D = 10.5\text{ A},$ $V_{GS} = 4.5\text{ V}$		43	60	nC
Q_{gs}	Gate-Source Charge			7		nC
Q_{gd}	Gate-Drain Charge			8		nC

Drain-Source Diode Characteristics and Maximum Ratings

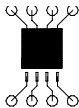
I_S	Maximum Continuous Drain-Source Diode Forward Current			2.1	A	
V_{SD}	Drain-Source Diode Forward Voltage	$V_{GS} = 0\text{ V}, I_S = 2.1\text{ A}$ (Note 2)		0.6	1.2	V

Notes:

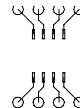
1. $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.



a) 50°C/W when mounted on a 1 in^2 pad of 2 oz copper



b) 105°C/W when mounted on a $.04\text{ in}^2$ pad of 2 oz copper



c) 125°C/W when mounted on a minimum pad.

Scale 1 : 1 on letter size paper

2. Pulse Test: Pulse Width < $300\mu\text{s}$, Duty Cycle < 2.0%

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