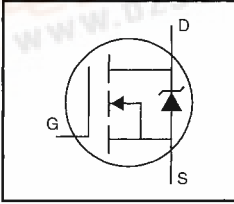


HEXFET® Power MOSFET

- Isolated Package
- High Voltage Isolation= 2.5KV RMS ⑤
- Sink to Lead Creepage Dist.= 4.8mm
- Dynamic dv/dt Rating
- Low Thermal Resistance

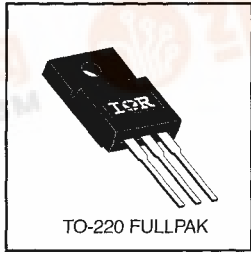


$V_{DSS} = 600V$
$R_{DS(on)} = 4.4\Omega$
$I_D = 1.7A$

**Description**

Third Generation HEXFETs from International Rectifier provide the designer with the best combination of fast switching, ruggedized device design, low on-resistance and cost-effectiveness.

The TO-220 Fullpak eliminates the need for additional insulating hardware in commercial-industrial applications. The moulding compound used provides a high isolation capability and a low thermal resistance between the tab and external heatsink. This isolation is equivalent to using a 100 micron mica barrier with standard TO-220 product. The Fullpak is mounted to a heatsink using a single clip or by a single screw fixing.



DATA SHEETS

**Absolute Maximum Ratings**

	Parameter	Max.	Units
$I_D @ T_C = 25^\circ C$	Continuous Drain Current, $V_{GS} @ 10 V$	1.7	A
$I_D @ T_C = 100^\circ C$	Continuous Drain Current, $V_{GS} @ 10 V$	1.1	
$I_{DM}$	Pulsed Drain Current ①	6.8	
$P_D @ T_C = 25^\circ C$	Power Dissipation	30	W
	Linear Derating Factor	0.24	W/°C
$V_{GS}$	Gate-to-Source Voltage	$\pm 20$	V
$E_{AS}$	Single Pulse Avalanche Energy ②	84	mJ
$I_{AR}$	Avalanche Current ①	1.7	A
$E_{AR}$	Repetitive Avalanche Energy ①	3.0	mJ
dv/dt	Peak Diode Recovery dv/dt ③	3.0	V/ns
$T_J$	Operating Junction and	-55 to +150	°C
$T_{STG}$	Storage Temperature Range		
	Soldering Temperature, for 10 seconds		
	Mounting Torque, 6-32 or M3 screw	10 lbf·in (1.1 N·m)	

**Thermal Resistance**


	Parameter	Min.	Typ.	Max.	Units
$R_{JC}$	Junction-to-Case	—	—	4.1	°C/W
$R_{JA}$	Junction-to-Ambient	—	—	65	




# IRFIB20G



## Electrical Characteristics @ $T_J = 25^\circ\text{C}$ (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Test Conditions
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	600	—	—	V	$V_{GS}=0V, I_D=250\mu A$
$\Delta V_{(BR)DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	—	0.88	—	V/°C	Reference to $25^\circ\text{C}, I_D=1\text{mA}$
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	—	—	4.4	$\Omega$	$V_{GS}=10V, I_D=1.0A$ ④
$V_{GS(th)}$	Gate Threshold Voltage	2.0	—	4.0	V	$V_{DS}=V_{GS}, I_D=250\mu A$
$g_{fs}$	Forward Transconductance	1.4	—	—	S	$V_{DS}=50V, I_D=1.0A$ ④
$I_{DSS}$	Drain-to-Source Leakage Current	—	—	100	$\mu A$	$V_{DS}=600V, V_{GS}=0V$
		—	—	500		$V_{DS}=480V, V_{GS}=0V, T_J=125^\circ\text{C}$
$I_{GSS}$	Gate-to-Source Forward Leakage	—	—	100	nA	$V_{GS}=20V$
	Gate-to-Source Reverse Leakage	—	—	-100		$V_{GS}=-20V$
$Q_g$	Total Gate Charge	—	—	18	nC	$I_D=2.0A$
$Q_{gs}$	Gate-to-Source Charge	—	—	3.0		$V_{DS}=360V$
$Q_{gd}$	Gate-to-Drain ("Miller") Charge	—	—	8.9		$V_{GS}=10V$ See Fig. 6 and 13 ④
$t_{d(on)}$	Turn-On Delay Time	—	10	—		$V_{DD}=300V$
$t_r$	Rise Time	—	23	—	ns	$I_D=2.0A$
$t_{d(off)}$	Turn-Off Delay Time	—	30	—		$R_G=18\Omega$
$t_f$	Fall Time	—	25	—		$R_D=150\Omega$ See Figure 10 ④
$L_D$	Internal Drain Inductance	—	4.5	—	nH	Between lead, 6 mm (0.25in.) from package and center of die contact
$L_S$	Internal Source Inductance	—	7.5	—		
$C_{iss}$	Input Capacitance	—	350	—	pF	$V_{GS}=0V$
$C_{oss}$	Output Capacitance	—	48	—		$V_{DS}=25V$
$C_{rss}$	Reverse Transfer Capacitance	—	8.6	—		$f=1.0\text{MHz}$ See Figure 5
$C$	Drain to Sink Capacitance	—	12	—		$f=1.0\text{MHz}$

## Source-Drain Ratings and Characteristics

	Parameter	Min.	Typ.	Max.	Units	Test Conditions
$I_S$	Continuous Source Current (Body Diode)	—	—	1.7	A	MOSFET symbol showing the integral reverse p-n junction diode. 
$I_{SM}$	Pulsed Source Current (Body Diode) ①	—	—	6.8		
$V_{SD}$	Diode Forward Voltage	—	—	1.6	V	$T_J=25^\circ\text{C}, I_S=1.7A, V_{GS}=0V$ ④
$t_{rr}$	Reverse Recovery Time	—	290	580	ns	$T_J=25^\circ\text{C}, I_F=2.0A$
$Q_{rr}$	Reverse Recovery Charge	—	0.65	1.3	$\mu C$	$di/dt=100A/\mu s$ ④
$t_{on}$	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by $L_S+L_D$ )				

Notes:

① Repetitive rating; pulse width limited by max. junction temperature (See Figure 11)

②  $I_{SD} \leq 2.2A, di/dt \leq 40A/\mu s, V_{DD} \leq V_{(BR)DSS}, T_J \leq 150^\circ\text{C}$

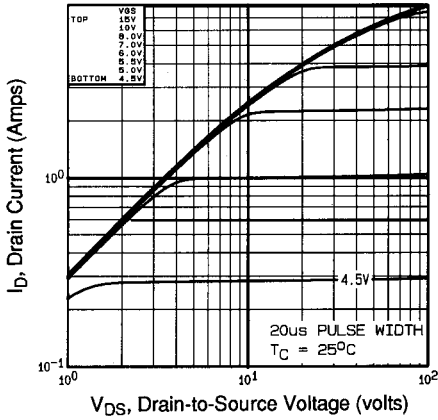
③  $t=60s, f=60\text{Hz}$

④  $V_{DD}=50V, \text{starting } T_J=25^\circ\text{C}, L=53\text{mH}$   
 $R_G=25\Omega, I_{AS}=1.7A$  (See Figure 12)

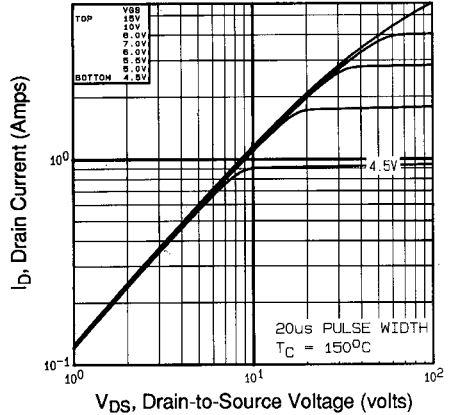
⑤ Pulse width  $\leq 300 \mu s$ ; duty cycle  $\leq 2\%$ .



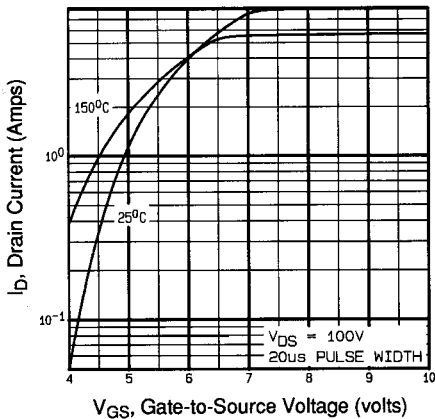
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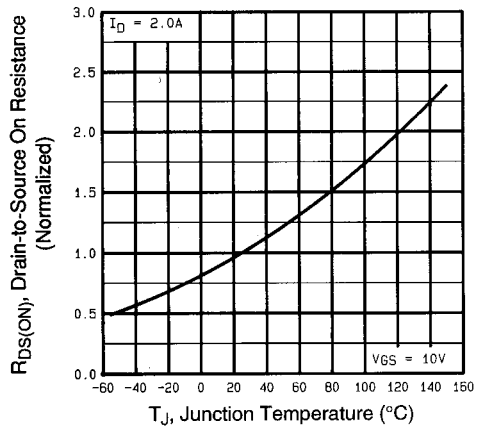
**Fig 1.** Typical Output Characteristics,  
 $T_C=25^\circ\text{C}$



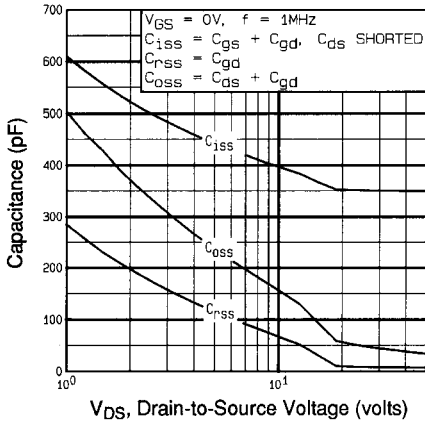
**Fig 2.** Typical Output Characteristics,  
 $T_C=150^\circ\text{C}$



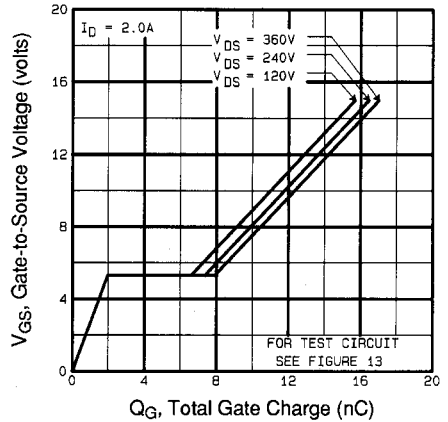
**Fig 3.** Typical Transfer Characteristics



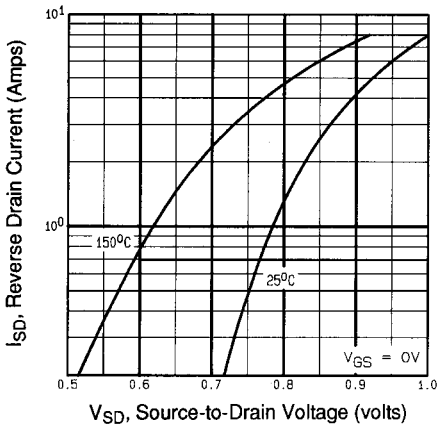
**Fig 4.** Normalized On-Resistance  
Vs. Temperature



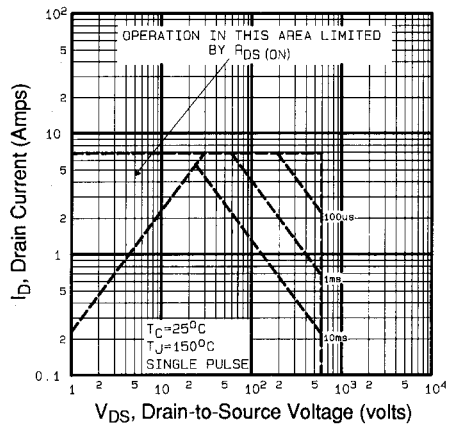
**Fig 5.** Typical Capacitance Vs. Drain-to-Source Voltage



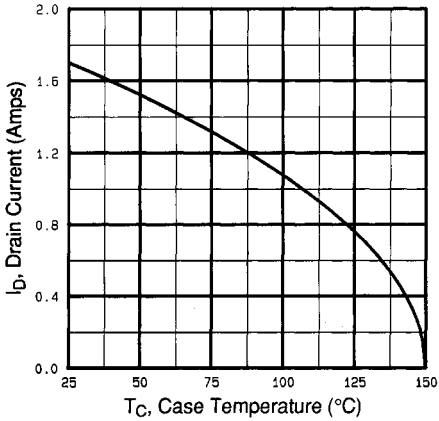
**Fig 6.** Typical Gate Charge Vs. Gate-to-Source Voltage



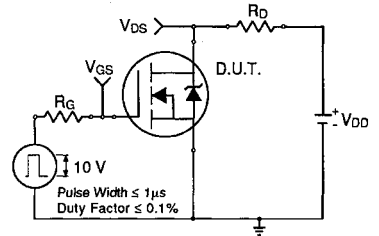
**Fig 7.** Typical Source-Drain Diode Forward Voltage



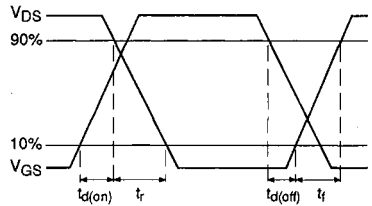
**Fig 8.** Maximum Safe Operating Area



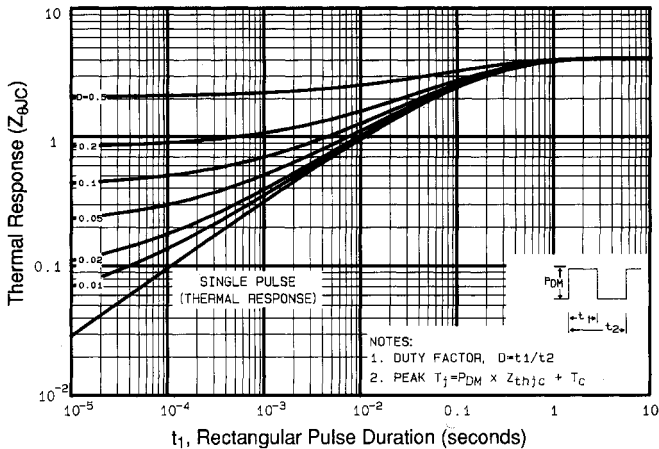
**Fig 9.** Maximum Drain Current Vs. Case Temperature



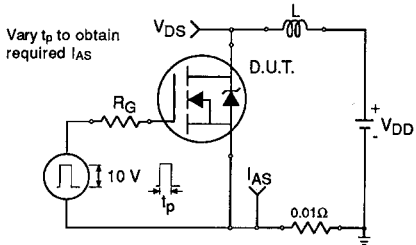
**Fig 10a.** Switching Time Test Circuit



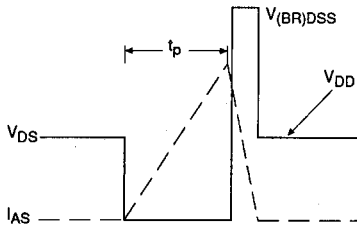
**Fig 10b.** Switching Time Waveforms



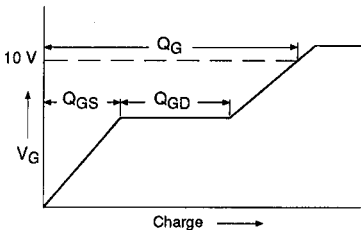
**Fig 11.** Maximum Effective Transient Thermal Impedance, Junction-to-Case



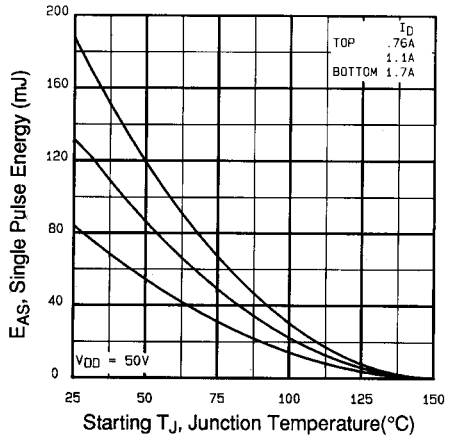
**Fig 12a.** Unclamped Inductive Test Circuit



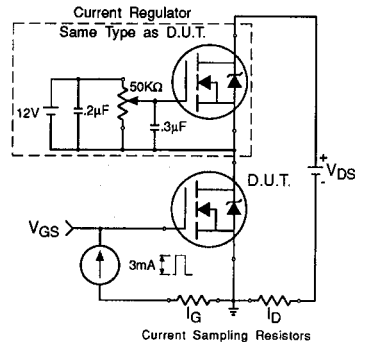
**Fig 12b.** Unclamped Inductive Waveforms



**Fig 13a.** Basic Gate Charge Waveform



**Fig 12c.** Maximum Avalanche Energy Vs. Drain Current



**Fig 13b.** Gate Charge Test Circuit

**Appendix A:** Figure 14, Peak Diode Recovery  $dv/dt$  Test Circuit – See page 1505

**Appendix B:** Package Outline Mechanical Drawing – See page 1510

**Appendix C:** Part Marking Information – See page 1517