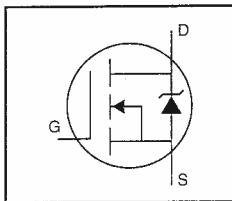


HEXFET® Power MOSFET

- Isolated Package
- High Voltage Isolation= 2.5KV RMS ⑤
- Sink to Lead Creepage Dist.= 4.8mm
- Dynamic dv/dt Rating
- Low Thermal Resistance



$$V_{DSS} = 600V$$

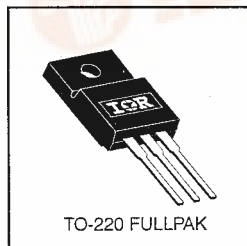
$$R_{DS(on)} = 1.2\Omega$$

$$I_D = 3.5A$$

Description

Third Generation HEXFETs from International Rectifier provide the designer with the best combination of fast switching, ruggedized device design, low on-resistance and cost-effectiveness.

The TO-220 Fullpak eliminates the need for additional insulating hardware in commercial-industrial applications. The moulding compound used provides a high isolation capability and a low thermal resistance between the tab and external heatsink. This isolation is equivalent to using a 100 micron mica barrier with standard TO-220 product. The Fullpak is mounted to a heatsink using a single clip or by a single screw fixing.



Absolute Maximum Ratings

	Parameter	Max.	Units
$I_D @ T_C = 25^\circ C$	Continuous Drain Current, $V_{GS} @ 10 V$	3.5	A
$I_D @ T_C = 100^\circ C$	Continuous Drain Current, $V_{GS} @ 10 V$	2.2	
$I_{DM}$	Pulsed Drain Current ①	14	
$P_D @ T_C = 25^\circ C$	Power Dissipation	40	W
	Linear Derating Factor	0.32	W/°C
$V_{GS}$	Gate-to-Source Voltage	±20	V
$E_{AS}$	Single Pulse Avalanche Energy ②	320	mJ
$I_{AR}$	Avalanche Current ①	3.5	A
$E_{AR}$	Repetitive Avalanche Energy ①	4.0	mJ
dv/dt	Peak Diode Recovery dv/dt ③	3.0	V/ns
$T_J$	Operating Junction and	-55 to +150	°C
$T_{STG}$	Storage Temperature Range		
	Soldering Temperature, for 10 seconds		
	Mounting Torque, 6-32 or M3 screw	10 lbf·in (1:1 N·m)	

Thermal Resistance

	Parameter	Min.	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case	—	—	3.1	°C/W
$R_{\theta JA}$	Junction-to-Ambient	—	—	65	



# IRFIBC40GLC



## Electrical Characteristics @ T<sub>J</sub> = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Test Conditions
V <sub>(BR)DSS</sub>	Drain-to-Source Breakdown Voltage	600	—	—	V	V <sub>GS</sub> =0V, I <sub>D</sub> =250μA
ΔV <sub>(BR)DSS</sub> /ΔT <sub>J</sub>	Breakdown Voltage Temp. Coefficient	—	0.70	—	V/°C	Reference to 25°C, I <sub>D</sub> =1mA
R <sub>DS(on)</sub>	Static Drain-to-Source On-Resistance	—	—	1.2	Ω	V <sub>GS</sub> =10V, I <sub>D</sub> =2.1A ③ V <sub>GS</sub> =V, I <sub>D</sub> =A ④
V <sub>GS(th)</sub>	Gate Threshold Voltage	2.0	—	4.0	V	V <sub>DS</sub> =V <sub>GS</sub> , I <sub>D</sub> =250μA
g <sub>fs</sub>	Forward Transconductance	3.7	—	—	S	V <sub>DS</sub> =100V, I <sub>D</sub> =3.7A ④
I <sub>DSS</sub>	Drain-to-Source Leakage Current	—	—	25	μA	V <sub>DS</sub> =600V, V <sub>GS</sub> =0V
		—	—	250	μA	V <sub>DS</sub> =480V, V <sub>GS</sub> =0V, T <sub>J</sub> =125°C
I <sub>GSS</sub>	Gate-to-Source Forward Leakage	—	—	100	nA	V <sub>GS</sub> =20V
	Gate-to-Source Reverse Leakage	—	—	-100	nA	V <sub>GS</sub> =-20V
Q <sub>g</sub>	Total Gate Charge	—	—	39	nC	I <sub>D</sub> =6.2A
Q <sub>gs</sub>	Gate-to-Source Charge	—	—	10	nC	V <sub>DS</sub> =360V
Q <sub>gd</sub>	Gate-to-Drain ("Miller") Charge	—	—	19	nC	V <sub>GS</sub> =10V See Fig. 6 and 13 ④
t <sub>d(on)</sub>	Turn-On Delay Time	—	12	—	ns	V <sub>DD</sub> =300V
t <sub>r</sub>	Rise Time	—	20	—		I <sub>D</sub> =6.2A
t <sub>d(off)</sub>	Turn-Off Delay Time	—	27	—		R <sub>G</sub> =9.1Ω
t <sub>f</sub>	Fall Time	—	17	—		R <sub>D</sub> =47Ω See Figure 10 ④
L <sub>D</sub>	Internal Drain Inductance	—	4.5	—	nH	Between lead, 6 mm (0.25in.) from package and center of die contact
L <sub>S</sub>	Internal Source Inductance	—	7.5	—		
C <sub>iss</sub>	Input Capacitance	—	1100	—	pF	V <sub>GS</sub> =0V
C <sub>oss</sub>	Output Capacitance	—	140	—		V <sub>DS</sub> =25V
C <sub>rss</sub>	Reverse Transfer Capacitance	—	15	—		f=1.0MHz See Figure 5
C	Drain to Sink Capacitance	—	12	—	pF	f=1.0MHz



## Source-Drain Ratings and Characteristics

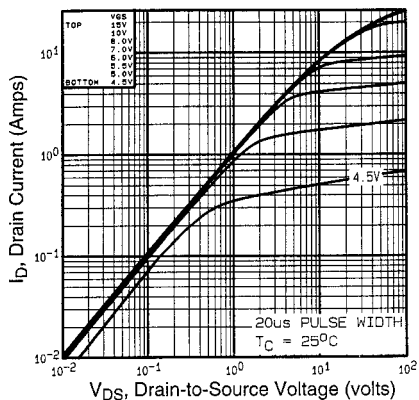
	Parameter	Min.	Typ.	Max.	Units	Test Conditions
I <sub>S</sub>	Continuous Source Current (Body Diode)	—	—	3.5	A	MOSFET symbol showing the integral reverse p-n junction diode.
I <sub>SM</sub>	Pulsed Source Current (Body Diode) ①	—	—	14		
V <sub>SD</sub>	Diode Forward Voltage	—	—	1.5	V	T <sub>J</sub> =25°C, I <sub>S</sub> =3.5A, V <sub>GS</sub> =0V ④
t <sub>rr</sub>	Reverse Recovery Time	—	440	660	ns	T <sub>J</sub> =25°C, I <sub>F</sub> =6.2A
Q <sub>rr</sub>	Reverse Recovery Charge	—	2.1	3.2	μC	di/dt=100A/μs ④
t <sub>on</sub>	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by L <sub>S</sub> +L <sub>D</sub> )				

### Notes:

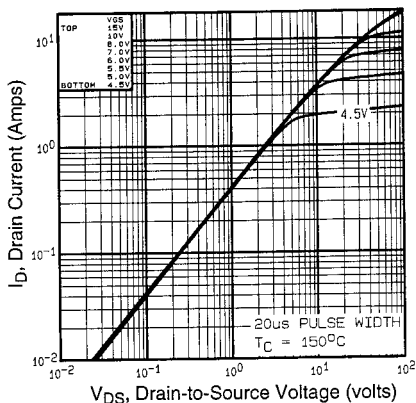
- ① Repetitive rating; pulse width limited by max. junction temperature (See Figure 11)
- ② V<sub>DD</sub>=50V, starting T<sub>J</sub>=25°C, L=12μH R<sub>G</sub>=25Ω, I<sub>AS</sub>=3.5A (See Figure 12)
- ③ I<sub>SD</sub>≤6.2A, di/dt≤80A/μs, V<sub>DD</sub>≤V<sub>(BR)DSS</sub>, T<sub>J</sub>≤150°C
- ④ Pulse width ≤ 300 μs; duty cycle ≤2%
- ⑤ t=60s, f=60Hz



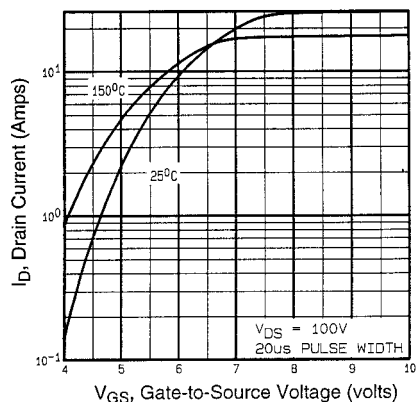
# IRFIBC40GLC



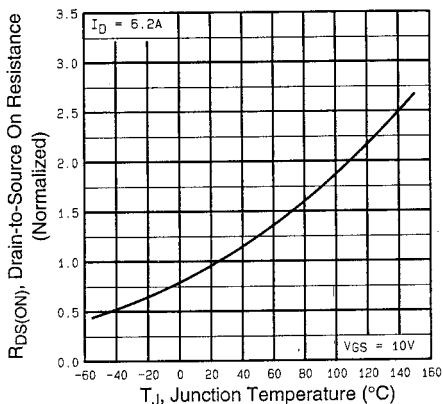
**Fig 1.** Typical Output Characteristics,  
 $T_C=25^\circ\text{C}$



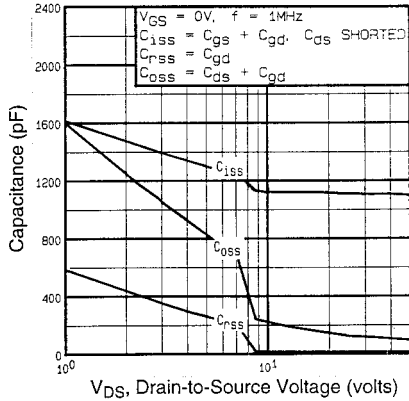
**Fig 2.** Typical Output Characteristics,  
 $T_C=150^\circ\text{C}$



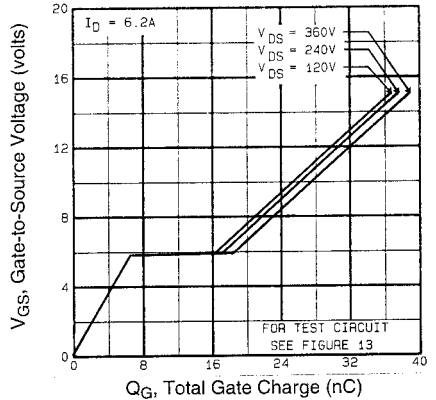
**Fig 3.** Typical Transfer Characteristics



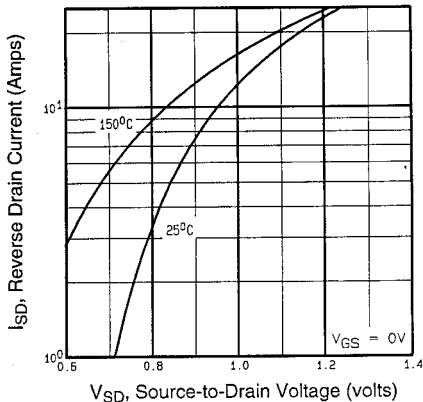
**Fig 4.** Normalized On-Resistance  
Vs. Temperature



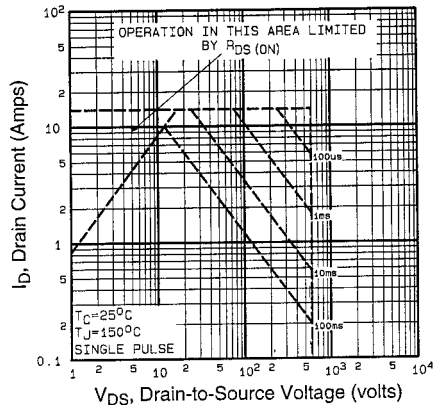
**Fig 5.** Typical Capacitance Vs. Drain-to-Source Voltage



**Fig 6.** Typical Gate Charge Vs. Gate-to-Source Voltage



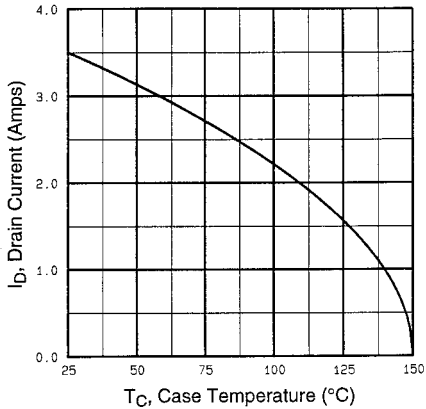
**Fig 7.** Typical Source-Drain Diode Forward Voltage



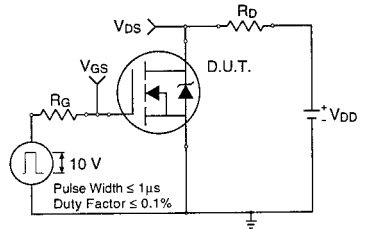
**Fig 8.** Maximum Safe Operating Area



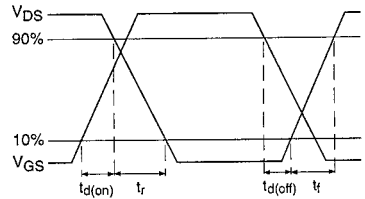
# IRFIBC40GLC



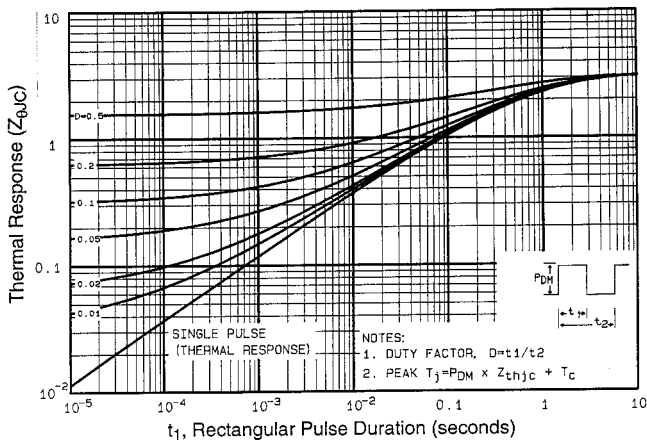
**Fig 9.** Maximum Drain Current Vs. Case Temperature



**Fig 10a.** Switching Time Test Circuit

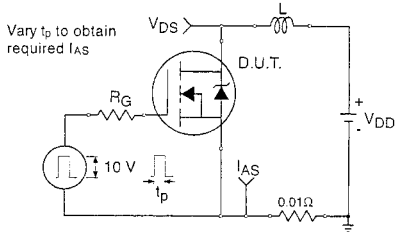


**Fig 10b.** Switching Time Waveforms

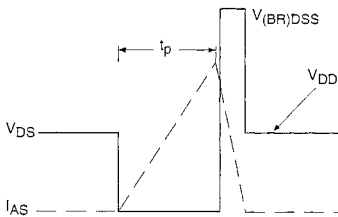


**Fig 11.** Maximum Effective Transient Thermal Impedance, Junction-to-Case

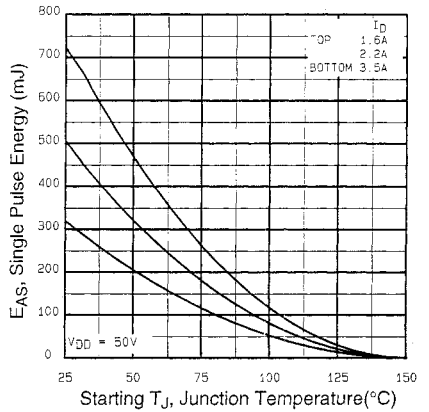
# IRFIBC40GLC



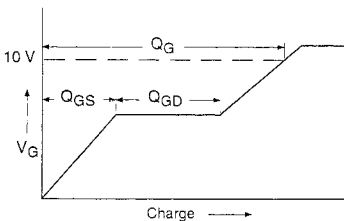
**Fig 12a.** Unclamped Inductive Test Circuit



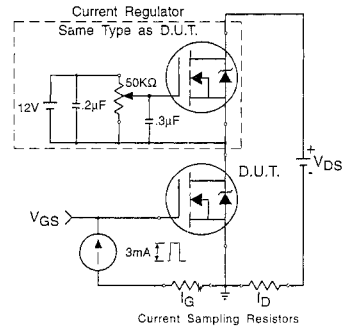
**Fig 12b.** Unclamped Inductive Waveforms



**Fig 12c.** Maximum Avalanche Energy Vs. Drain Current



**Fig 13a.** Basic Gate Charge Waveform

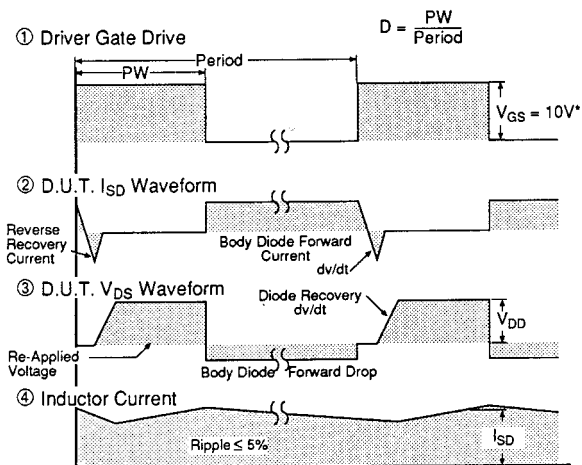
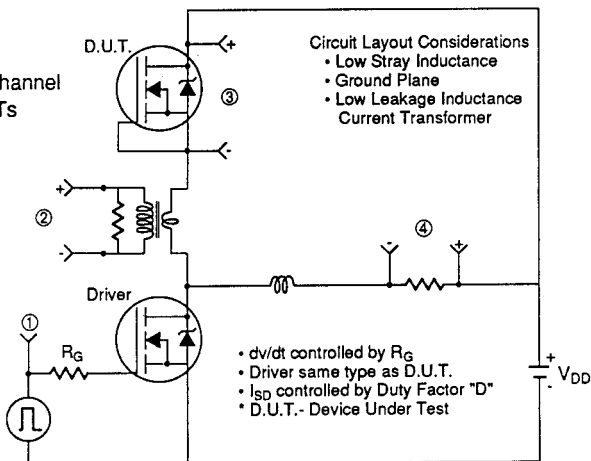


**Fig 13b.** Gate Charge Test Circuit

## Appendix A

### Peak Diode Recovery dv/dt Test Circuit

Fig 14. For N-Channel HEXFETs



\*  $V_{GS} = 5V$  for Logic Level Devices

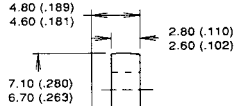
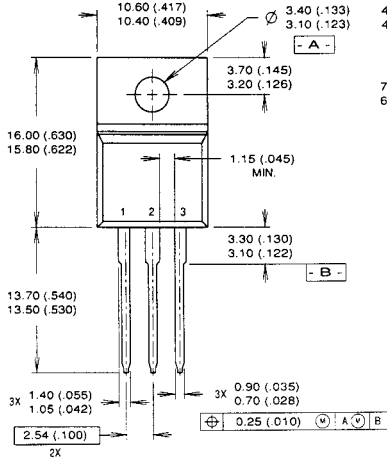
# IRFIBC40GLC



## Package Outline

### TO-220 FullPak Outline

Dimensions are shown in millimeters (inches)

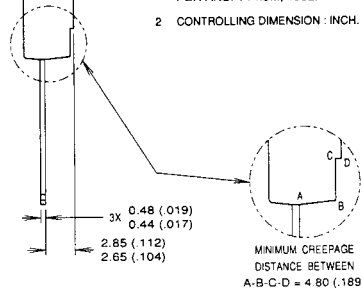


#### LEAD ASSIGNMENTS

- 1 - GATE
- 2 - DRAIN
- 3 - SOURCE

#### NOTES:

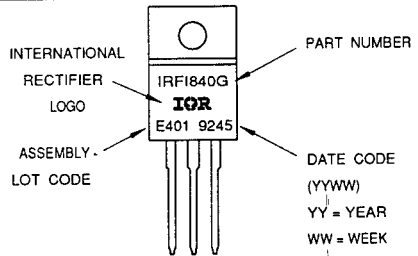
- 1 DIMENSIONING & TOLERANCING PER ANSI Y14.5M, 1982.
- 2 CONTROLLING DIMENSION : INCH.



## Part Marking Information

### TO-220 FULL-PAK

EXAMPLE: THIS IS AN IRF1840G WITH ASSEMBLY LOT CODE E401



## Appendix C