

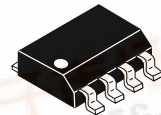
## The MRFIC Line Broadband GaAs Switch

The MRFIC0903 is an integrated GaAs SPDT switch designed for transceivers operating in the 100 MHz to 2.0 GHz frequency range. The design utilizes Motorola's advanced GaAs RF process to yield superior performance in a cost effective monolithic device. Applications for the MRFIC0903 include Class 4 and 5 GSM, Class 1 and 2 DCS1800, DCS1900, DAMPS, PDC, digital cellular systems as well as analog cellular systems.

- 2.8 W Transmitting Capability through the Transmit Path with a 5.0 Volt Differential Control Signal
- 1.25 W Transmitting Capability through the Transmit Path with a 3.0 Volt Differential Control Signal
- Single Source Operating Supply Voltage
- Low Power Consumption
- Low-Cost, Low Profile Plastic SOIC Package
- Available in Tape and Reel by Adding R2 Suffix. R2 Suffix = 2,500 Units per Reel.
- Device Marking = M0903

### MRFIC0903

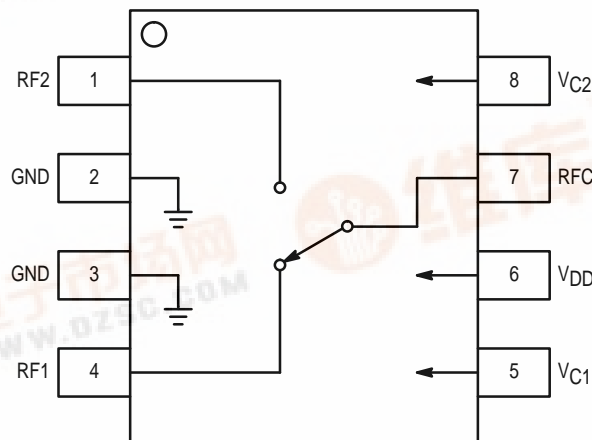
**ANTENNA SWITCH  
GaAs MONOLITHIC  
INTEGRATED CIRCUIT**



**CASE 751-05  
(SO-8)**

#### ABSOLUTE MAXIMUM RATINGS (T<sub>A</sub> = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Supply Voltage	V <sub>DD</sub>	10	Vdc
Control Voltage	V <sub>C1</sub> , V <sub>C2</sub>	V <sub>DD</sub> + 0.8, V <sub>DD</sub> - 12	Vdc
Power Dissipation	P <sub>D</sub>	1.0	W
Power Input (Non-selected Port)	P <sub>in</sub>	0.325	W
Ambient Operating Temperature	T <sub>A</sub>	-35 to +85	°C
Storage Temperature	T <sub>stg</sub>	-65 to +150	°C



**Pin Connections and Functional Block Diagram**

## RECOMMENDED OPERATING RANGES

Parameter	Symbol	Value	Unit
Supply Voltage	$V_{DD}$	0 to 5.0	Vdc
Control Voltage Range	$V_{C1}, V_{C2}$	$V_{DD} - 5.0$ to $V_{DD} + 0.5$	Vdc
RF Frequency Range	$f_{RF}$	100 to 2000	MHz

## ELECTRICAL CHARACTERISTICS ( $V_{DD} = 5.0$ V, $P_{in} = 2.5$ W (34 dBm), $f = 900$ MHz, $T_A = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Min	Typ	Max	Unit
Supply Current				
$I_{DD}$	—	100	170	$\mu\text{A}$
$I_{Control}$	—	150	300	$\mu\text{A}$
VSWR	—	1.5:1	—	
Insertion Loss (RFC/RF1, RFC/RF2)	—	0.55	0.8	dB
Isolation (RFC/RF2, RFC/RF1)	18	20	—	dB
Output Power at 0.1 dB Compression	—	34.5	—	dBm

Electrical Characteristics at 900 MHz measured in test circuit schematic shown in Figure 1 with board losses removed.

## ELECTRICAL CHARACTERISTICS ( $V_{DD} = 5.0$ V, $P_{in} = 2.0$ W (33 dBm), $f = 1800$ MHz, $T_A = 25^\circ\text{C}$ unless otherwise noted)

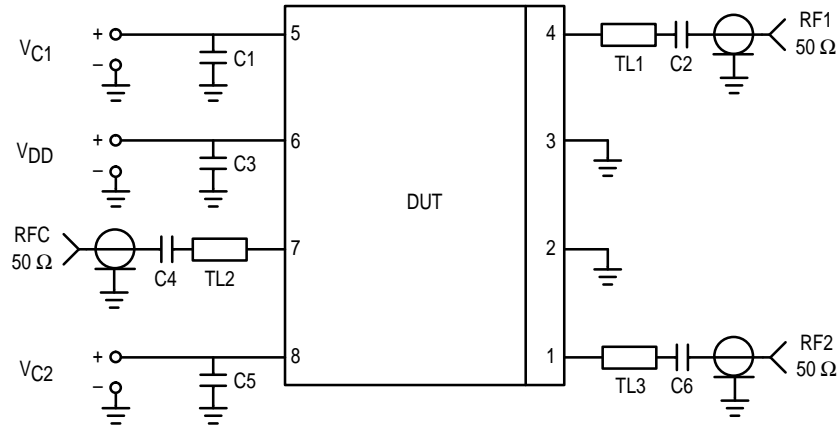
Characteristic	Min	Typ	Max	Unit
Supply Current				
$I_{DD}$	—	100	170	$\mu\text{A}$
$I_{Control}$	—	150	300	$\mu\text{A}$
VSWR	—	1.5:1	—	
Insertion Loss (RFC/RF1, RFC/RF2)	—	0.7	0.85	dB
Isolation (RFC/RF2, RFC/RF1)	18	20	—	dB
Output Power at 0.1 dB Compression	—	34	—	dBm

Electrical Characteristics at 1800 MHz measured in test circuit schematic shown in Figure 2 with board losses removed.

$V_{C1}$ and $V_{C2}$ Input Voltage	Min	Typ	Max	Unit
High	$V_{DD}$	—	$V_{DD} + 0.5$	Vdc
Low	$V_{DD} - 10$	—	$V_{DD} - 5$	Vdc

$V_{C1}$	$V_{C2}$	RFC – RF1	RFC – RF2
High	Low	Insertion Loss	Isolation
Low	High	Isolation	Insertion Loss

Table 1. Logic Levels

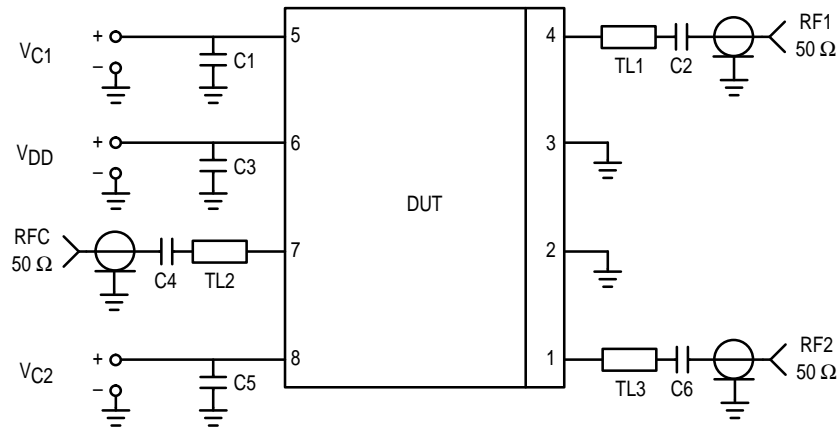


C1, C5 — 2.7 pF, Chip Capacitor  
 C2, C4, C6 — 100 pF, Chip Capacitor  
 C3 — 10 pF, Chip Capacitor

TL1, TL3 — 12 degrees of 50 Ω line at 1 GHz  
 TL2 — 15 degrees of 50 Ω line at 1 GHz

Note: Decoupling capacitors on pins 5, 6 and 8 must be as close as possible to the pins.

**Figure 1. 300 MHz to 1600 MHz Test Circuit Configuration**



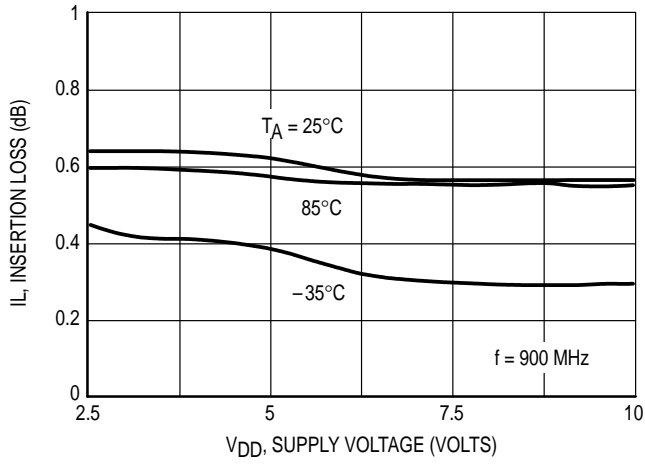
C1, C5 — 1.3 pF, Chip Capacitor  
 C2, C3, C4, C6 — 8.2 pF, Chip Capacitor

TL1, TL3 — 12 degrees of 50 Ω line at 1 GHz  
 TL2 — 15 degrees of 50 Ω line at 1 GHz

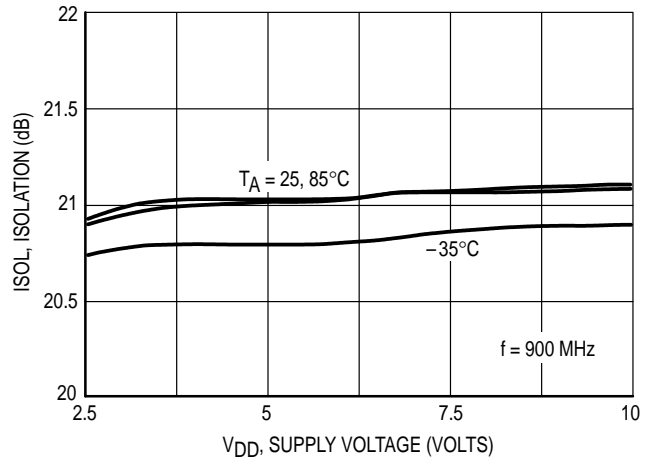
Note: Decoupling capacitors on pins 5, 6 and 8 must be as close as possible to the pins.

**Figure 2. 1600 MHz to 2000 MHz Test Circuit Configuration**

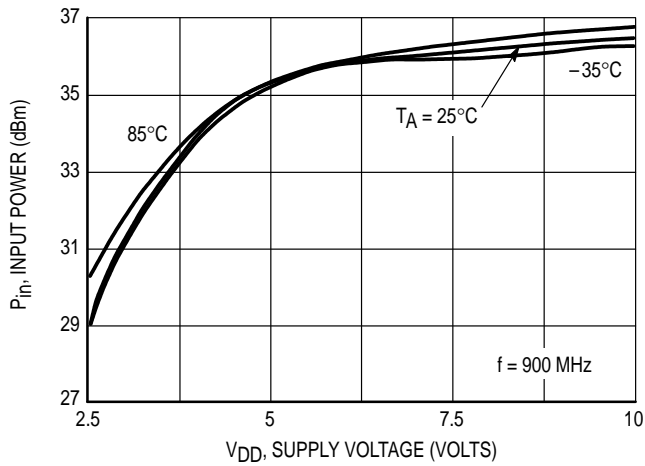
## TYPICAL CHARACTERISTICS



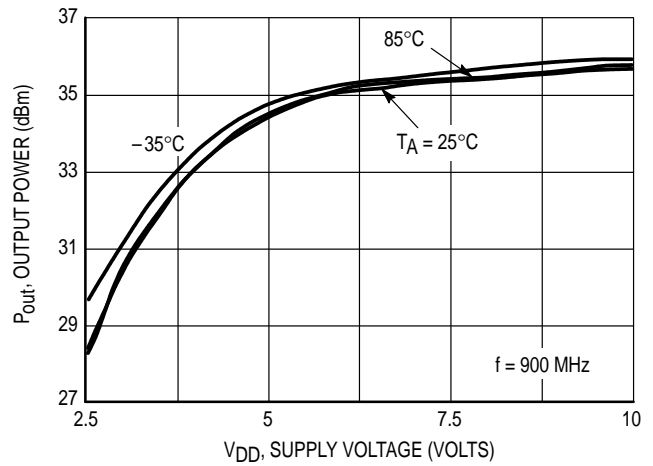
**Figure 3. Insertion Loss at 0.1 dB Compression versus Supply Voltage**



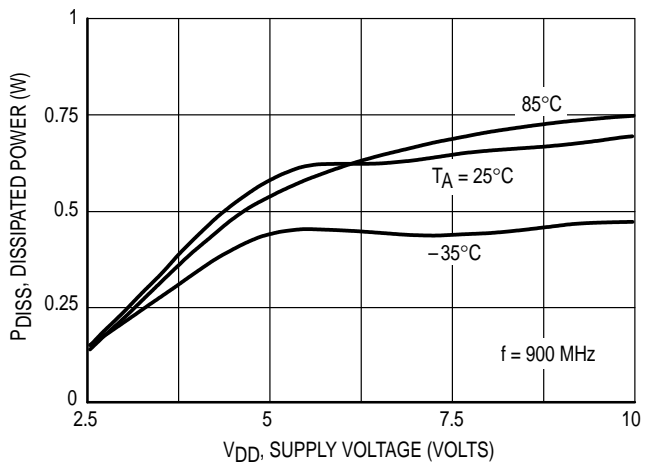
**Figure 4. Isolation at 0.1 dB Compression versus Supply Voltage**



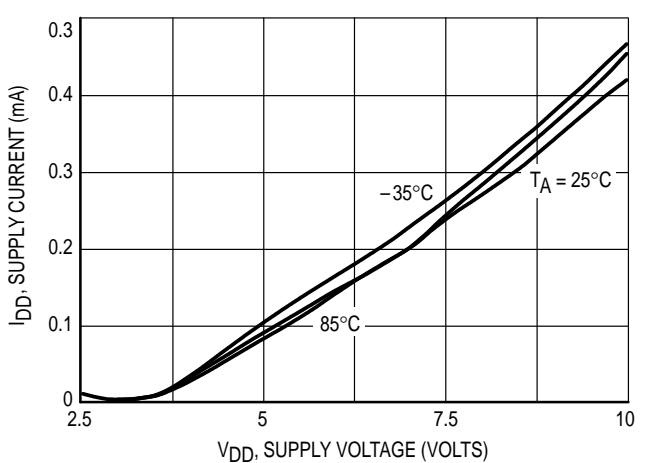
**Figure 5. Input Power at 0.1 dB Compression versus Supply Voltage**



**Figure 6. Output Power at 0.1 dB Compression versus Supply Voltage**

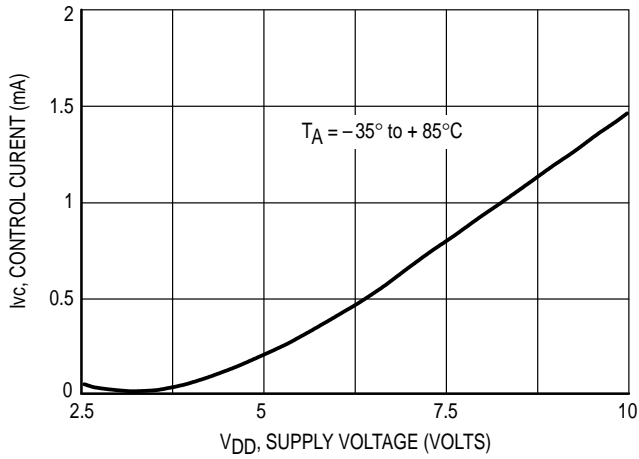


**Figure 7. Dissipated Power at 0.1 dB Compression versus Supply Voltage**

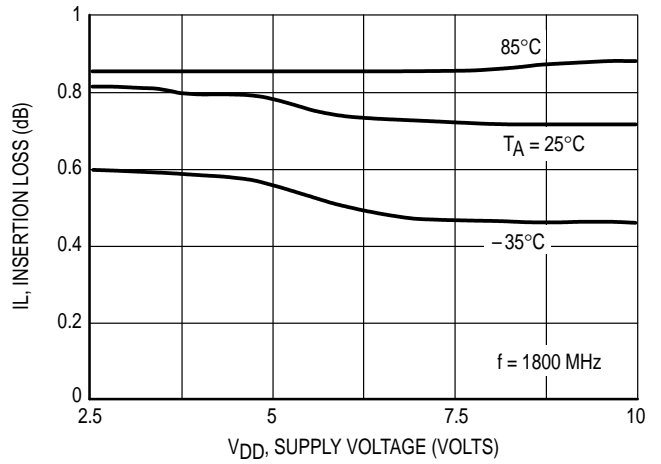


**Figure 8. Supply Current at 0.1 dB Compression versus Supply Voltage**

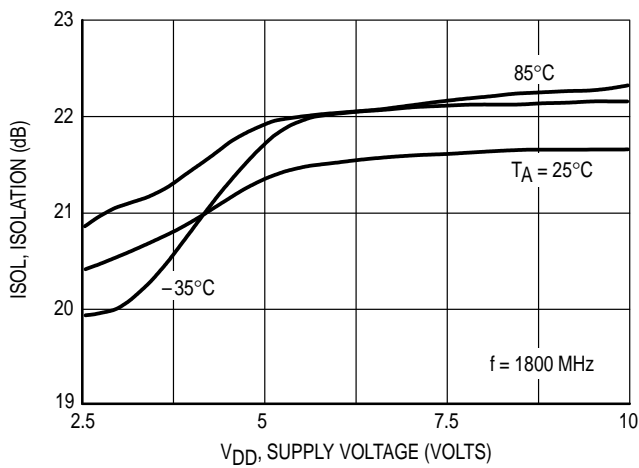
## TYPICAL CHARACTERISTICS



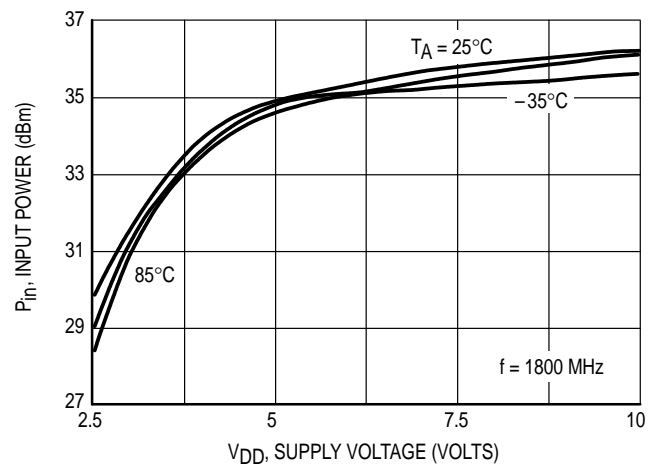
**Figure 9. Control Current at Vc Pins at 0.1 dB Compression versus Supply Voltage**



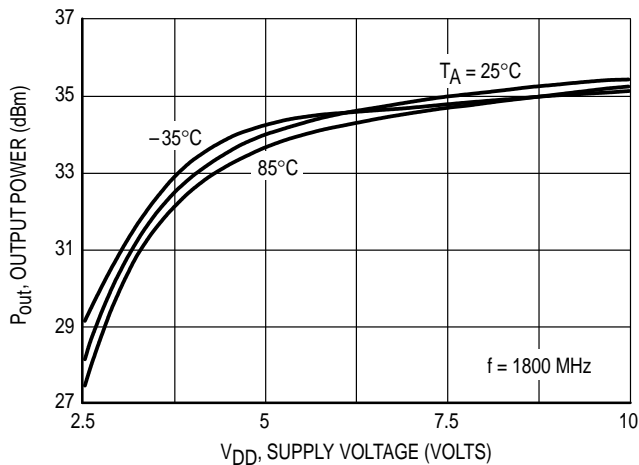
**Figure 10. Insertion Loss at 0.1 dB Compression versus Supply Voltage**



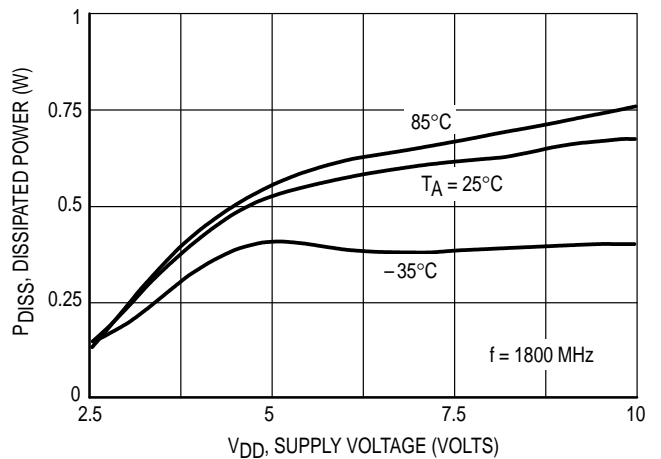
**Figure 11. Isolation at 0.1 dB Compression versus Supply Voltage**



**Figure 12. Input Power at 0.1 dB Compression versus Supply Voltage**



**Figure 13. Output Power at 0.1 dB Compression versus Supply Voltage**



**Figure 14. Dissipated Power at 0.1 dB Compression versus Supply Voltage**

## TYPICAL CHARACTERISTICS

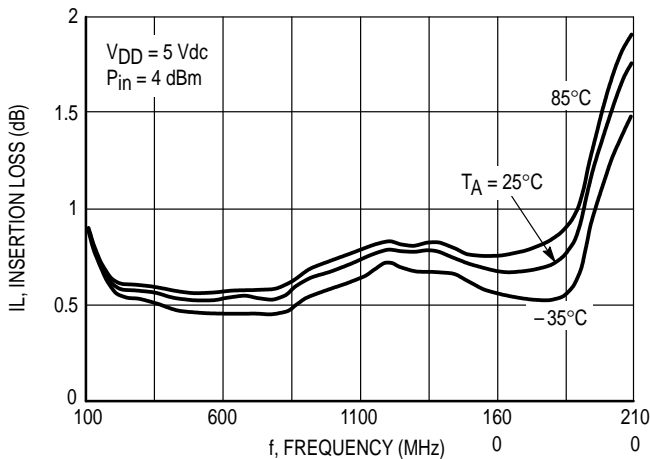


Figure 15. Insertion Loss versus Frequency

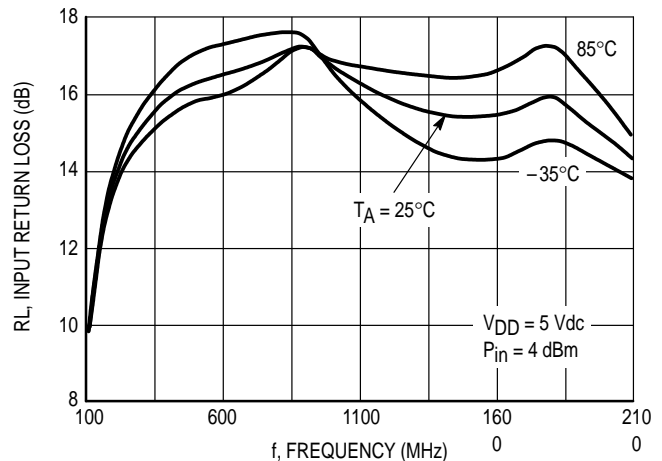


Figure 16. Input Return Loss versus Frequency

## APPLICATIONS INFORMATION

### DESIGN INFORMATION

The MRFIC0903 SPDT antenna switch was designed for low cost, flexibility and ease of use. This is accomplished by its internal topology that allows control of the switch through its TTL/CMOS compatible (0 to  $V_{DD}$ ) control pins. Operating on a single positive supply, the switch was designed for a minimum supply voltage, minimum power consumption and low current TTL/CMOS compatible control signals.

### THEORY OF OPERATION

The MRFIC0903 can be used as a transmit and receive or antenna diversity switch in the frequency range from 100 MHz to 2 GHz with incident power levels as high as 4 watts.

The frequency behavior can be optimized by resonating the DC blocking capacitor's position and value with the parasitic inductance of the package lead. Operation from 300 MHz to 1.6 GHz can be optimized with a high Q 100 pF blocking capacitor. For the higher frequency band from 1.6 GHz to 2.0 GHz, a 8.2 pF capacitor is suggested. Further improvements can be achieved by resonating the inductance of  $V_{DD}$ ,  $V_{C1}$ , and  $V_{C2}$  pins with the appropriate capacitor values.

The power handling capability and linearity of the MRFIC0903 is dependent only on the supply voltage. With a 3 V supply, the device handles 1.25 W (1.6 W PEP) of incident power while maintaining good linearity and low harmonic distortion. The power transmitting capability increases to 3 W of incident power with a 5 V supply and up to 4 W with a 7.5 V supply.

Due to the device's inherently low harmonic distortion, the switch requires little harmonic filtering at its outputs. It also has a high reverse third-order intercept point for use in non-TDMA antenna diversity applications (analog cellular systems).

### BIASING CONSIDERATIONS

The MRFIC0903 is based on a floating "cold FET" topology. With this topology, the differential voltage between  $V_{C1}$  and  $V_{C2}$  dictates the power handling capability. For example, the device's power handling capability is the same with the device biased with 5 V at  $V_{C1}$  and 0 V at  $V_{C2}$ , with 0 V at  $V_{C1}$  and -5 V at  $V_{C2}$ , or with 3 V at  $V_{C1}$  and -2 V at  $V_{C2}$ .

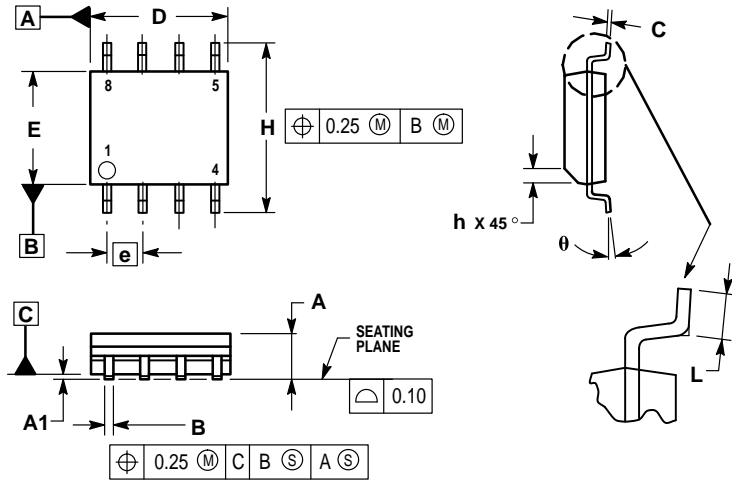
### POSSIBLE APPLICATIONS

The MRFIC0903 can be used in a number of cellular and cordless phone applications. The part is applicable for analog cellular phones in systems such as AMPS, TACS, NAMPS, ETACS and NMT900; for digital cellular phones in systems such as GSM, PDC, DAMPS, DCS1800, PCS and NADC; and for cordless phones in systems such as DECT, PHS, ISM, CT1 and CT2. In general it can fit into any application where high power handling capability is required for frequencies ranging from 100 MHz to 2 GHz.

### EVALUATION BOARDS


Evaluation boards are available for RF Monolithic Integrated Circuits by adding a "TF" suffix to the device type. For a complete list of currently available boards and ones in development for newly introduced product, please contact your local Motorola Distributor or Sales Office.

## PACKAGE DIMENSIONS



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
  2. DIMENSIONS ARE IN MILLIMETERS.
  3. DIMENSION D AND E DO NOT INCLUDE MOLD PROTRUSION.
  4. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.
  5. DIMENSION B DOES NOT INCLUDE MOLD PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 TOTAL IN EXCESS OF THE B DIMENSION AT MAXIMUM MATERIAL CONDITION.

**CASE 751-05  
ISSUE S**

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