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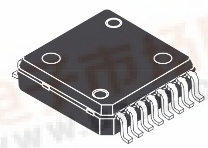
The MRFIC Line
900 MHz GaAs Integrated Power Amplifier

Designed primarily for use in high efficiency Analog Cellular applications, the MRFIC0912 is a two–stage power amplifier in Motorola's proprietary Power Flat Pack 16–lead package. This integrated circuit requires minimal off-chip matching while allowing for the maximum in flexibility in optimizing gain and efficiency. The design employs Motorola's planar, self–aligned GaAs MESFET IC process to give the highest efficiency possible.

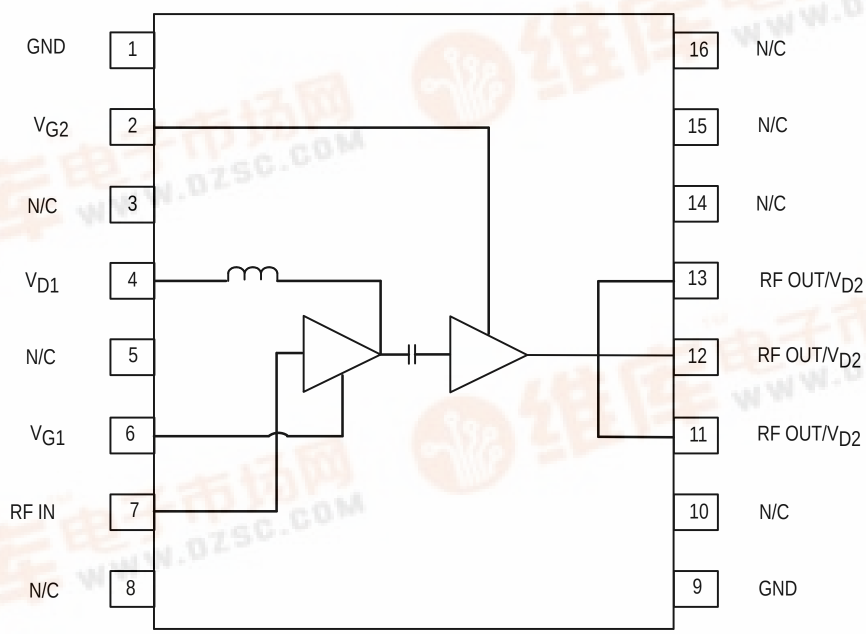
- Usable Frequency Range = 800–1000 MHz, Specified for 824–905 MHz
- 30.8 dBm Minimum Output Power
- 470 mA Maximum Supply Current at 30.8 dBm Output
- 23.8 dB Minimum Gain
- Simple Off–chip Matching for Maximum Power/Efficiency Flexibility
- 4.6 Volt Supply
- 45 dB/Volt Typical Power Output Control
- Order MRFIC0912R2 for Tape and Reel Option.
  R2 Suffix = 1,500 Units per 16 mm, 13 inch Reel.
- Device Marking = M0912

MRFIC0912

900 MHz
GaAs INTEGRATED
POWER AMPLIFIER



CASE 978–02
(PFP–16)



Pin Connections and Functional Block Diagram

MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

Ratings	Symbol	Limit	Unit
Supply Voltage	V_{D1}, V_{D2}	8	Vdc
RF Input Power	P_{RF}	20	dBm
Gate Voltage	V_{G1}, V_{G2}, V_{GG}	–5	Vdc
Storage Temperature Range	T_{stg}	– 65 to +150	°C
Operating Case Temperature	T_C	– 35 to +100	°C
Thermal Resistance, Junction to Case	$R_{\theta JC}$	18	°C/W

RECOMMENDED OPERATING RANGES

Parameter	Symbol	Value	Unit
RF Frequency	f_{RF}	824–905	MHz
Supply Voltage	V_{D1}, V_{D2}	4.0–6.0	Vdc
Gate Voltage	V_{G1}, V_{G2}	–2.3 to –1.5	Vdc

ELECTRICAL CHARACTERISTICS (V_{D1}, V_{D2} = 4.6 V, T_A = 25°C, f_{RF} = 840 MHz, P_{in} = 7 dBm, V_{GG} set for I_{D2Q} = 200 mA, Tested in Circuit Shown in Figure 1)

Characteristic	Min	Typ	Max	Unit
RF Output Power	30.8	31.2	—	dBm
Power Slump (V_{D1}, V_{D2} = 4.0 V, T_C = 100°C)	28.5	—	—	dBm
Load Mismatch Survival (V_{D1}, V_{D2} = 7 V, Load VSWR = 10:1, all phases, 10 sec)		No Degradation		
Spurious Output (V_{D1},V_{D2} = 0 to 7 V, P_{in} = 5 to 9 dBm, Load VSWR = 10:1)	—	—	–60	dBc
Input Return Loss	—	10	—	dB
Harmonic Output (P_{out} = 30.8 dBm)				dBc
$2f_0$	—	—	–25	
$3f_0$	—	—	–40	
$4f_0$	—	—	–40	
Noise Power (V_{DD} = 0 to 7 V, 45 MHz Above f_{RF} at 30 kHz BW)	—	—	–93	dBm
Maximum Power Control Voltage Slope (Change in P_{out} for Change on V_{D1})	—	45	—	dB/V
Total Supply Current (V_{D1} set for P_{out} = 30.8 dBm)	—	430	470	mA
V_{GG} Required for I_{D2Q} = 200 mA	–2.3	–2.0	–1.7	Vdc
Gate Current during RF Operation	–2	—	2	mA

DESIGN AND APPLICATIONS INFORMATION

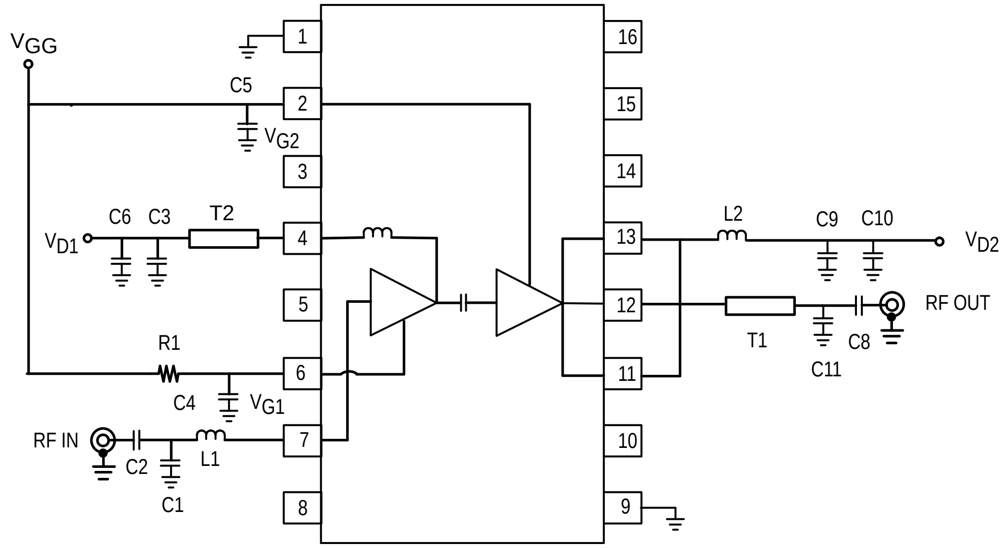
The MRFIC0912 has been designed for high efficiency 900 MHz applications such as analog cellular and Industrial, Medical and Scientific (ISM) equipment. The two stage MESFET design utilizes Motorola's planar refractory gate process to allow high performance GaAs to be applied to consumer applications. The proprietary PFP–16 package assures good grounding and low thermal resistance.

As shown in Figure 1, the gate voltage pins can be ganged together and one voltage applied to both gates to set the quiescent operating current. Alternatively, V_{G1} and V_{G2} can be set separately. V_{D1} can be used as power control with a 45 dB per volt sensitivity. The placement of C3 in the V_{D1} supply line can be varied to optimize RF performance since T2 is part of a shunt L matching section. On the output, pins 11, 12 and 13, the placement of C11 is adjusted for best RF performance.

Layout is important for amplifier stability and RF performance. Ground vias must be located as close to circuit ground connections as possible. Power supply bypassing C3, C6, C9, and C10 must be included to reduce out–of–band gain and prevent spurious output.

Evaluation Boards

Evaluation boards are available for RF Monolithic Integrated Circuits by adding a "TF" suffix to the device type. For a complete list of currently available boards and ones in development for newly introduced product, please contact your local Motorola Distributor or Sales Office.



R1	1 kΩ	C6	0.01 µF	L2	22 nH
C1	3.3 pF	C10	1 µF	T1	50 Ω, 13° @ 840 MHz
C2, C3, C8, C9	100 pF	C4, C5	1000 pF	T2	50 Ω, 8° @ 840 MHz
C11	8.2 pF	L1	10 nH	BOARD MATERIAL — GLASS/EPOXY, ε_r = 4.45, THICKNESS = 18 MIL	

Figure 1. Applications Circuit Configuration

TYPICAL CHARACTERISTICS

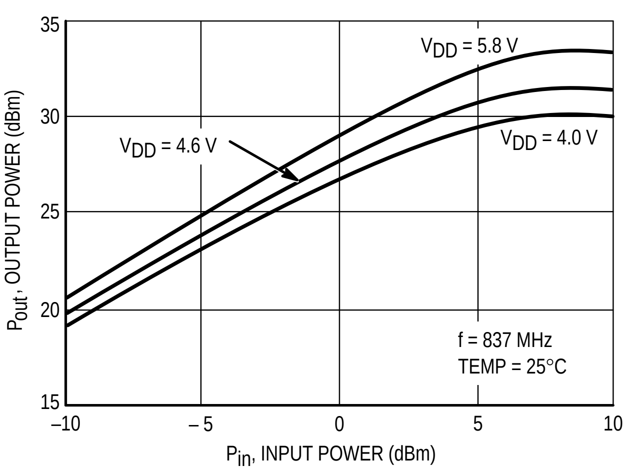


Figure 2. Output Power versus Input Power

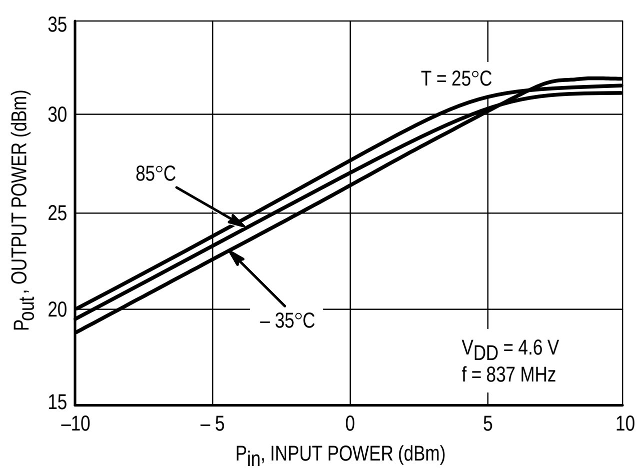


Figure 3. Output Power versus Input Power

TYPICAL CHARACTERISTICS

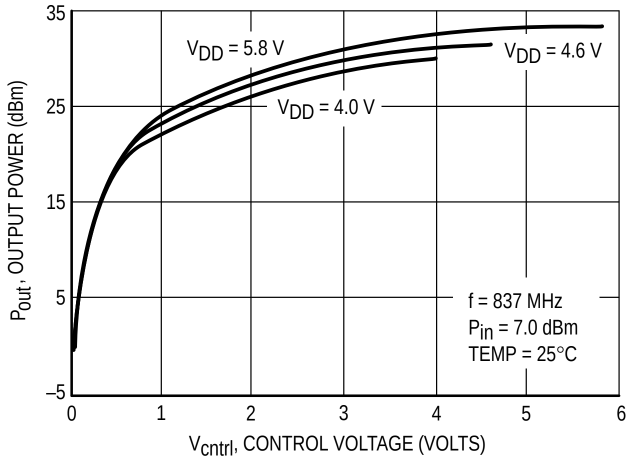


Figure 4. Output Power versus Control Voltage

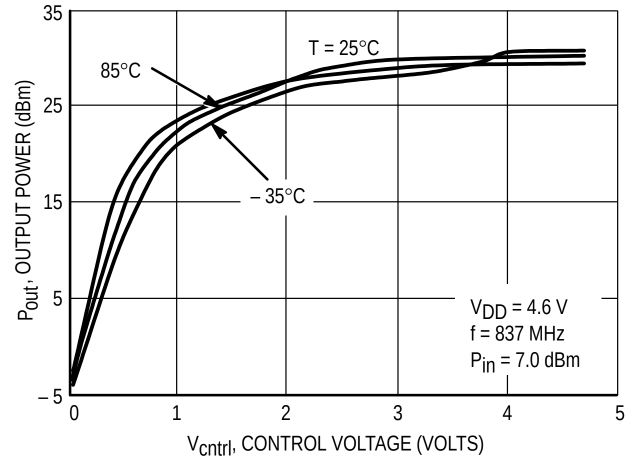


Figure 5. Output Power versus Control Voltage

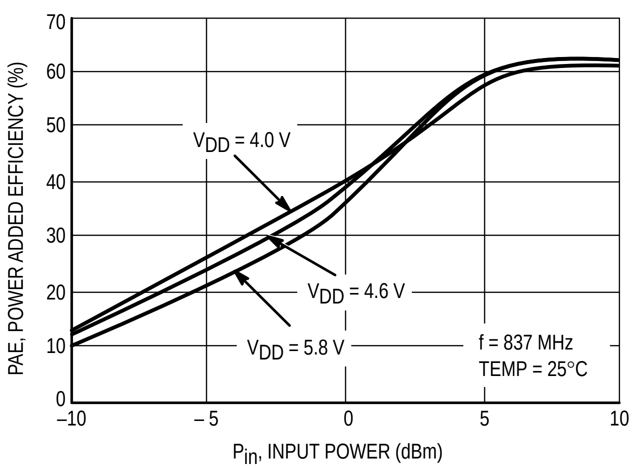


Figure 6. Power Added Efficiency versus Input Power

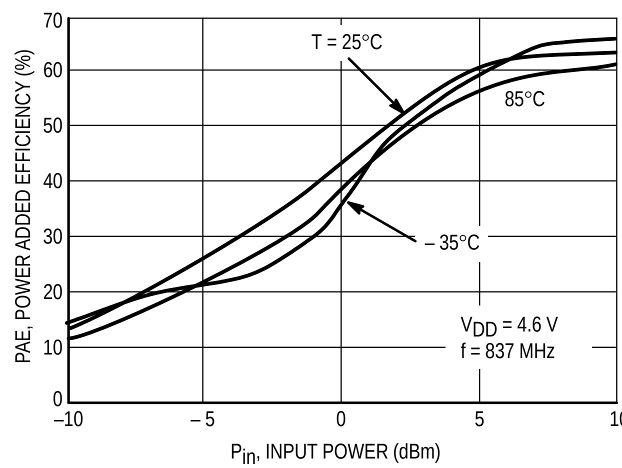


Figure 7. Power Added Efficiency versus Input Power

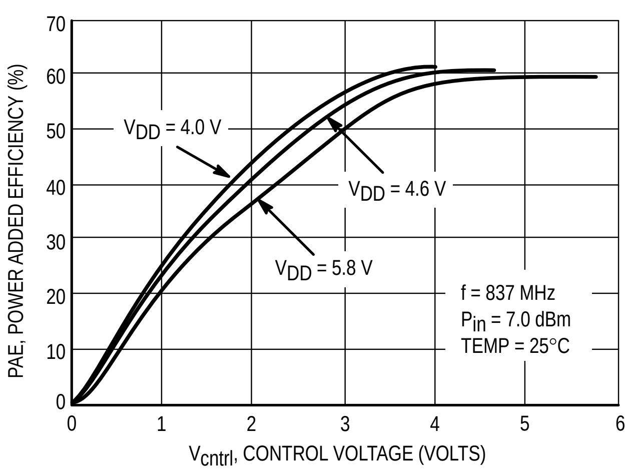


Figure 8. Power Added Efficiency versus Control Voltage

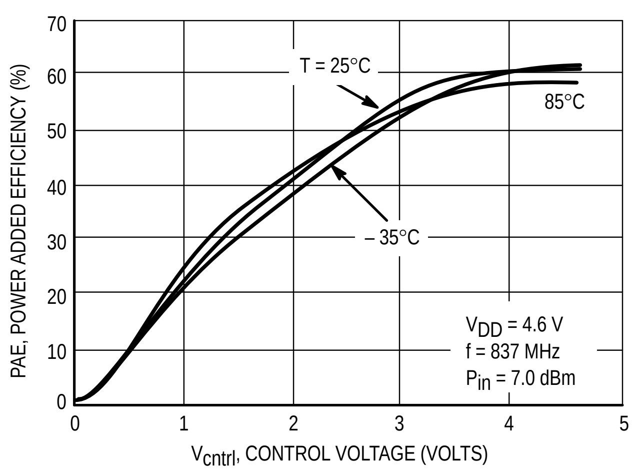


Figure 9. Power Added Efficiency versus Control Voltage

TYPICAL CHARACTERISTICS

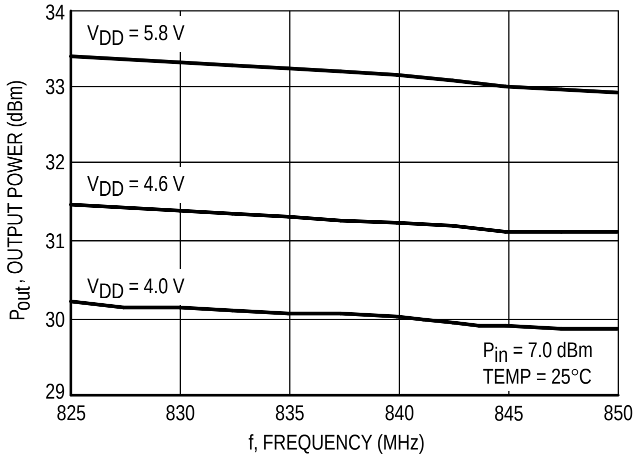


Figure 10. Output Power versus Frequency

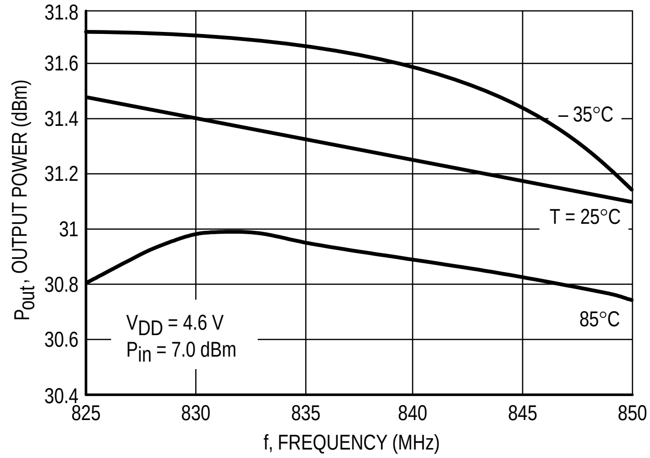


Figure 11. Output Power versus Frequency

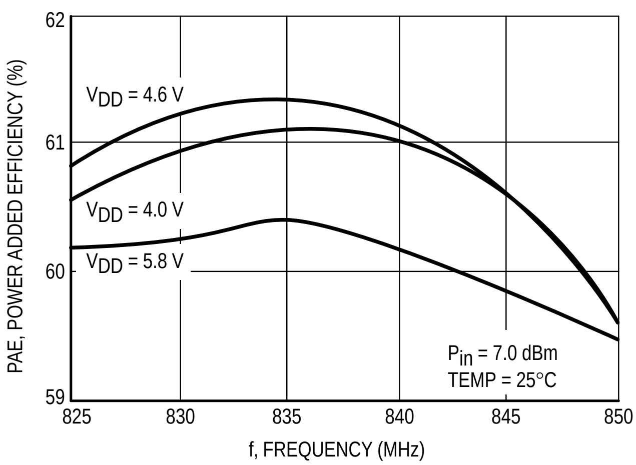


Figure 12. Power Added Efficiency versus Frequency

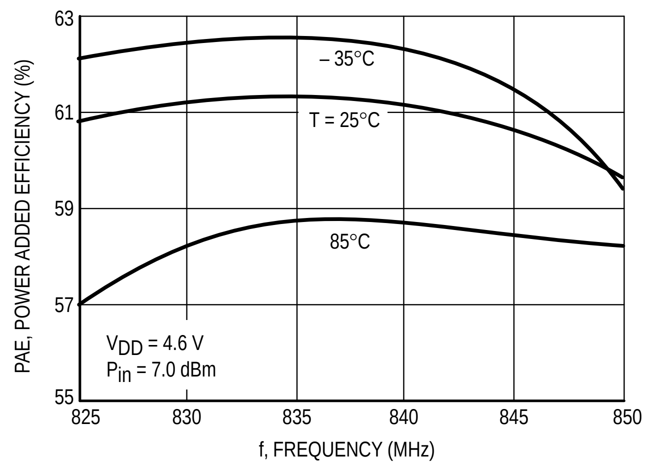


Figure 13. Power Added Efficiency versus Frequency

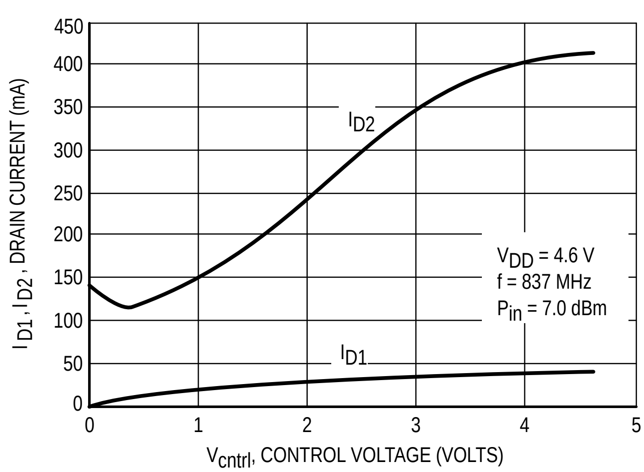
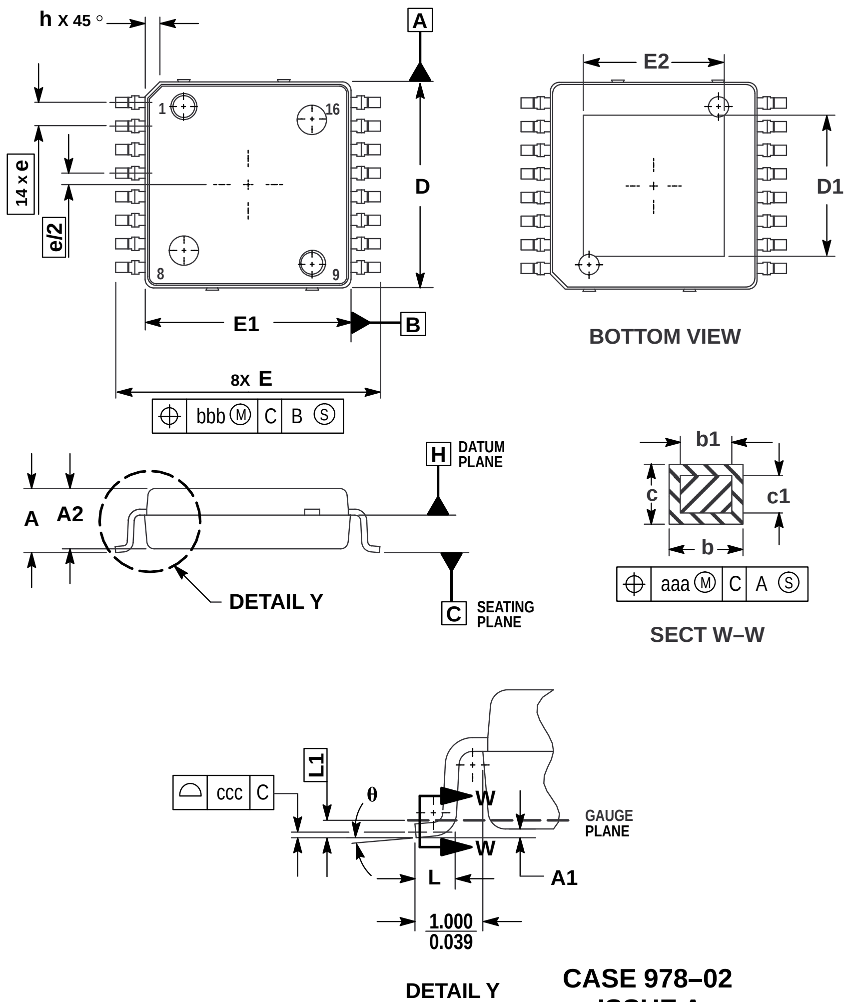


Figure 14. Drain Current versus Control Voltage

PACKAGE DIMENSIONS



NOTES:
1. CONTROLLING DIMENSION: MILLIMETER.
2. DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994.
3. DATUM PLANE –H– IS LOCATED AT BOTTOM OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE BOTTOM OF THE PARTING LINE.
4. DIMENSIONS D AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.250 PER SIDE. DIMENSIONS D AND E1 DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE –H–.
5. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION IS 0.127 TOTAL IN EXCESS OF THE b DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. DATUMS –A– AND –B– TO BE DETERMINED AT DATUM PLANE –H–.

	MILLIMETERS	
DIM	MIN	MAX
A	2.000	2.350
A1	0.025	0.152
A2	1.950	2.100
D	6.950	7.100
D1	4.372	5.180
E	8.850	9.150
E1	6.950	7.100
E2	4.372	5.180
L	0.466	0.720
L1	0.250 BSC	
b	0.300	0.432
b1	0.300	0.375
c	0.180	0.279
c1	0.180	0.230
e	0.800 BSC	
h	——	0.600
θ	0 °	7 °
aaa	0.200	
bbb	0.200	
ccc	0.100	

CASE 978–02
ISSUE A

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JAPAN: Nippon Motorola Ltd.; Tatsumi–SPD–JLDC, 6F Seibu–Butsuryu–Center, 3–14–2 Tatsumi Koto–Ku, Tokyo 135, Japan. 81–3–3521–8315

ASIA / PACIFIC: Motorola Semiconductors H.K. Ltd.; 8B Tai Ping Industrial Park, 51 Ting Kok Road, Tai Po, N.T., Hong Kong. 852–26629298