Document Title

128K x 8 High-Speed SRAM

Revision History

Revision No	History	Draft Date	Remark
0A	Initial Draft	March 13,2001	
0B	Revise typo on page 6 and page 8	October 18,2001	

128K x 8 HIGH-SPEED CMOS STATIC RAM

FEATURES

- High-speed access time: 12, 15, 20, 25 ns
- Low active power: 600 mW (typical)
- Low standby power: 500 µW (typical) CMOS standby
- Output Enable ($\overline{OE}$) and two Chip Enable ($\overline{CE}1$ and CE2) inputs for ease in applications
- Fully static operation: no clock or refresh required
- TTL compatible inputs and outputs
- Single 5V (±10%) power supply
- Low power version available: IC61C1024L
- Commercial and industrial temperature ranges available

DESCRIPTION

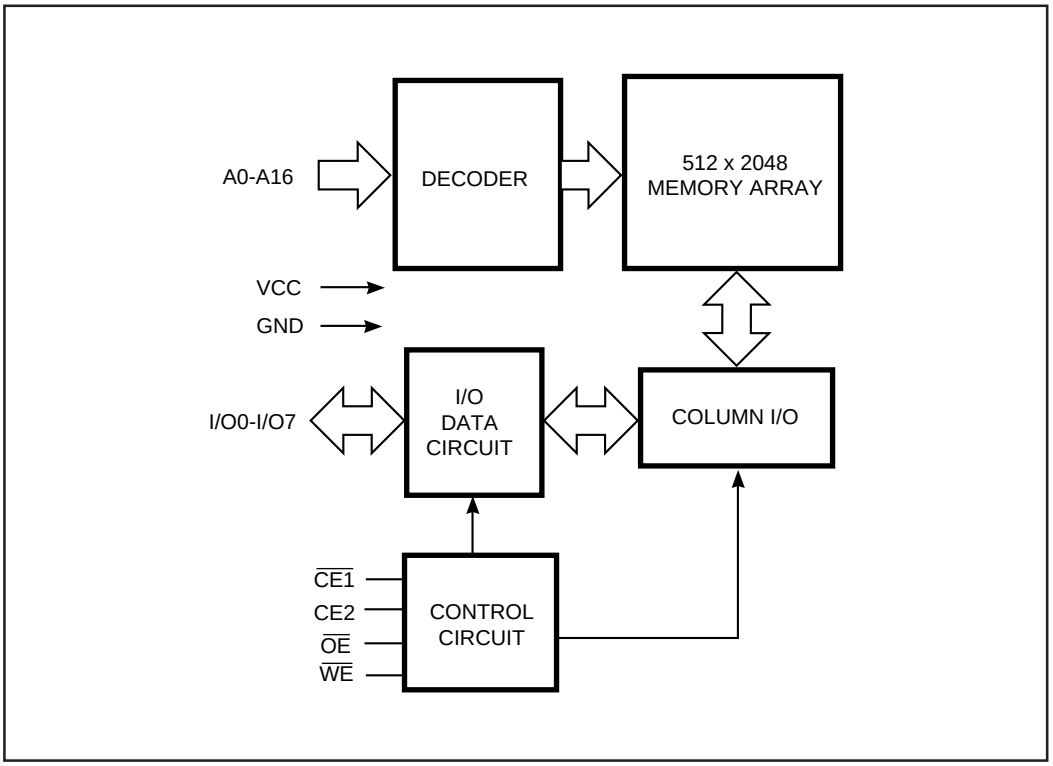
The *ICSI* IC61C1024 and IC61C1024L are very high-speed, low power, 131,072-word by 8-bit CMOS static RAMs. They are fabricated using *ICSI*'s high-performance CMOS technology. This highly reliable process coupled with innovative circuit design techniques, yields higher performance and low power consumption devices.

When $\overline{CE}1$ is HIGH or CE2 is LOW (deselected), the device assumes a standby mode at which the power dissipation can be reduced by using CMOS input levels.

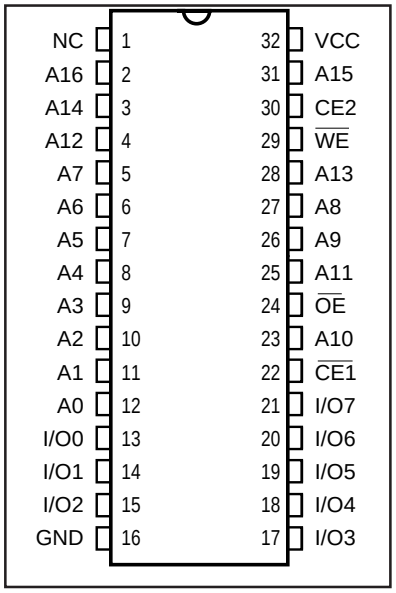
Easy memory expansion is provided by using two Chip Enable inputs, $\overline{CE}1$ and CE2. The active LOW Write Enable ($\overline{WE}$) controls both writing and reading of the memory.

The IC61C1024 and IC61C1024L are available in 32-pin 300mil SOJ, and 8*20mm TSOP-1, and 8*13.4mm TSOP-1 packages.

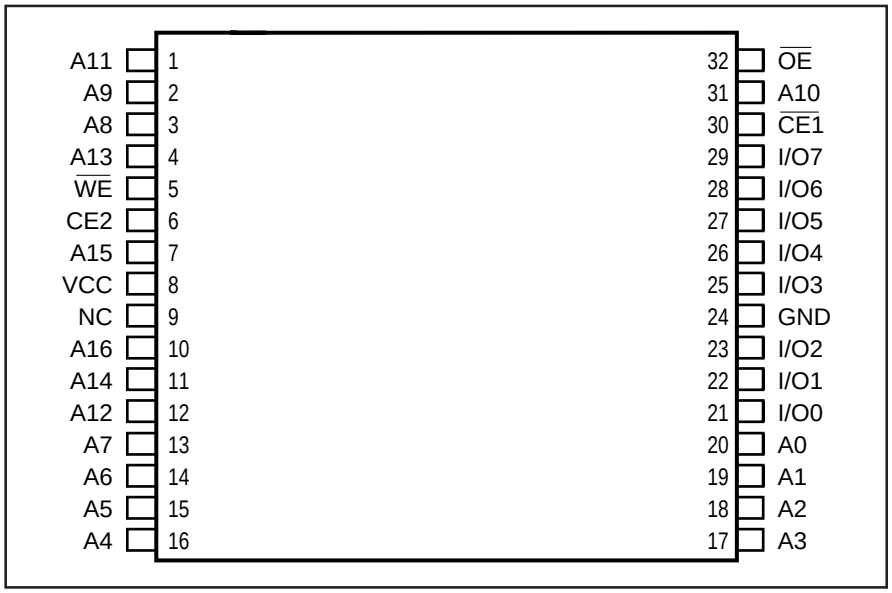
FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION
32-Pin SOJ



PIN CONFIGURATION
32-Pin 8x20mm TSOP-1 and 8x13.4mm TSOP-1



PIN DESCRIPTIONS

A0-A16	Address Inputs
$\overline{CE}$1	Chip Enable 1 Input
CE2	Chip Enable 2 Input
$\overline{OE}$	Output Enable Input
$\overline{WE}$	Write Enable Input
I/O0-I/O7	Input/Output
Vcc	Power
GND	Ground

OPERATING RANGE

Range	Ambient Temperature	Vcc
Commercial	0°C to +70°C	5V ± 10%
Industrial	–40°C to +85°C	5V ± 10%

TRUTH TABLE

Mode	$\overline{WE}$	$\overline{CE}$1	CE2	$\overline{OE}$	I/O Operation	Vcc Current
Not Selected	X	H	X	X	High-Z	I_{SB1}, I_{SB2}
(Power-down)	X	X	L	X	High-Z	I_{SB1}, I_{SB2}
Output Disabled	H	L	H	H	High-Z	I_{CC1}, I_{CC2}
Read	H	L	H	L	D_{OUT}	I_{CC1}, I_{CC2}
Write	L	L	H	X	D_{IN}	I_{CC1}, I_{CC2}

ABSOLUTE MAXIMUM RATINGS[1]

Symbol	Parameter	Value	Unit
V_{TERM}	Terminal Voltage with Respect to GND	–0.5 to +7.0	V
T_{BIAS}	Temperature Under Bias	–55 to +125	°C
T_{STG}	Storage Temperature	–65 to +150	°C
P_T	Power Dissipation	1.5	W
I_{OUT}	DC Output Current (LOW)	20	mA

Notes:
1. Stress greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

CAPACITANCE[1,2]

Symbol	Parameter	Conditions	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	5	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	7	pF

Notes:
1. Tested initially and after any design or process changes that may affect these parameters.
2. Test conditions: T_A = 25°C, f = 1 MHz, Vcc = 5.0V.

DC ELECTRICAL CHARACTERISTICS (Over Operating Range)

Symbol	Parameter	Test Conditions		Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = –4.0 mA		2.4	—	V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 8.0 mA		—	0.4	V
V_{IH}	Input HIGH Voltage			2.2	V_{CC} + 0.5	V
V_{IL}	Input LOW Voltage[1]			–0.3	0.8	V
I_{LI}	Input Leakage	GND ≤ V_{IN} ≤ V_{CC}	Com. Ind.	–2 –5	2 5	µA
I_{LO}	Output Leakage	GND ≤ V_{OUT} ≤ V_{CC} Outputs Disabled	Com. Ind.	–2 –5	2 5	µA

Note:
1. V_{IL} = –3.0V for pulse width less than 10 ns.

IC61C1024 POWER SUPPLY CHARACTERISTICS[1] (Over Operating Range)

Symbol	Parameter	Test Conditions		-12 ns Min.	-12 ns Max.	-15 ns Min.	-15 ns Max.	-20 ns Min.	-20 ns Max.	-25 ns Min.	-25 ns Max.	Unit
I_{CC1}	Vcc Operating Supply Current	V_{CC} = V_{CC} MAX., $\overline{CE}$ = V_{IL} I_{OUT} = 0 mA, f = 0	Com. Ind.	— —	85 110	— —	85 110	— —	85 110	— —	85 110	mA
I_{CC2}	Vcc Dynamic Operating Supply Current	V_{CC} = V_{CC} MAX., $\overline{CE}$ = V_{IL} I_{OUT} = 0 mA, f = f_{MAX}	Com. Ind.	— —	170 180	— —	160 170	— —	150 160	— —	140 150	mA
I_{SB1}	TTL Standby Current (TTL Inputs)	V_{CC} = V_{CC} MAX., V_{IN} = V_{IH} or V_{IL} $\overline{CE}1 \geq V_{IH}$, f = 0 or CE2 ≤ V_{IL}, f = 0	Com. Ind.	— —	40 60	— —	40 60	— —	40 60	— —	40 60	mA
I_{SB2}	CMOS Standby Current (CMOS Inputs)	V_{CC} = V_{CC} MAX., $\overline{CE}1 \geq V_{CC}$ – 0.2V, CE2 ≤ 0.2V $V_{IN} > V_{CC}$ – 0.2V, or $V_{IN} \leq$ 0.2V, f = 0	Com. Ind.	— —	30 40	— —	30 40	— —	30 40	— —	30 40	mA

Note:
1. At f = f_{MAX}, address and data inputs are cycling at the maximum frequency, f = 0 means no input lines change.

IC61C1024L POWER SUPPLY CHARACTERISTICS[1] (Over Operating Range)

Symbol	Parameter	Test Conditions		-15 ns Min.	-15 ns Max.	-20 ns Min.	-20 ns Max.	-25 ns Min.	-25 ns Max.	Unit
I_{CC1}	Vcc Operating Supply Current	V_{CC} = V_{CC} MAX., $\overline{CE}$ = V_{IL} I_{OUT} = 0 mA, f = 0	Com. Ind.	— —	85 110	— —	85 110	— —	85 110	mA
I_{CC2}	Vcc Dynamic Operating Supply Current	V_{CC} = V_{CC} MAX., $\overline{CE}$ = V_{IL} I_{OUT} = 0 mA, f = f_{MAX}	Com. Ind.	— —	160 170	— —	150 160	— —	140 150	mA
I_{SB1}	TTL Standby Current (TTL Inputs)	V_{CC} = V_{CC} MAX, V_{IN} = V_{IH} or V_{IL} $\overline{CE}1 \geq V_{IH}$, f = 0 or CE2 ≤ V_{IL}, f = 0	Com. Ind.	— —	40 60	— —	40 60	— —	40 60	mA
I_{SB2}	CMOS Standby Current (CMOS Inputs)	V_{CC} = V_{CC} MAX., $\overline{CE}1 \geq V_{CC}$ – 0.2V, CE2 ≤ 0.2V $V_{IN} > V_{CC}$ – 0.2V, or $V_{IN} \leq$ 0.2V, f = 0	Com. Ind.	— —	500 750	— —	500 750	— —	500 750	µA

Note:
1. At f = f_{MAX}, address and data inputs are cycling at the maximum frequency, f = 0 means no input lines change.

READ CYCLE SWITCHING CHARACTERISTICS[1] (Over Operating Range)

Symbol	Parameter	-12[2] Min.	-12[2] Max.	-15 ns Min.	-15 ns Max.	-20 ns Min.	-20 ns Max.	-25 ns Min.	-25 ns Max.	Unit
t_{RC}	Read Cycle Time	12	—	15	—	20	—	25	—	ns
t_{AA}	Address Access Time	—	12	—	15	—	20	—	25	ns
t_{OHA}	Output Hold Time	3	—	3	—	3	—	3	—	ns
t_{ACE1}	$\overline{CE}1$ Access Time	—	12	—	15	—	20	—	25	ns
t_{ACE2}	CE2 Access Time	—	12	—	15	—	20	—	25	ns
t_{DOE}	$\overline{OE}$ Access Time	—	6	—	7	—	9	—	9	ns
t_{LZOE}[3]	$\overline{OE}$ to Low-Z Output	0	—	0	—	0	—	0	—	ns
t_{HZOE}[3]	$\overline{OE}$ to High-Z Output	0	6	0	6	0	7	0	10	ns
t_{LZCE1}[3]	$\overline{CE}1$ to Low-Z Output	2	—	2	—	3	—	3	—	ns
t_{LZCE2}[3]	CE2 to Low-Z Output	2	—	2	—	3	—	3	—	ns
t_{HZCE}[3]	$\overline{CE}1$ or CE2 to High-Z Output	0	7	0	8	0	9	0	10	ns
t_{PU}[4]	$\overline{CE}1$ or CE2 to Power-Up	0	—	0	—	0	—	0	—	ns
t_{PD}[4]	$\overline{CE}1$ or CE2 to Power-Down	—	12	—	12	—	18	—	20	ns

Notes:
1. Test conditions assume signal transition times of 3 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V and output loading specified in Figure 1.
2. -12 ns device for IC61C1024 only.
3. Tested with the load in Figure 2. Transition is measured ±500 mV from steady-state voltage. Not 100% tested.
4. Not 100% tested.

AC TEST CONDITIONS

Parameter	Unit
Input Pulse Level	0V to 3.0V
Input Rise and Fall Times	3 ns
Input and Output Timing and Reference Level	1.5V
Output Load	See Figures 1 and 2

AC TEST LOADS

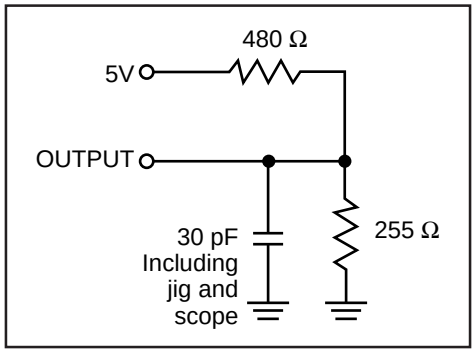


Figure 1

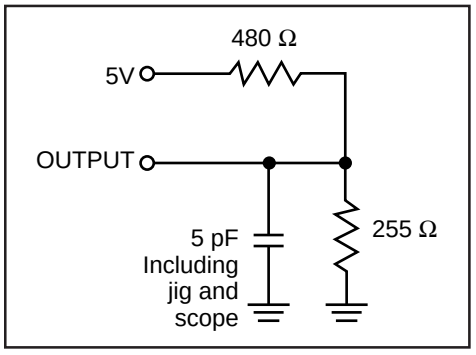
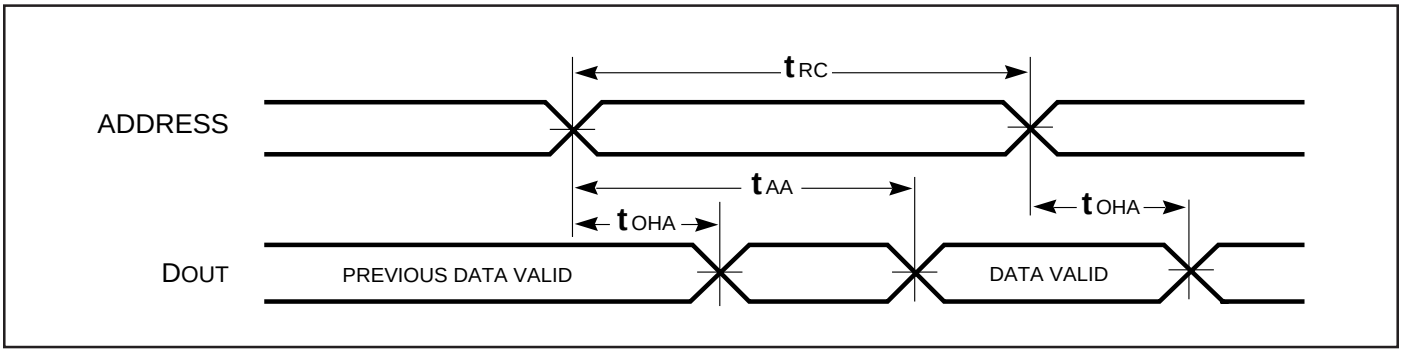


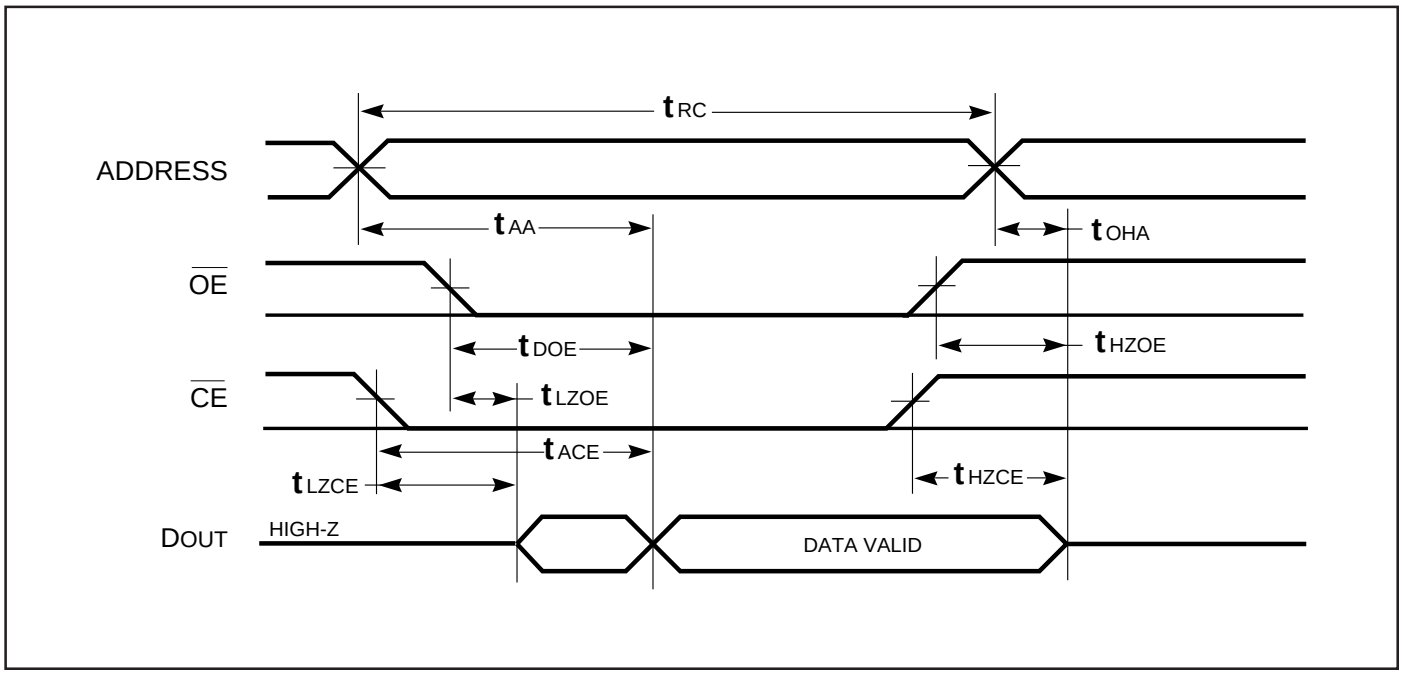
Figure 2

AC WAVEFORMS

READ CYCLE NO. 1[1,2]



READ CYCLE NO. 2[1,3]



Notes:
1. $\overline{WE}$ is HIGH for a Read Cycle.
2. The device is continuously selected. $\overline{OE}$, $\overline{CE1}$ = V_{IL}, CE2 = V_{IH}.
3. Address is valid prior to or coincident with $\overline{CE1}$ LOW and CE2 HIGH transitions.

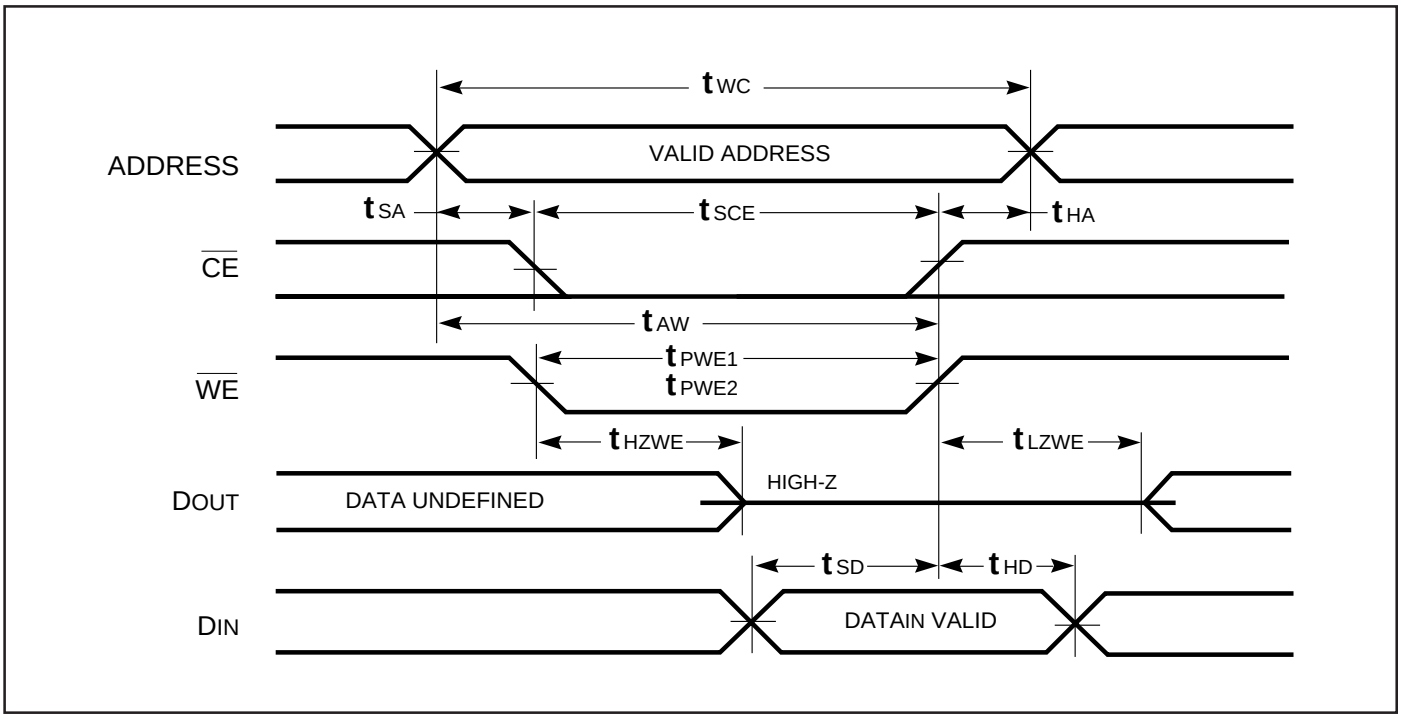
WRITE CYCLE SWITCHING CHARACTERISTICS[1,2] (Over Operating Range, Standard and Low Power)

		-12 ns[3]		-15 ns		-20 ns		-25 ns		
Symbol	Parameter	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Unit
t_{WC}	Write Cycle Time	12	—	15	—	20	—	25	—	ns
t_{SCE1}	$\overline{CE}$1 to Write End	10	—	12	—	15	—	20	—	ns
t_{SCE2}	CE2 to Write End	10	—	12	—	15	—	20	—	ns
t_{AW}	Address Setup Time to Write End	10	—	12	—	15	—	20	—	ns
t_{HA}	Address Hold from Write End	0	—	0	—	0	—	0	—	ns
t_{SA}	Address Setup Time	0	—	0	—	0	—	0	—	ns
t_{PWE}[4]	$\overline{WE}$ Pulse Width	10	—	10	—	12	—	15	—	ns
t_{SD}	Data Setup to Write End	7	—	8	—	10	—	12	—	ns
t_{HD}	Data Hold from Write End	0	—	0	—	0	—	0	—	ns
t_{HZWE}[5]	$\overline{WE}$ LOW to High-Z Output	—	7	—	7	—	10	—	12	ns
t_{LZWE}[5]	$\overline{WE}$ HIGH to Low-Z Output	2	—	2	—	2	—	2	—	ns

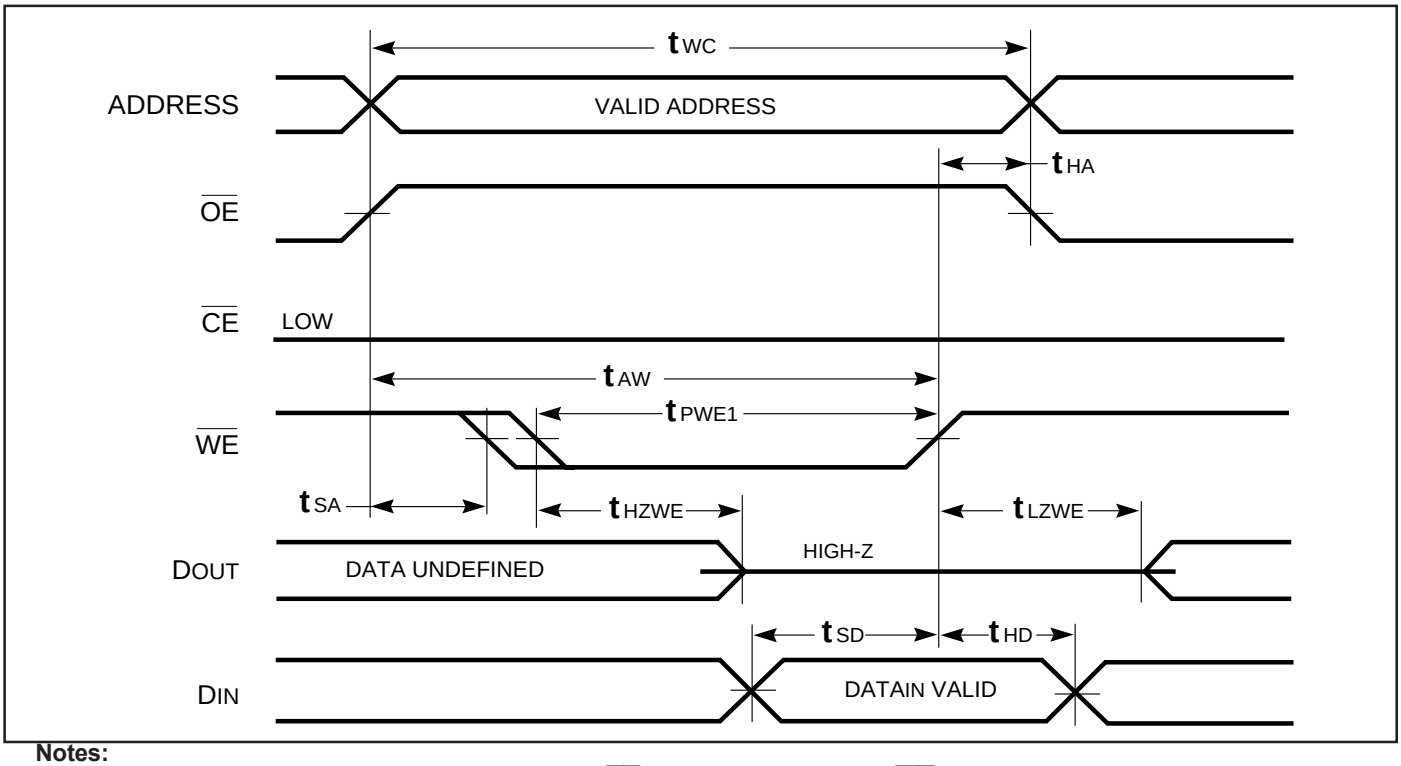
Notes:
1. Test conditions assume signal transition times of 5 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V and output loading specified in Figure 1.
2. The internal write time is defined by the overlap of $\overline{CE}$1 LOW, CE2 HIGH and $\overline{WE}$ LOW. All signals must be in valid states to initiate a Write, but any one can go inactive to terminate the Write. The Data Input Setup and Hold timing are referenced to the rising or falling edge of the signal that terminates the Write.
3. -12 ns device for IC61C1024 only.
4. Tested with $\overline{OE}$ HIGH.
5. Tested with the load in Figure 2. Transition is measured ±500 mV from steady-state voltage. Not 100% tested.

AC WAVEFORMS

WRITE CYCLE NO. 1 ($\overline{CE}$ Controlled, $\overline{OE}$ is HIGH or LOW) (1)



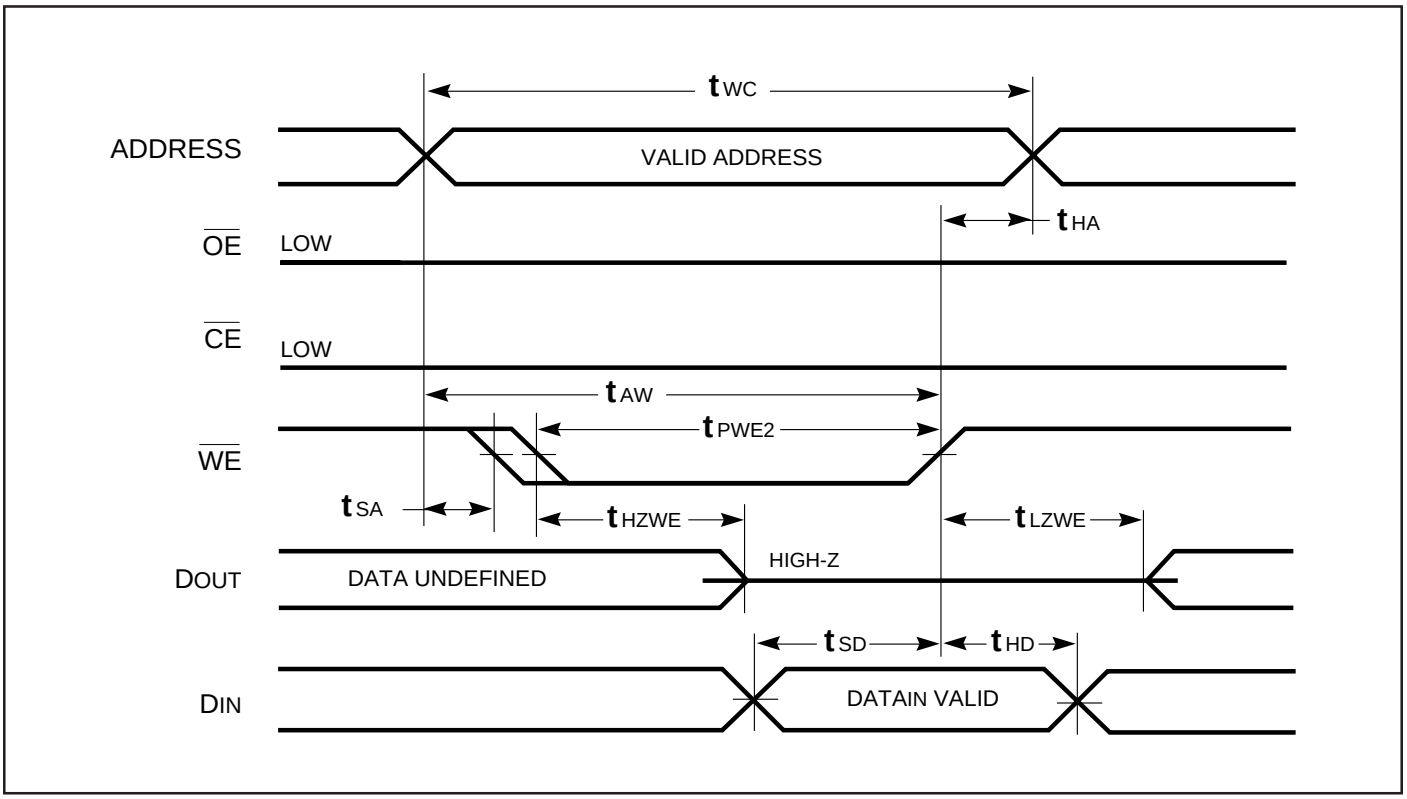
WRITE CYCLE NO. 2 ($\overline{OE}$ is HIGH During Write Cycle) (1,2)



Notes:

1. The internal write time is defined by the overlap of $\overline{CE}$1 LOW, CE2 HIGH and $\overline{WE}$ LOW. All signals must be in valid states to initiate a Write, but any one can go inactive to terminate the Write. The Data Input Setup and Hold timing are referenced to the rising or falling edge of the signal that terminates the Write.
2. I/O will assume the High-Z state if $\overline{OE}$ = V_{IH}.

WRITE CYCLE NO. 3 ($\overline{OE}$ is LOW During Write Cycle) [1]



IC61C1024 STANDARD VERSION ORDERING INFORMATION
Commercial Range: 0°C to +70°C

Speed (ns)	Order Part No.	Package
12	IC61C1024-12J	300mil SOJ
12	IC61C1024-12K	400mil SOJ
12	IC61C1024-12H	8*13.4mm TSOP-1
12	IC61C1024-12T	8*20mm TSOP-1
15	IC61C1024-15J	300mil SOJ
15	IC61C1024-15K	400mil SOJ
15	IC61C1024-15H	8*13.4mm TSOP-1
15	IC61C1024-15T	8*20mm TSOP-1
20	IC61C1024-20J	300mil SOJ
20	IC61C1024-20K	400mil SOJ
20	IC61C1024-20H	88*13.4mm TSOP-1
20	IC61C1024-20T	8*20mm TSOP-1
25	IC61C1024-25J	300mil SOJ
25	IC61C1024-25K	400mil SOJ
25	IC61C1024-25H	8*13.4mm TSOP-1
25	IC61C1024-25T	8*20mm TSOP-1

IC61C1024 STANDARD VERSION ORDERING INFORMATION
Industrial Range: –40°C to +85°C

Speed (ns)	Order Part No.	Package
12	IC61C1024-12JI	300mil SOJ
12	IC61C1024-12KI	400mil SOJ
12	IC61C1024-12HI	8*13.4mm TSOP-1
12	IC61C1024-12TI	8*20mm TSOP-1
15	IC61C1024-15JI	300mil SOJ
15	IC61C1024-15KI	400mil SOJ
15	IC61C1024-15HI	8*13.4mm TSOP-1
15	IC61C1024-15TI	8*20mm TSOP-1
20	IC61C1024-20JI	300mil SOJ
20	IC61C1024-20KI	400mil SOJ
20	IC61C1024-20HI	8*13.4mm TSOP-1
20	IC61C1024-20TI	8*20mm TSOP-1
25	IC61C1024-25JI	300mil SOJ
25	IC61C1024-25KI	400mil SOJ
25	IC61C1024-25HI	8*13.4mm TSOP-1
25	IC61C1024-25TI	8*20mm TSOP-1

IC61C1024L LOW POWER VERSION ORDERING INFORMATION
Commercial Range: 0°C to +70°C

Speed (ns)	Order Part No.	Package
15	IC61C1024L-15J	300mil SOJ
	IC61C1024L-15K	400mil SOJ
	IC61C1024L-15H	8*13.4mm TSOP-1
	IC61C1024L-15T	8*20mm TSOP-1
20	IC61C1024L-20J	300mil SOJ
	IC61C1024L-20K	400mil SOJ
	IC61C1024L-20H	8*13.4mm TSOP-1
	IC61C1024L-20T	8*20mm TSOP-1
25	IC61C1024L-25J	300mil SOJ
	IC61C1024L-25K	400mil SOJ
	IC61C1024L-25H	8*13.4mm TSOP-1
	IC61C1024L-25T	8*20mm TSOP-1

IC61C1024L LOW POWER VERSION ORDERING INFORMATION
Industrial Range: –40°C to +85°C

Speed (ns)	Order Part No.	Package
15	IC61C1024L-15JI	300mil SOJ
	IC61C1024L-15KI	400mil SOJ
	IC61C1024L-12HI	8*13.4mm TSOP-1
	IC61C1024L-15TI	8*20mm TSOP-1
20	IC61C1024L-20JI	300mil SOJ
	IC61C1024L-20KI	400mil SOJ
	IC61C1024L-12HI	8*13.4mm TSOP-1
	IC61C1024L-20TI	8*20mm TSOP-1
25	IC61C1024L-25JI	300mil SOJ
	IC61C1024L-25KI	400mil SOJ
	IC61C1024L-12HI	8*13.4mm TSOP-1
	IC61C1024L-25TI	8*20mm TSOP-1

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