

**ICPL2730
ICPL2731**

HIGH SPEED DUAL CHANNEL OPTICALLY COUPLED ISOLATOR PHOTODARLINGTON OUTPUT

APPROVALS

- UL recognised, File No. E91231

DESCRIPTION

These dual channel diode-darlington optocouplers use a pair of light emitting diodes and an integrated high gain photon detectors to provide 2500Volts RMS electrical isolation between input and output.

Separate connection for the photodiode bias and output darlington collector improve the speed up to a hundred times that of a conventional photodarlington coupler by reducing the base-collector capacitance.

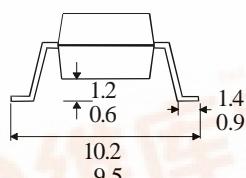
FEATURES

- High speed - DC to 200kBits/s operation
- High Common Mode Transient Immunity 10kV/ μ s typical
- TTL Compatible - 0.1V V_{OL} typical
- Low Input Current Requirement - 0.5mA
- High Current Transfer Ratio - 2000% typ.
- Open Collector Output
- 2500V RMS Withstand Test Voltage, 1 min
- ICPL2731 has improved noise shield which gives superior common mode rejection
- Options :-
10mm lead spread - add G after part no.
Surface mount - add SM after part no.
Tape&reel - add SMT&R after part no.
- All electrical parameters 100% tested
- Custom electrical selections available

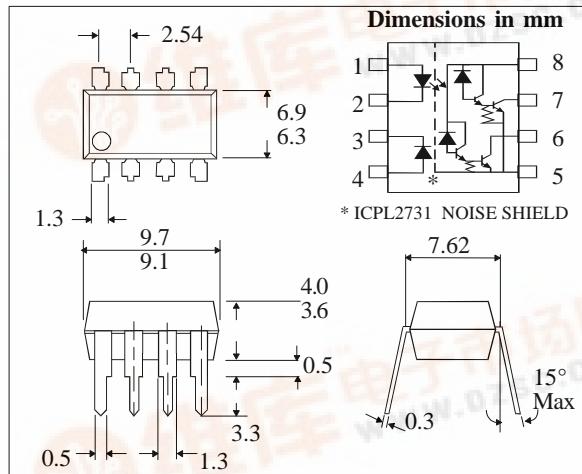
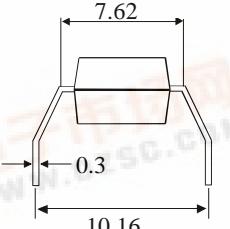
APPLICATIONS

- Line receivers
- Digital logic ground isolation
- Telephone ring detector
- Current loop receiver

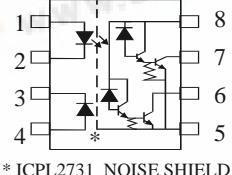
OPTION SM SURFACE MOUNT



OPTION G



Dimensions in mm



ABSOLUTE MAXIMUM RATINGS (25°C unless otherwise specified)

Storage Temperature _____ -55°C to + 125°C
Operating Temperature _____ -40°C to + 85°C
Lead Soldering Temperature
(1/16 inch (1.6mm) from case for 10 secs) 260°C

INPUT DIODE

Average Forward Current _____ 20mA (1)
Peak Forward Current _____ 40mA
(50% duty cycle, 1ms pulse width)
Reverse Voltage _____ 5V
Power Dissipation _____ 35mW(2)

DETECTOR

Output Current	60mA (3)
Supply and Output Voltage	
ICPL2730	-0.5 to +7V
ICPL2731	-0.5 to +18V
Power Dissipation	100mW (4)

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ELECTRICAL CHARACTERISTICS ($T_A = 0^\circ\text{C}$ to 70°C , $V_{CC} = 4.5\text{V}$ Unless otherwise noted)

PARAMETER	SYM	DEVICE	MIN	TYP*	MAX	UNITS	TEST CONDITION
Current Transfer Ratio (note 5, 6)	CTR	ICPL2731	400	2000		%	$I_F = 0.5\text{mA}, V_O = 0.4\text{V}$
		ICPL2731	500	2000		%	$I_F = 1.6\text{mA}, V_O = 0.4\text{V}$
		ICPL2730	300	2000		%	$I_F = 1.6\text{mA}, V_O = 0.4\text{V}$
Logic Low Output Voltage (note 5)	V_{OL}	ICPL2731		0.1	0.4	V	$I_F = 0.5\text{mA}, I_O = 2\text{mA}$
		ICPL2731		0.1	0.4	V	$I_F = 1.6\text{mA}, I_O = 8\text{mA}$
		ICPL2731		0.1	0.4	V	$I_F = 5\text{mA}, I_O = 15\text{mA}$
		ICPL2731		0.1	0.4	V	$I_F = 12\text{mA}, I_O = 24\text{mA}$
		ICPL2730		0.1	0.4	V	$I_F = 1.6\text{mA}, I_O = 4.8\text{mA}$
Logic High Output Current (note 5)	I_{OH}	ICPL2731		0.01	100	μA	$I_F = 0\text{mA}$ $V_O = V_{CC} = 18\text{V}$
		ICPL2730		0.01	100	μA	$I_F = 0\text{mA}$ $V_O = V_{CC} = 7\text{V}$
Logic Low Supply Current	I_{CCL}	ICPL2731		0.5		mA	$I_{FI} = I_{F2} = 1.6\text{mA}, V_{CC} = 18\text{V}$ $V_{OI} = V_{O2} = \text{open}$
		ICPL2730		0.4		mA	$I_{FI} = I_{F2} = 1.6\text{mA}, V_{CC} = 7\text{V}$ $V_{OI} = V_{O2} = \text{open}$
Logic High Supply Current	I_{CCH}	ICPL2731		5		nA	$I_{FI} = I_{F2} = 0\text{mA}, V_{CC} = 18\text{V}$ $V_{OI} = V_{O2} = \text{open}$
		ICPL2730		4		nA	$I_{FI} = I_{F2} = 0\text{mA}, V_{CC} = 18\text{V}$ $V_{OI} = V_{O2} = \text{open}$
Input Forward Voltage (note 5)	V_F			1.45	1.7	V	$I_F = 1.6\text{mA}, T_A = 25^\circ\text{C}$
Temperature Coefficient of Forward Voltage (note 5)	$\frac{\Delta V_F}{\Delta T_A}$			-1.8		mV/ $^\circ\text{C}$	$I_F = 1.6\text{mA}$
Input Reverse Voltage (note 5)	V_R		5			V	$I_R = 10\mu\text{A}, T_A = 25^\circ\text{C}$
Input Capacitance (note 5)	C_{IN}			60		pF	$f = 1\text{MHz}, V_F = 0$
Input-output Isolation Voltage (note 10)	V_{ISO}		2500	5000		V_{RMS}	R.H.equal to or less than 50%, t = 1min. $T_A = 25^\circ\text{C}$
Resistance (Input to Output) (note 10)	R_{I-O}			10^{12}		Ω	$V_{I-O} = 500\text{V dc}$
Capacitance (Input to Output) (note 10)	C_{I-O}			0.6		pF	$f = 1\text{MHz}$
Input-Input Insulation (note 7)	I_{I-I}			0.005		μA	R.H.equal to or less than 50%, t = 5sec. $V_{I-I} = 500\text{DC}$
Resistance (Input to Input) (note 7)	R_{I-I}			10^{11}		Ω	$V_{I-I} = 500\text{V dc}$
Capacitance (Input to Input) (note 7)	C_{I-I}			0.25		pF	$f = 1\text{MHz}$

* All typicals at $T_A = 25^\circ\text{C}$

SWITCHING SPECIFICATIONS AT $T_A = 25^\circ\text{C}$ ($V_{CC} = 5\text{V}$ Unless otherwise noted)

PARAMETER	SYM	DEVICE	MIN	TYP	MAX	UNITS	TEST CONDITION
Propagation Delay Time to Logic Low at Output (fig 1)(note 5)	t_{PHL}	ICPL2731 ICPL2730/1 ICPL2730/1		25 0.5 4.0	100 2 20	μs μs μs	$I_F = 0.5\text{mA}, R_L = 4.7\text{k}\Omega$ $I_F = 12\text{mA}, R_L = 270\Omega$ $I_F = 1.6\text{mA}, R_L = 2.2\text{k}\Omega$
Propagation Delay Time to Logic High at Output (fig 1)(note 5)	t_{PLH}	ICPL2731 ICPL2730/1 ICPL2730/1		20 4 12	60 10 35	μs μs μs	$I_F = 0.5\text{mA}, R_L = 4.7\text{k}\Omega$ $I_F = 12\text{mA}, R_L = 270\Omega$ $I_F = 1.6\text{mA}, R_L = 2.2\text{k}\Omega$
Common Mode Transient Immunity at Logic High Level Output (fig 2)(note 9)	CM_H		1000	10000		V/ μs	$I_F = 0\text{mA}, V_{CM} = 10\text{V}_{PP}$ $R_L = 2.2\text{k}\Omega$
Common Mode Transient Immunity at Logic Low Level Output (fig 2)(note 8)	CM_L		-1000	-10000		V/ μs	$I_F = 1.6\text{mA}, V_{CM} = 10\text{V}_{PP}$ $R_L = 2.2\text{k}\Omega$

NOTES:-

- Derate linearly above 70°C free air temperature at a rate of $0.5 \text{ mA}/^\circ\text{C}$.
- Derate linearly above 70°C free air temperature at a rate of $0.9 \text{ mW}/^\circ\text{C}$.
- Derate linearly above 70°C free air temperature at a rate of $0.6 \text{ mA}/^\circ\text{C}$.
- Derate linearly above 35°C free air temperature at a rate of $1.7 \text{ mW}/^\circ\text{C}$.
Output power = (Collector output) + (Supply output).
- Each channel.
- CURRENT TRANSFER RATIO is defined as the ratio of output collector current, I_O , to the forward LED input current, I_F times 100%.
- Measured between pins 1 and 2 shorted together, and pins 3 and 4 shorted together.
- Common mode transient immunity in Logic Low level is the maximum tolerable (negative) dV_{CM}/dt on the trailing edge of the common mode pulse signal, V_{CM} to assure that the output will remain in Logic Low state (i.e. $V_O < 0.8\text{V}$). Measured in volts per microsecond ($\text{V}/\mu\text{s}$).
- Common mode transient immunity in Logic High level is the maximum tolerable (positive) dV_{CM}/dt on the leading edge of the common mode pulse V_{CM} to assure that the output will remain in a Logic High state (i.e. $V_O > 2.0\text{V}$). Measured in volts per microsecond ($\text{V}/\mu\text{s}$).
- Device considered a two-terminal device: pins 1,2,3, and 4 shorted together and pins 5,6,7 and 8 shorted together.

FIG.1 SWITCHING TEST CIRCUIT

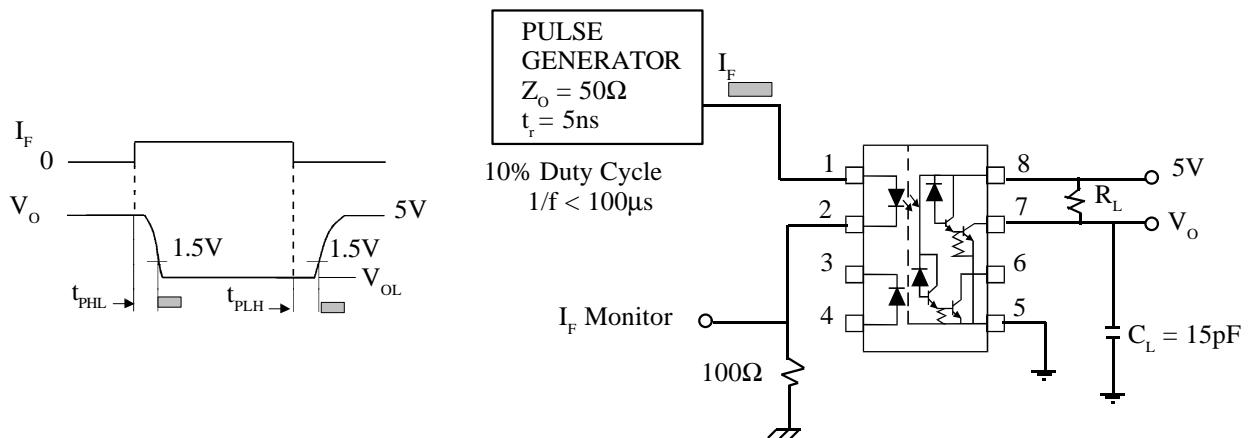


FIG. 2 TEST CIRCUIT FOR TRANSIENT IMMUNITY AND TYPICAL WAVEFORMS

