Integrated Circuit Systems, Inc.

Differential Output Video Dot Clock Generator

General Description

The **ICS1567** is a very high performance monolithic PLL frequency synthesizer. Utilizing ICS's advanced CMOS mixed-mode technology, the **ICS1567** provides a low cost solution for high-end video clock generation, and for telecom system clock generation.

The **ICS1567** has differential video clock outputs (CLK and $\overline{CLK}$) that are compatible with industry standard video DACs & RAMDACs. An additional clock output, $\overline{LD}$, is provided, whose frequency is divided down from the main clock by a programmable divider.

Operating frequencies are selectable from a pre-programmed (customer-defined) table. An on-chip crystal oscillator for generating the reference frequency is provided on the **ICS1567**.

Programming of the **ICS1567** is accomplished via frequency select pins on the package. The **ICS1567** has five lines plus a STROBE pin which permits selection of 32 frequencies. Reset of the pipeline delay on Brooktree RAMDACs is automatically performed on a rising edge of the STROBE line.

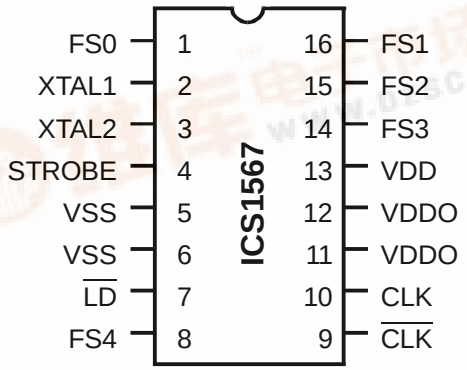
Features

- High frequency operation for extended video modes - up to 180 MHz
- Compatible with Brooktree high performance RAMDACs
  a) Differential output clocks with ECL logic levels
  b) Programmable divider modulus for load clock
  c) Circuitry included for automatic reset of Brooktree RAMDAC pipeline delay
- Low cost - eliminates need for multiple ECL crystal clock oscillators in video display systems
- Strobed/Transparent frequency select options
- 32-user selected mask-programmable frequencies
- Fast acquisition of selected frequencies, strobed or non-strobed
- Advanced PLL for low phase-jitter
- Dynamic control of VCO sensitivity providing optimized loop gain over entire frequency range
- Small footprint - 16-pin wide body (300 mil) SOIC

Applications

- Workstations
- High-resolution PC and MAC displays
- 8514A - TMS340X0 systems
- EGA - VGA - Super VGA video
- Telecom reference clock generation - suitable for Sonet, ATM and other data rates up to 155.52Mb.

Pin Configuration



16-Pin SOIC

Block Diagram

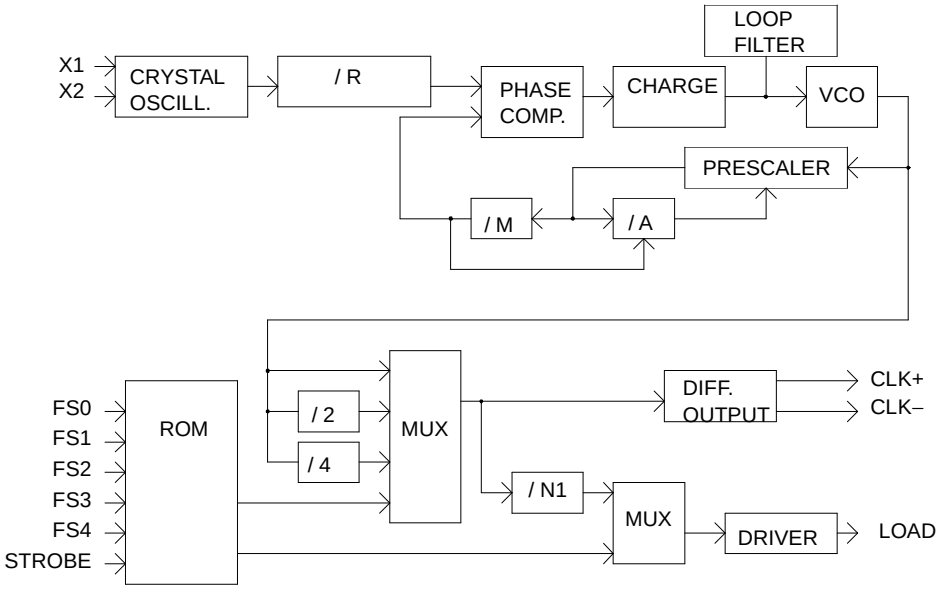


Figure 1

System Schematic

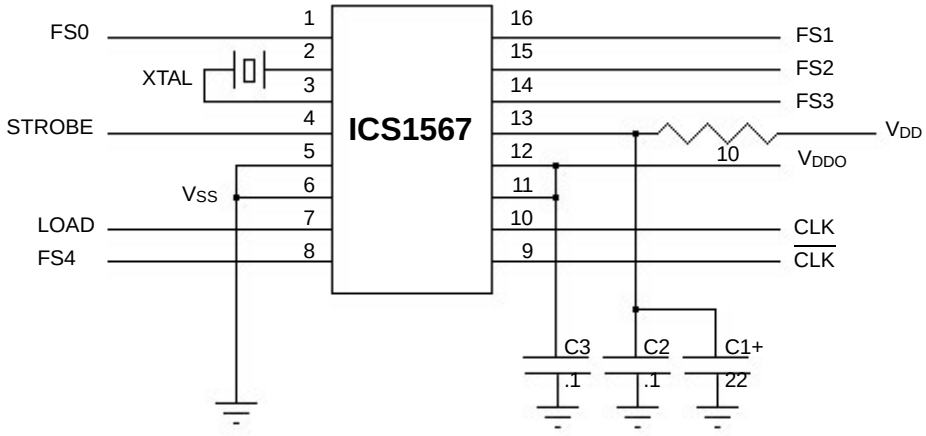
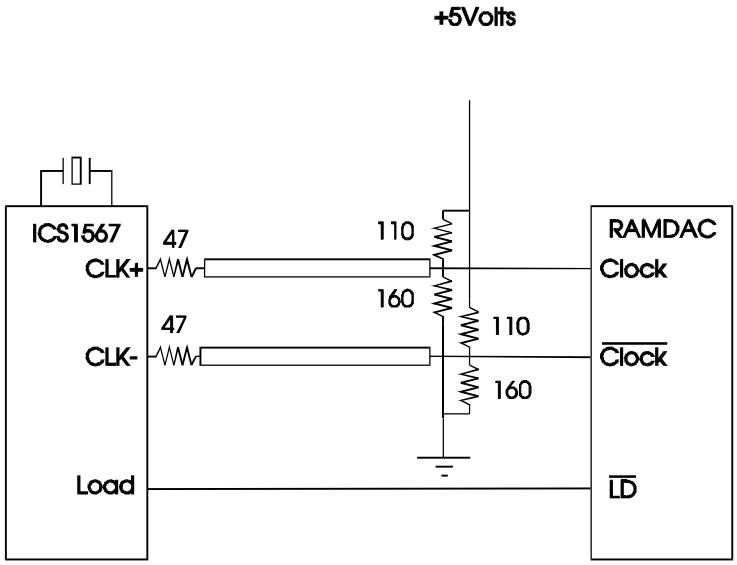


Figure 2

Typical Output Configuration



Notes:
CLK & $\overline{CLK}$ outputs are pseudo-ECL. Logic low level is set by the ratio of the resistors stacked across the power supply
V_{LO} = (V supply • 160)/(110 +160) in the example shown above.
The above values are a good starting point for RAMDAC or clock generator interface.

Figure 3

Pin Description

PIN NUMBER	PIN SYMBOL	TYPE	DESCRIPTION
1	• FS0	IN	Frequency Select LSB.
2	XTAL1	IN	Crystal Interface/External Oscillator Input.
3	XTAL2	OUT	Crystal Interface.
4	• STROBE	IN	Control For Frequency Select Latch, also performs automatic RAMDAC reset.
5	VSS	--	Device Ground (Both pins must be connected.)
6	VSS	--	Device Ground (Both pins must be connected.)
7	$\overline{LD}$	OUT	Load Output. This output is at CLK frequency divided by N1.
8	• FS4	IN	Frequency Select MSB.
9	$\overline{CLK}$	OUT	Clock Output Inverted.
10	CLK	OUT	Clock Output Non-Inverted.
11	VDDO	--	Output Stage Power (Both pins must be connected).
12	VDDO	--	Output Stage Power (Both pins must be connected).
13	VDD	--	PLL System Power.
14	• FS3	IN	Frequency Select.
15	• FS2	IN	Frequency Select.
16	• FS1	IN	Frequency Select.

• = inputs with internal pull-up resistor

Circuit Description

Overview

The **ICS1567** is designed to provide the graphics system clock signals required by industry standard RAMDACs. One of 32 pre-programmed (user-definable) frequencies may be selected under digital control. Fully programmable feedback and reference divider capability allow virtually any frequency to be generated, not just simple multiples of the reference frequency. The **ICS1567** uses the latest generation of frequency synthesis techniques developed by ICS and is completely suitable for the most demanding video applications.

Digital Inputs

The FS0-FS4 pins and the STROBE pin are used to select the desired operating frequency from the 32 pre-programmed frequencies in the ROM table of the **ICS1567**. The STROBE pin also controls activation of the pipeline delay RESET function included in the **ICS1567** (see PIPELINE DELAY RESET section for details). The FS0-FS4 and STROBE pins are each equipped with a pull-up and will be at a logic HIGH level when not connected.

Transparent Mode - When the STROBE pin is held HIGH, the FS0 through FS4 inputs are transparent; that is, they directly access the ROM table. The synthesizer will output the frequency programmed into the location addressed by the FS0-FS4 pins.

Latched Mode - When the STROBE pin is held LOW, the FS0-FS4 pins are ignored. The synthesizer will output the frequency corresponding to the state of the FS0-FS4 pins when the STROBE pin was last HIGH. In the event that the **ICS1567** is powered-up with the STROBE pin held LOW, the synthesizer will output the frequency programmed into address 0 (i.e., the one selected with FS0 through FS4 at a logic LOW level).

Frequency Synthesizer Description

Refer to Figure 1 for a block diagram of the **ICS1567**. The reference frequency is generated by an on-chip crystal oscillator, or the reference frequency may be applied to the **ICS1567** from an external frequency source.

The **ICS1567** generates its output frequencies using phase-locked loop techniques. The phase-locked loop (or PLL) is a closed-loop feedback system that drives the output frequency to be ratiometrically related to the reference frequency provided to the PLL. The phase-frequency detector shown in the block diagram drives the VCO to a frequency that will cause the two inputs to the phase-frequency detector to be matched in frequency and phase. This occurs when:

$$F(vco) = \frac{F(XTAL1) \bullet \text{Feedback Divider}}{\text{Reference Divider}}$$

This expression is exact; that is, the accuracy of the output frequency depends solely on the reference frequency provided to the part (assuming correctly-programmed dividers). The divider programming is one of the functions performed by the ROM look-up table in the **ICS1567**. The VCO gain is also ROM programmable which permits the **ICS1567** to be optimized for best performance at each frequency in the table.

The feedback divider makes use of a dual-modulus prescaler technique that allows construction of a programmable counter to operate at high speeds while still allowing the feedback divider to be programmed in steps of 1. This is an improvement over conventional fixed prescaler architectures that typically impose a factor-of-four penalty (or larger) in this respect.

A post-divider may be inserted between the VCO and the CLK and $\overline{\text{CLK}}$ outputs of the **ICS1567**. This is useful in generation of lower frequencies, as the VCO has been optimized for high-frequency operation. Different post-divider settings may be used for each frequency in the table.

Load Clock Divider

The **ICS1567** has an additional programmable divider that is used to generate the LOAD frequency. The modulus of this divider may be set to 3, 4, 5, 6, 8, or 10. The design of this divider permits the output duty factor to be 50/50, even when an odd modulus is selected.

The selection of the modulus is done by the ROM look-up table. A different modulus may, therefore, be selected for each frequency address.

Pipeline Delay Reset Function

The **ICS1567** implements the clocking sequence required to reset the pipeline delay on Brooktree RAMDACs. This sequence is automatically generated by the **ICS1567** upon any rising edge of the STROBE line.

When the frequency select inputs (FS0-FS4) are used in a transparent mode, simply lower and raise the STROBE line to activate the function. When the frequency select inputs are latched, simply load the same frequency into the **ICS1567** twice.

When changing frequencies, it is advisable to allow 500uSec after the new frequency is selected to activate the reset function. The output frequency of the synthesizer should be stable enough at that point for the RAMDAC to correctly execute its reset sequence.

See Figure 4 for a diagram of the clock sequencing.

Output Stage Description

The CLK and $\overline{\text{CLK}}$ outputs are each connected to the drains of P-Channel MOSFET devices. The source of each of these devices is connected to VDDO. Typical on resistance of each device is 15 Ohms. These outputs will drive the clock and $\overline{\text{clock}}$ of a RAMDAC device when a resistive network equivalent to Figure 3 is utilized.

The $\overline{\text{LD}}$ output is a high-current CMOS type drive whose frequency is controlled by a programmable divider that may be selected for a modulus of 3, 4, 5, 6, 8, or 10. Under control of the ROM, this output may also be suppressed (logic low level) at any frequency select address, if desired.

Application Information

Power Supplies

The **ICS1567** has two VSS pins to reduce the effects of package inductance. Both pins are connected to the same potential on the die (the ground bus). BOTH of these pins should connect to the ground plane of the video board as close to the package as is possible.

The **ICS1567** has two VDDO pins which are the supply of +5 volt power to all output stages. Again, both VDDO pins connect to the same point on the die. BOTH of these pins should be connected to the power plane (or bus) using standard high-frequency decoupling practice. This decoupling consists of a low series inductance bypass capacitor, using the shortest leads possible, mounted close to the **ICS1567**.

The VDD pin is the power supply for the synthesizer circuitry and other lower current digital functions. We recommend that RC decoupling or zener regulation be provided for this pin (as shown in the recommended application circuitry). This will allow the PLL to "track" through power supply fluctuations without visible effects.

Crystal Oscillator and Crystal Selection

The **ICS1567** has circuitry on-board to implement a Pierce oscillator with the addition of only one external component, a quartz crystal. Pierce oscillators operate the crystal in anti- (also called parallel-) resonant mode. See the AC Characteristics for the effective capacitive loading to specify when ordering crystals.

So-called series-resonant crystals may also be used with the **ICS1567**. Be aware that the oscillation frequency will be slightly higher than the frequency that is stamped on the can (typically 0.005-0.01%).

As the entire operation of the phase-locked loop depends on having a stable reference frequency, we recommend that the crystal be mounted as closely as possible to the package. Avoid routing digital signals or the **ICS1567** outputs underneath or near these traces. It is also desirable to ground the crystal can to the ground plane, if possible.

Application Notes *(continued)*

Bus Clock Interface

In some applications, it may be desirable to utilize the bus clock. To do this, connect the clock through a .047uF capacitor to XTAL1 (2) and keep the lead length of the capacitor to XTAL1 (2) to a minimum to reduce noise susceptibility. This input is internally biased at VDD/2. Since TTL compatible clocks typically exhibit a VOH of 3.5V, capacitively coupling the input restores noise immunity. The **ICS1567** is not sensitive to the duty cycle of the bus clock; however, the quality of this signal varies considerably with different motherboard designs. As the quality of the bus clock is typically outside the control of the graphics adapter card manufacturer, it is suggested that this signal be buffered on the graphics adapter board. XTAL2 (3) must be left open in this configuration.

ICS1567 Interface

The **ICS1567** should be located as close as possible to the video DAC or RAMDAC. Figure 3 illustrates interfacing the **ICS1567** to a RAMDAC. The differential output CLOCK drivers are current sourcing only and are designed to drive resistive terminations in a complementary fashion CLK and $\overline{CLK}$ connections should follow good ECL interconnection practice. Terminating resistors should be as close as possible to the RAMDAC.

Absolute Maximum Ratings

Ambient Temeperature under bias	T_o	0°C to 70°C
Supply Voltage	V_{DD}	-0.5V to +7V
Input Voltage	V_{IN}	-0.5V to V_{DD} + 0.5V
Output Voltage	V_{OUT}	-0.5V to V_{DD} + 0.5V
Clamp Diode Current	V_{IK} & I_{OK}	±30mA
Output Current per Pin	I_{OUT}	±50mA
Storage Temperature	T_S	-85°C to + 150°C
Power Dissipation	P_D	500mW

Values beyond these ratings may damage the device. This device contains circuitry to protect the inputs and outputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid applications of any voltage higher than the maximum rated voltages. For proper operation, it is recommended that V_{IN} and V_{OUT} be constrained to > = V_{SS} and < = V_{DD}.

Standard Test Conditions

The characteristics below apply for the following standard test conditions, unless otherwise noted. All voltages are referenced to VSS (OV Ground). Positive current flows into the referenced pin.

Operating Temperature range	0°C to 70°C
Power supply voltage	4.75 to 5.25 Volts

DC Characteristics

PARAMETER	SYMBOL	MIN	MAX	UNITS	CONDITIONS
Input High Voltage	V_{IH}	2.0	V_{DD} + 0.5	V	
Input Low Voltage	V_{IL}	V_{SS} -0.5	0.8	V	
Input High Current	I_{IH}		10	uA	$V_{IN} = V_{DD}$
Input Low Current	I_{IL}		-200	uA	$V_{IN} = V_{SS}$
LOAD OUTPUT					
Output High Voltage	V_{OH}	2.4		V	I_{OH} = -4.0 mA
Output Low Voltage	V_{OL}		0.4	V	I_{OL} = 6.0 mA
CLOCK OUTPUTS					
Differential Output Voltage (CLK-$\overline{CLK}$)	V_{OD}	1.2		V	See Figure 4
XTAL1 INPUT					
Input High Voltage	V_{XH}	3.75	V_{DD} + 0.5	V	
Input Low Voltage	V_{XL}	VSS -0.5	1.25	V	
Operating Current	I_{DD}		50	mA	Outputs Unloaded
Input Pin Capacitance	C_{IN}		8	pF	F_C = 1 MHz
Output Pin Capacitance	C_{OUT}		12	pF	F_C = 1 MHz

AC Characteristics

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
CLK and $\overline{CLK}$ TIMING						
Duty Cycle	T_{HIGH}	40		60	%	3, 4, 9
Frequency Error				0.5	%	
Rise Time	T_r			2	ns	5, 9
Fall Time	T_f			2	ns	5, 9
VCO Frequency	F_{VCO}	20		180	MHz	1
PLL Acquire Time	T_{LOCK}		500		uS	
LD* TIMING						
Duty Cycle	T_{HIGH}	40		60	%	6
Load Frequency	F_{LOAD}			60	MHz	
Rise Time	T_r			2	ns	7, 8
Fall Time	T_f			2	ns	7, 8
REFERENCE INPUT CLOCK						
Crystal Frequency	F_{XTAL}	5		20	MHz	
Crystal Oscillator Loading Capacitance	C_{PAR}		20		pF	
XTAL1 High Time	T_{XHI}	8			ns	2
XTAL1 Low Time	T_{XLO}	8			ns	2
Rise Time	T_r			10	ns	2, 7
Fall Time	T_f			10	ns	2, 7
DIGITAL INPUTS						
Frequency Select Setup Time	1	10			ns	10
Frequency Select Hold Time	2	10			ns	10
Strobe Pulse Width	3	20			ns	10
PIPELINE DELAY RESET						
Reset Activation	4			$2*T_{CLK}$	ns	10
Reset Duration	5	$4*T_{CLK}$			ns	10
Restart Delay	6	$-1*T_{CLK}$		$+1.5*T_{CLK}$	ns	10

Notes:

1. Use of the post-divider is required for frequencies lower than 20 MHz on CLK and $\overline{CLK}$ outputs. Use of the post-divider is recommended for output frequencies lower than 65 MHz.
2. Values for XTAL1 driven by an external clock
3. Duty Cycle for Differential Output (CLK- $\overline{CLK}$)
4. Duty cycle measured at VOD/2 for Differential CLK Output
5. Rise and fall time between 20% and 80% of VOD
6. Duty cycle measured at 1.4V for TTL I/O
7. Rise and fall time between 0.8 and 2.0 VDC for TTL I/O
8. Output pin loading = 15 pF
9. See Figure 3.
10. See Figure 4.

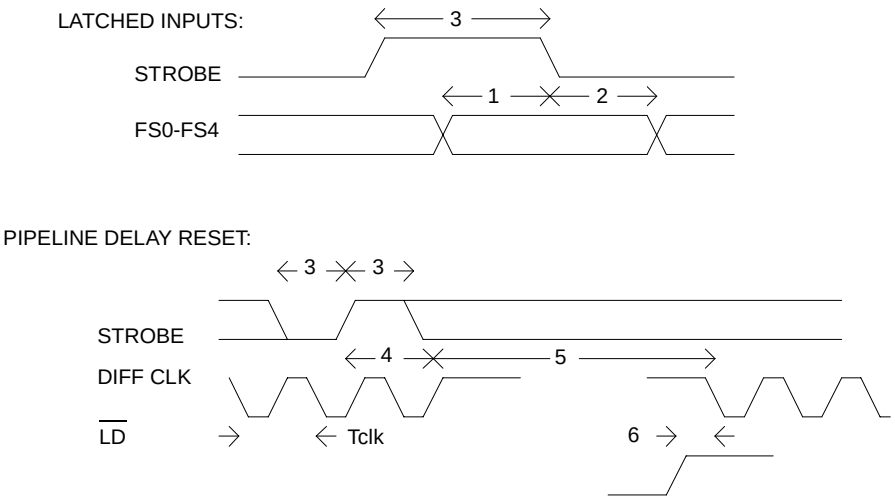

LATCHED INPUTS:
3
STROBE
1
2
FS0-FS4
PIPELINE DELAY RESET:
3
3
STROBE
4
5
DIFF CLK
LD
Tclk
6

Figure 4

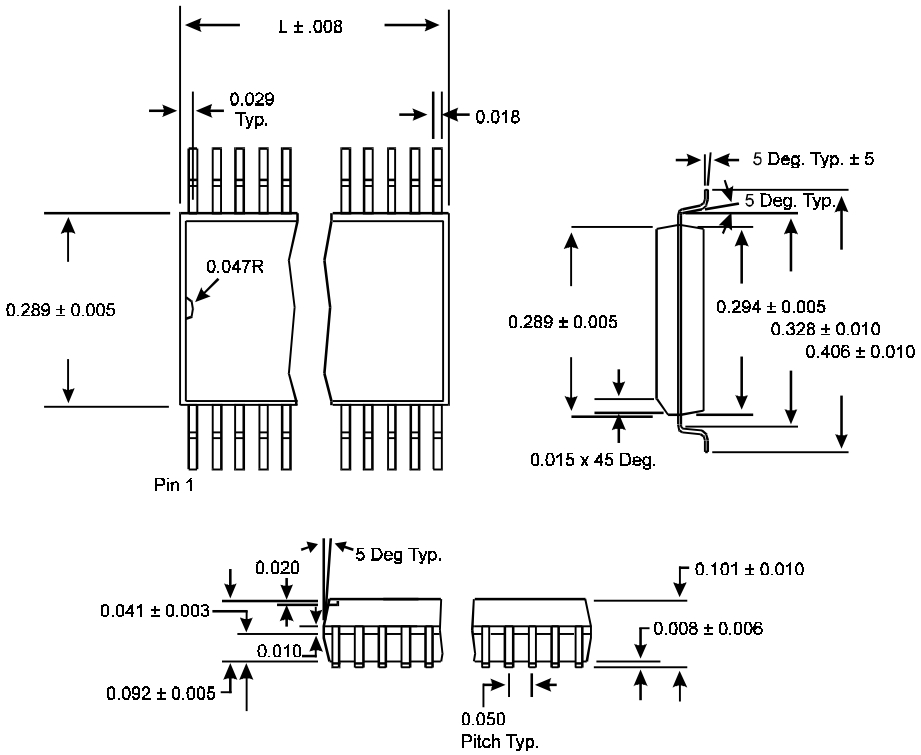
ICS1567 Pattern Request Form

Custom patterns are also available, although a significant volume commitment and/or one-time mask charge will apply. Contact ICS Sales for details.

ICS Part Number	ICS1567-742	ICS1567-Custom Pattern #1
Video Clock Address (HEX)	Frequency (MHz)	Frequency (MHz)
0	112.000	
1	148.000	
2	OFF	
3	135.000	
4	31.500	
5	105.500	
6	78.000	
7	86.000	
8	108.000	
9	120.000	
10	128.000	
11	93.000	
12	112.000	
13	148.000	
14	135.000	
15	89.210	
16	105.500	
17	112.000	
18	25.000	
19	45.000	
20	64.000	
21	75.000	
22	78.000	
23	86.000	
24	103.000	
25	108.000	
26	120.000	
27	127.000	
28	128.000	
29	135.000	
30	112.000	
31	148.000	

Custom pattern #1 reference frequency = _____

Standard pattern shown above uses 16.000 MHz as the input reference frequency.



LEAD COUNT	16L
DIMENSION L	.404

Figure 5: 16-Pin SOIC Package

Ordering Information

ICS1567M-XXX

Example:

ICS XXXX M -XXX

- **Pattern Number (2 or 3 digit number for parts with ROM code patterns)**
- **Package Type**
  - M=SOIC
- **Device Type (consists of 3 or 4 digit numbers)**
- **Prefix**
  - ICS, AV=Standard Device; GSP=Genlock Device