Integrated Circuit Systems, Inc.

Motherboard Clock Generator

Description

The **ICS2694** Motherboard Clock Generator is an integrated circuit using PLL and VCO technology to generate virtually all the clock signals required in a PC. The use of the device can be generalized to satisfy the timing needs of most digital systems by reprogramming the VCO or reconfiguring the counter stages which derive the output frequencies from the VCO's.

The primary VCO is customarily used to generate the CPU clock and is so labeled on the **ICS2694**. Pre-programmed frequency sets are listed on page 6. These choices were made to match the major microprocessor families. CPUSEL (0-3) allow the user to select the appropriate frequency for the application.

Due to the filter in the phase-locked loop, the CPUCLK will move in a linear fashion from one frequency to a newly-selected frequency without glitches. If a fixed CPUCLK value is desired, CPUSEL (0-3) may be hard wired to the desired address with STROBE tied high. (It has a pull-up.) For board test and debug, pulling OUTPUTE to Ground will tristate all the outputs.

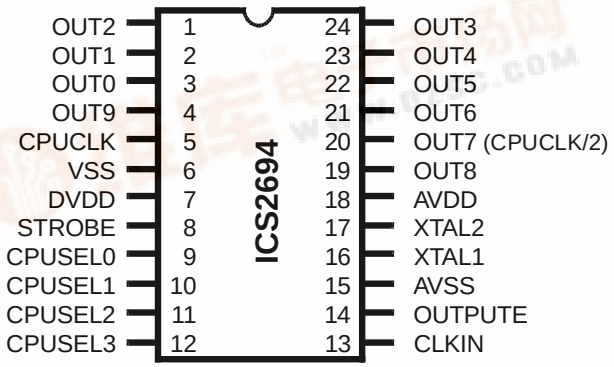
Features

- Low cost - eliminates multiple oscillators and Count Down Logic
- Primary VCO has 16 Mask Programmable frequencies (normally CPU clock)
- Secondary VCO has 1 Mask Programmable frequency (usually 96 MHz)
- Pre-programmed versions for typical PC applications
- 10 Outputs in addition to the primary CPU clock
- Capability to reconfigure counter stages to change the frequencies of the outputs via mask options
- Advanced PLL design
- On-chip PLL filters
- Very Flexible Architecture

Applications

- CPU clock and Co-processor clock
- Hard Disk and Floppy Disk clock
- Keyboard clock
- Serial Port clock
- Bus clock
- System counting or timing functions

Pin Configuration



24-Pin DIP or SOIC

Pin Description

PIN NUMBER	NAME	DESCRIPTION
1	OUT2	4mA Output.
2	OUT1	4mA Output.
3	OUT0	4mA Output
4	OUT9	4mA Output.
5	CPUCLK	4mA Output driven by Voltage Controlled Oscillator 1 (VC01). VC01 is controlled by a 16 word ROM.
6	VSS	Ground for digital portion of chip.
7	DVDD	Plus supply for digital portion of chip.
8	STROBE	Input control for transparent latches associated with CPU (0-3) which select one of 16 values for CPUCLK. Holding STROBE high causes the latches to be transparent.
9	CPUSEL0	LSB CPUCLK address bit.
10	CPUSEL1	CPUCLK address bit.
11	CPUSEL2	CPUCLK address bit.
12	CPUSEL3	MSB CPUCLK address bit.
13	CLKIN	An alternative input for the reference clock. The crystal oscillator output and CLKIN are gated together to generate the reference clock for the VCO's. If CLKIN is used, XTAL1 should be held high and XTAL2 left open. If the internal oscillator is used, hold CLKIN high.
14	OUTPUTE	Pulling this line low tristates all outputs.
15	AVSS	Ground for analog portion of chip.
16	XTAL1	Input of internal crystal oscillator stage.
17	XTAL2	Output of internal crystal oscillator stage. This pin should have nothing connected to it but one of the quartz crystal terminals.
18	AVDD	Positive supply for analog portion of chip.
19	OUT8	4mA Output.
20	OUT7	4mA Output. (Usually assigned as CPUCLK/2 for co-processor use.)
21	OUT6	4mA Output.
22	OUT5	4mA Output.
23	OUT4	4mA Output.
24	OUT3	4mA Output.

Frequency Reference

The internal reference oscillator contains all of the passive components required. An appropriate series-resonant crystal should be connected between XTAL1 (1) and XTAL2 (2). In IBM-compatible applications, this will typically be a 14.31818 MHz crystal, but fundamental mode crystals between 10 MHz and 25 MHz have been tested. Maintain short lead lengths between the crystal and the **ICS2694**. In order to optimize the quality of the quartz crystal oscillator, the input switching threshold of XTAL1 is VDD/2 rather than the conventional 1.4V of TTL. Therefore, XTAL1 may not respond properly to a legal TTL signal since TTL is not required to exceed VDD/2. Therefore, another clock input CLKIN (pin 13) has been added to the chip which is sized to have an input switching point of 1.4V. Inside the chip, these two inputs are ANDED. Therefore, when using the XTAL1 and XTAL2, CLKIN should be held high. (It has a pull-up.) When using CLKIN, XTAL1 should be held high. (It does not have a pull-up because a pull-up would interfere with the oscillator bias.)

It is anticipated that some applications will use both clock inputs, properly gated, for either board test or unique system functions. By generating all the system clocks from one reference input, the phase and delay relationships between the various outputs will remain relatively fixed, thereby eliminating problems arising from totally unsynchronized clocks interacting in a system.

Power Supply Conditioning

The **ICS2694** is a member of the second generation of dot clock products. By incorporating the loop filter on chip and upgrading the VCO, the ease of application has been substantially improved over earlier products. If a stable and noise-free power supply is available, no external components are required. However, in some applications it may be judicious to decouple the power supply as shown in Figures 1 or 2. Figure 1 is the normal configuration for 5 volt only applications. Which of the two provides superior performance depends on the noise content of the power supplies. In general, the configuration of Figure 1 is satisfactory. Figure 2 is the more conventional if a 12 volt analog supply is available, although the improved performance comes at a cost of an extra component; however, the cost of the discretes used in Figure 1's are less than the cost of Figure 1's discrete components.

Since the **ICS2694** outputs a large number of high-frequency clocks, conservative design practices are recommended. Care should be exercised in the board layout of supply and ground traces, and adequate power supply decoupling capacitors consistent with the application should be used.

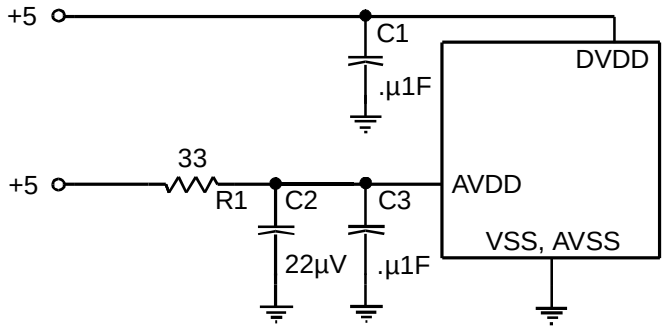


Figure 1

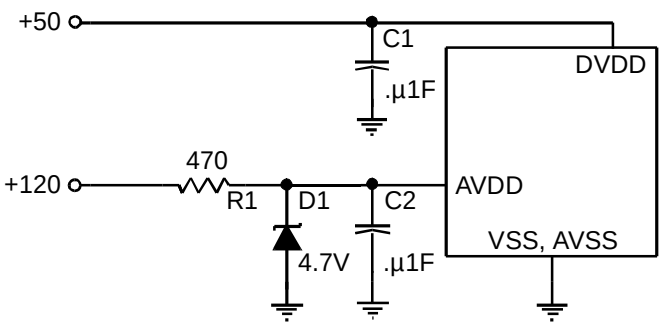


Figure 2

Absolute Maximum Ratings

Supply Voltage . . . . . V_{DD}. . . . . -0.5V to +7V
Input Voltage. . . . . V_{IN} . . . . . -0.5V to VDD +0.5V
Output Voltage . . . . . VOUT. . . . . -0.5V to VDD +0.5V
Clamp Diode Current . . . . . V_{IK} & I_{OK}. . . . . ±30mA
Output Current per Pin . . . . . I_{OUT} . . . . . ±50mA
Operating Temperature . . . . . T_O . . . . . 0°C to + 150°C
Storage Temperature . . . . . T_S . . . . . -85°C to + 150°C
Power Dissipation. . . . . P_D 500mW

Values beyond these ratings may damage the device. This device contains circuitry to protect the inputs and outputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid applications of any voltage higher than the maximum rated voltages. For proper operation, it is recommended that V_{IN} and V_{OUT} be constrained to > = V_{SS} and < = V_{DD}.

DC Characteristics (0°C to 70°C)

PARAMETER	SYMBOL	CONDITIONS	MIN	MAX	UNITS
Operating Voltage Range	V_{DD}		4.0	5.5	V
Input Low Voltage	V_{IL}	V_{DD} = 5V	VSS	0.8	V
Input High Voltage	V_{IH}	V_{DD} = 5V	2.0	V_{DD}	V
Input Leakage Current	I_{IH}	V_{IN} = V_{cc}	-	10	*u*A
Output Low Voltage	V_{OL}	I_{OL} = 4.0 mA	-	0.4	V
Output High Voltage	V_{OH}	I_{OH} = 4.0 mA	2.4	-	V
Supply Current	I_{DD}	V_{DD} = 5V, CPUCLK = 80 MHz	-	55	mA
Internal Pull-up Resistors	R_{UP} *	V_{DD} = 5V, V_{in} = 0V	50	-	k ohm
Input Pin Capacitance	C_{in}	F_c = 1 MHz	-	8	pF
Output Pin Capacitance	C_{out}	F_c = 1 MHz	-	12	pF

* The following inputs have pull-ups: OUTPUTE, STROBE, CPUSEL (0-3), CLKIN.

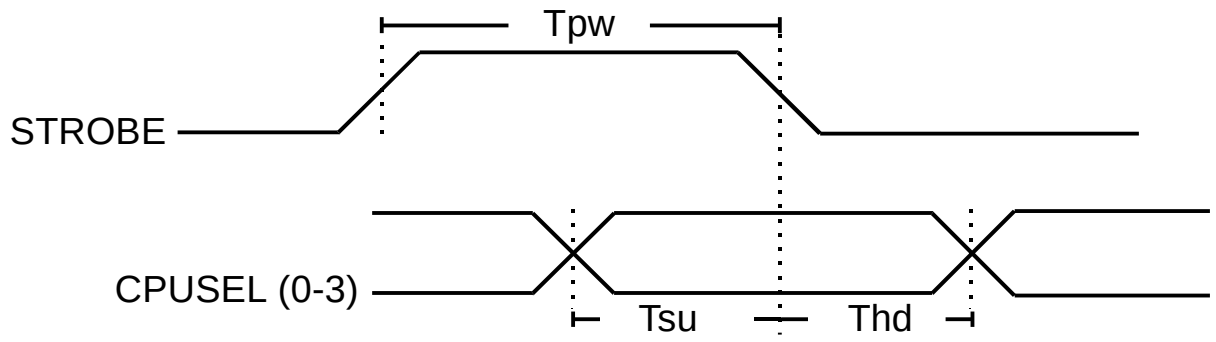
AC Timing Characteristics

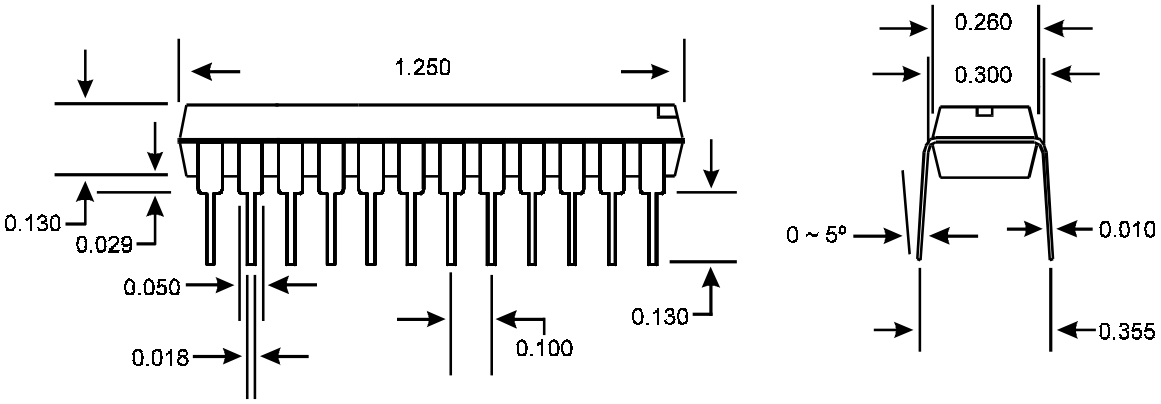
The following notes apply to all parameters presented in this section:

1. Xtal Frequency = 14.31818 MHz
2. All units are in nanoseconds (ns).
3. Rise and fall time is between 0.8 and 2.0 VDC.
4. Output pin loading = 15pF
5. Duty cycle is measured at 1.4V.
6. Supply Voltage Range = 4.5 to 5.5 volts
7. Temperature Range = 0°C to 70°C

SYMBOL	PARAMETER	MIN	MAX	NOTES
	STROBE TIMING			
Tpw	Strobe Pulse Width	20	-	
Tsu	Setup Time Data to Strobe	10	-	
Thd	Hold Time Data to Strobe	10	-	
	FOUT TIMING			
Tr	Rise Time	-	3	Duty Cycle 40% min. to 60% max.
Tf	Fall Time	-	3	at 80 MHz
-	Frequency Error		0.5	%
-	Maximum Frequency		135	MHz

Note:
Pattern -004 has rising edges of CPUCLK and CPUCLK/2 matched to ± 2 ns.





24-Pin DIP Package

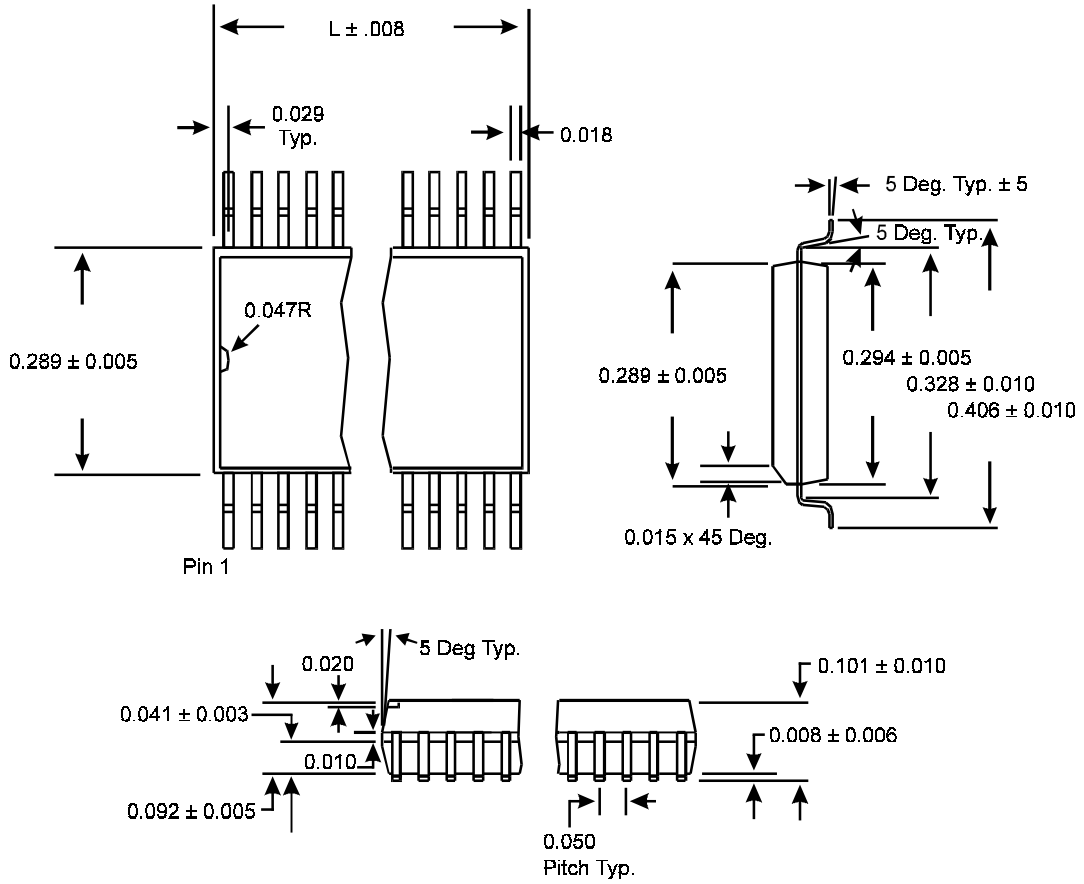
Ordering Information

ICS2694N-XXX

Example:

ICS XXXX M -XXX

- **Pattern Number (2 or 3 digit number for parts with ROM code patterns)**
- **Package Type**
  N=DIP (Plastic)
- **Device Type (consists of 3 or 4 digit numbers)**
- **Prefix**
  ICS, AV=Standard Device; GSP=Genlock Device



LEAD COUNT	14L	16L	18L	20L	24L	28L	32L
DIMENSION L	0.354	0.404	0.454	0.504	0.604	0.704	0.804

SOIC Packages

Ordering Information

ICS2694M-XXX

Example:

ICS XXXX M -XXX

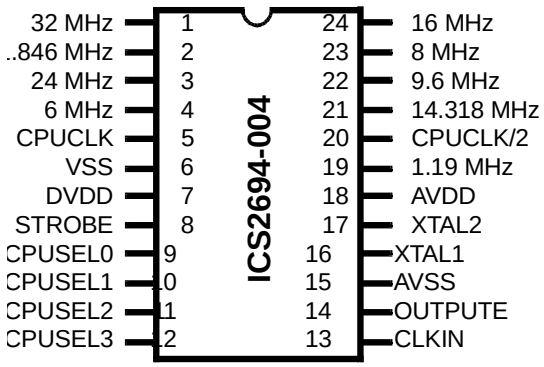
Pattern Number (2 or 3 digit number for parts with ROM code patterns)

Package Type
M=SOIC

Device Type (consists of 3 or 4 digit numbers)

Prefix
ICS, AV=Standard Device; GSP=Genlock Device

ICS2694 Standard Patterns



CPUSEL0-3 (Hex)	CPUCLK OUTPUT (Pin 5) (MHz)
0	2
1	10
2	20
3	24
4	25
5	32
6	33.33
7	40
8	48
9	50
10	54
11	66.67
12	68
13	80
14	100
15	16

Note: Pattern -004 has rising edges of CPUCLK and CPUCLK/2 matched to ± 2 ns.

Another alternative for CPU CLOCK generation is the ICS2494-244 if the additional functions of the **ICS2694** are not needed in the application.

ICS Part Number	ICS2494-244
Address FS3-0 (Hex)	Frequency (MHz)
0	20
1	24
2	32
3	40
4	50
5	66.6
6	80
7	100
8	54
9	70
0	90
B	110
C	25
D	33.3
E	40
F	50
Address MS1-0 (Hex)	Frequency (MHz)
0	16
1	24
2	50
3	66.6