SONY®

ICX027CKA

1/2 inch CCD Image Sensor for PAL Color Camera

Description

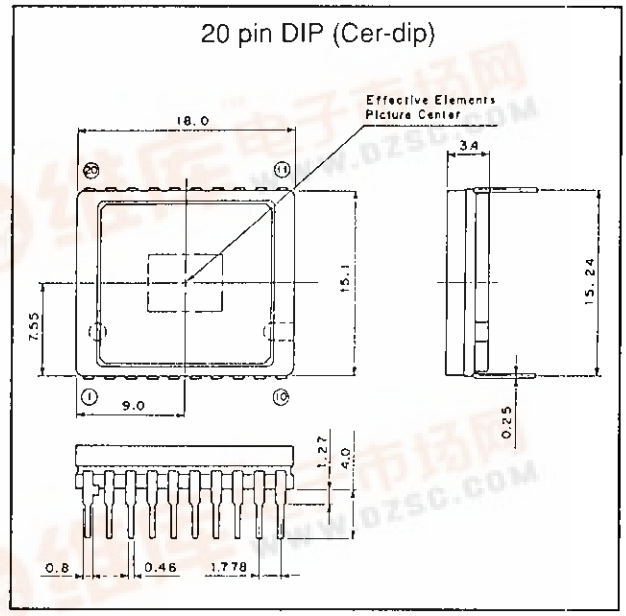
ICX027CKA is an interline transfer CCD solid-state image sensor suitable for PAL1/2 inch color video cameras. High sensitivity is achieved through the adoption of Ye, Cy, Mg and G complementary color mosaic filters and HAD (Hole-Accumulation Diode) sensors.

Beside correspondence with timing generator CXD1253, 5V drive of the reset gate is also possible.

This chip features a field integration read out system, an electronic shutter with variable charge-storage time and 20pin Cer-DIP package.

Package Outline

Unit: mm

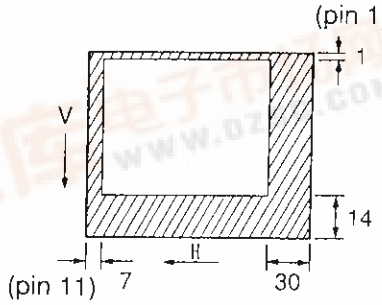


Features

- High sensitivity (+6 dB compare with ICX027AK)
- Optical size 1/2 inch format
- Field integration read out system
- Low dark current. High sensitivity HAD sensor
- Ye, Cy, Mg, G on chip type complementary color mosaic filter.
- Horizontal register 5V drive
- Reset gate 5V drive
- High antiblooming
- Low smear
- Variable speed electronic shutter

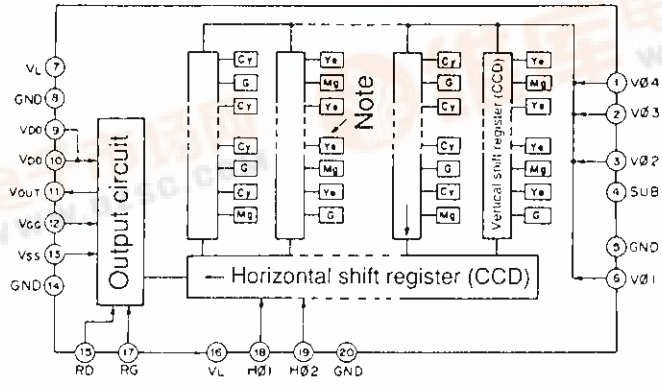
Device Structure

- Number of effective pixels 500 (H) × 582 (V)
- Number of total pixels 537 (H) × 597 (V)
- Interline transfer CCD image sensor
- Chip size 7.84 mm (H) × 6.40 mm (V)
- Unit cell size 12.7 µm (H) × 8.3 um (V)
- Optical black
  - Horizontal (H) direction Front 7 pixels Rear 30 pixels
  - Vertical (V) direction Front 14 pixels Rear 1 pixel
- Number of dummy bits
  - Horizontal 16
  - Vertical 1 (even field only)
- Substrate material silicon



Optical black position (Top View)

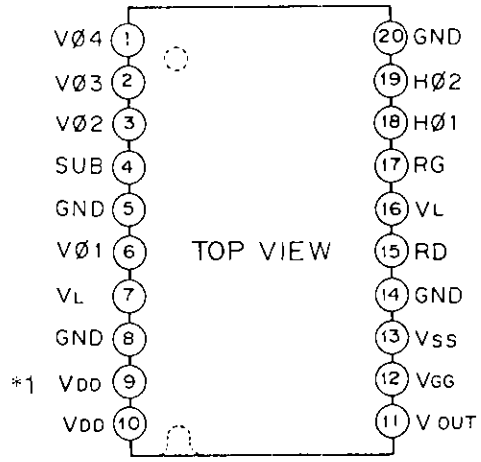
Block Diagram



Note) —□ : Photo sensor

E91646-YA

Pin Configuration (Top View)



*1 As Pins 9 and 10 are internally shorted, if either one is connected to the power supply while the other may be kept open. Should both be connected to the power supply, make sure the same voltage is applied.

Pin Description

No.	Symbol	Description	No.	Symbol	Description
1	Vφ4	Vertical register transfer clock	11	VOUT	Signal output
2	Vφ3	Vertical register transfer clock	12	VGG	Output amplifier gate bias
3	Vφ2	Vertical register transfer clock	13	VSS	Output amplifier source
4	SUB	Substrate (Overflow drain)	14	GND	GND
5	GND	GND	15	RD	Reset drain bias
6	Vφ1	Vertical register transfer clock	16	VL	Protective transistor bias
7	VL	Protective transistor bias	17	RG	Reset gate clock
8	GND	GND	18	Hφ1	Horizontal register transfer clock
9	VDD	Output amplifier drain supply	19	Hφ2	Horizontal register transfer clock
10	VDD	Output amplifier drain supply	20	GND	GND

Absolute Maximum Ratings

• Substrate voltage	SUB – GND	−0.3 to +55	V
• Supply voltage	VDD, RD, VOUT, VSS, – GND	−0.3 to +18	V
	VDD, RD, VOUT, VSS, – SUB	−55 to +10	V
• Clock input voltage	Vφ1, Vφ2, Vφ3, Vφ4, Hφ1, Hφ2 – GND	−15 to +20	V
	Vφ1, Vφ2, Vφ3, Vφ4, Hφ1, Hφ2 – SUB	−65 to +10	V
• Voltage difference between vertical clock input pins		+15	V *2
• Voltage difference between horizontal clock input pins		+17	V
• Hφ1, Hφ2, – Vφ4		−17 to +17	V
• RG, VGG – GND		−10 to +15	V
• RG, VGG – SUB		−55 to +10	V
• VL – SUB		−65 to +0.3	V
• Beside GND, SUB, VL – VL		−0.3 to +30	V
• Storage temperature		−30 to +80	°C
• Operating temperature		−10 to +60	°C

*2 +27 V (Max.) when clock width < 10 µs, duty factor < 0.1%.

Bias Conditions

Item	Symbol	Min.	Typ.	Max.	Unit	Remarks
Output amplifier drain voltage	V_{DD}	14.55	15.0	15.45	V	
Reset drain voltage	V_{RD}	14.55	15.0	15.45	V	$V_{RD} = V_{DD}$
Output amplifier gate voltage	V_{GG}	1.75	2.0	2.25	V	
Output amplifier source	Vss	Ground through 680 Ω resistor				±5%
Substrate voltage adjustment range	V_{SUB}	7.0		18.5	V	*1
Fluctuation range after substrate voltage adjustment	ΔV_{SUB}	−3		+3	%	
Reset gate clock voltage adjustment range	V_{RGL}	0.5		3.5	V	*1
Fluctuation range after reset gate clock voltage adjustment	ΔV_{RGL}	−3		+3	%	
Protective transistor bias	V_L	*2				

DC characteristics

Item	Symbol	Min.	Typ.	Max.	Unit	Remarks
Output amplifier drain current	I_{DD}		2.5		mA	
Input current	I_{IN1}			1	μA	*3
Input current	I_{IN2}			10	μA	*4

Note) *1. Substrate voltage (V_{SUB}) and reset gate clock voltage (V_{RGL}) setting values are displayed at the back of the device through a code address. Adjust so as to obtain the displayed voltages at SUB and RG pins respectively.

V_{SUB} code address - 1 digit display
V_{RGL} code address - 1 digit display

□ ↑ V_{RGL} code address

□ ↑ V_{SUB} code address

The relation between code address and actual numerical values.

V_{RGL} code address	0	1	2	3	4	5	6
Numerical value	0.5	1.0	1.5	2.0	2.5	3.0	3.5

V_{SUB} code address	A	b	C	D	E	f	G	h	J	K	L	m
Numerical value	7.0	7.5	8.0	8.5	9.0	9.5	10.0	10.5	11.0	11.5	12.0	12.5
V_{SUB} code address	N	P	Q	R	S	T	U	V	W	X	Y	Z
Numerical value	13.0	13.5	14.0	14.5	15.0	15.5	16.0	16.5	17.0	17.5	18.0	18.5

<Example> "5L" → V_{RGL} = 3.0 V, V_{SUB} = 12.0 V

*2. V_L setting is V_{VL} of the vertical transfer clock waveform.

*3. 1) Current to earth when 18V is applied to pins V_{DD}, V_{OUT}, Vss and SUB pin. However, pins that are not tested are grounded.
2) Current to earth when 20V is sequentially applied to pins Vφ1, Vφ2, Vφ3, Vφ4, Hφ1, and Hφ2. However, 20V is applied to SUB while pins that are not tested are grounded.
3) Current to earth when 15V is sequentially applied to pins RG and V_{GG}. However, 15V is applied to SUB while pins that are not tested are grounded.

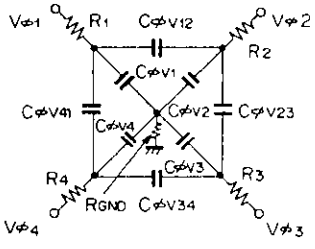
*4. 1) Current to earth when 55V is applied to SUB pin. Pins that are not tested are grounded.
2) Current to earth when V_L is grounded, GND and SUB are open and 30V is applied to other pins.

Clock Voltage Conditions

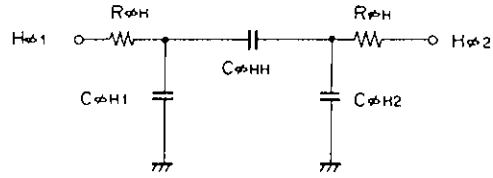
Item	Symbol	Min.	Typ.	Max.	Unit	Waveform	Remarks
Read out clock voltage	V_{VT}	14.3	15.0	15.7	V	1	
Vertical transfer clock voltage	$V_{VH1}, V_{VH2}, V_{VH3}, V_{VH4}$	−0.2	0	0.2	V	2	$V_{VH}=(V_{VH1}+V_{VH2})/2$
	$V_{VL1}, V_{VL2}, V_{VL3}, V_{VL4}$	−9.6	−9.0	−8.3	V	2	$V_{VL}=(V_{VL3}+V_{VL4})/2$
	$V_{\phi V}$	8.1	9.0	9.8	V	2	$V_{\phi V}=V_{VHn}-V_{VLn}$ (n=1 to 4)
	$\lvert V_{VH1} - V_{VH2} \rvert$			0.2	V	2	
	$V_{VH3} - V_{VH}$	−0.4		0.1	V	2	
	$V_{VH4} - V_{VH}$	−0.4		0.1	V	2	
	V_{VHH}			0.8	V	2	High level coupling
	V_{VHL}			1.0	V	2	High level coupling
	V_{VLH}			0.8	V	2	Low level coupling
	V_{VLL}			0.8	V	2	Low level coupling
Horizontal transfer clock voltage	$V_{\phi H}$	4.7	5.0	5.3	V	3	
	V_{HL}	−0.05	0	0.05	V	3	
Reset gate clock voltage	$V_{\phi RG}$	4.5	5.0	5.5	V	4	When V_{RGL} is adjusted to the displayed value
	$V_{RGLH} - V_{RGLL}$			0.8	V	4	
	$V_{\phi RG}$	8.0		11.5	V	4	When V_{RGL} is fixed
	V_{RGL}	−0.1	0	0.1	V	4	
	$V_{RGLH} - V_{RGLL}$			0.8	V	4	
Substrate clock voltage	$V_{\phi SUB}$	23.0		34.0	V	5	

Clock Equivalent Circuit Constant

Item	Symbol	Min.	Typ.	Max.	Unit	Remarks
Capacitance between vertical transfer clock and GND	$C_{\phi V1}$, $C_{\phi V3}$		1000		pF	
Capacitance between vertical transfer clock and GND	$C_{\phi V2}$, $C_{\phi V4}$		1200		pF	
Capacitance between vertical transfer clocks	$C_{\phi V12}$, $C_{\phi V34}$		1400		pF	
Capacitance between vertical transfer clocks	$C_{\phi V23}$, $C_{\phi V41}$		900		pF	
Capacitance between horizontal transfer clock and GND	$C_{\phi H1}$, C		70		pF	
Capacitance between horizontal transfer clocks	$C_{\phi HH}$		50		pF	
Capacitance between reset gate clock and GND	$C_{\phi RG}$		8		pF	
Capacitance between substrate clock and GND	$C_{\phi SUB}$		400		pF	
Vertical transfer clock serial resistor	R_1, R_2, R_3, R_4		33		Ω	
Vertical transfer clock ground resistor	R_{GND}		15		Ω	
Horizontal transfer clock serial resistor	$R_{\phi H}$		10			



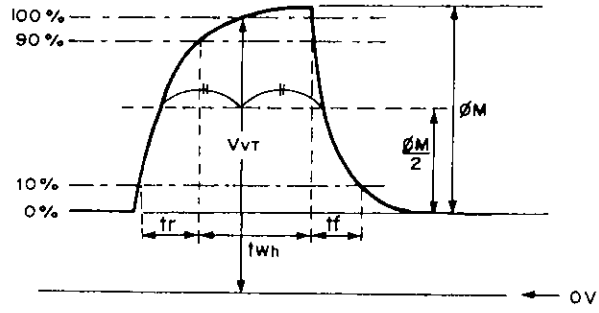
Vertical transfer clock equivalent circuit



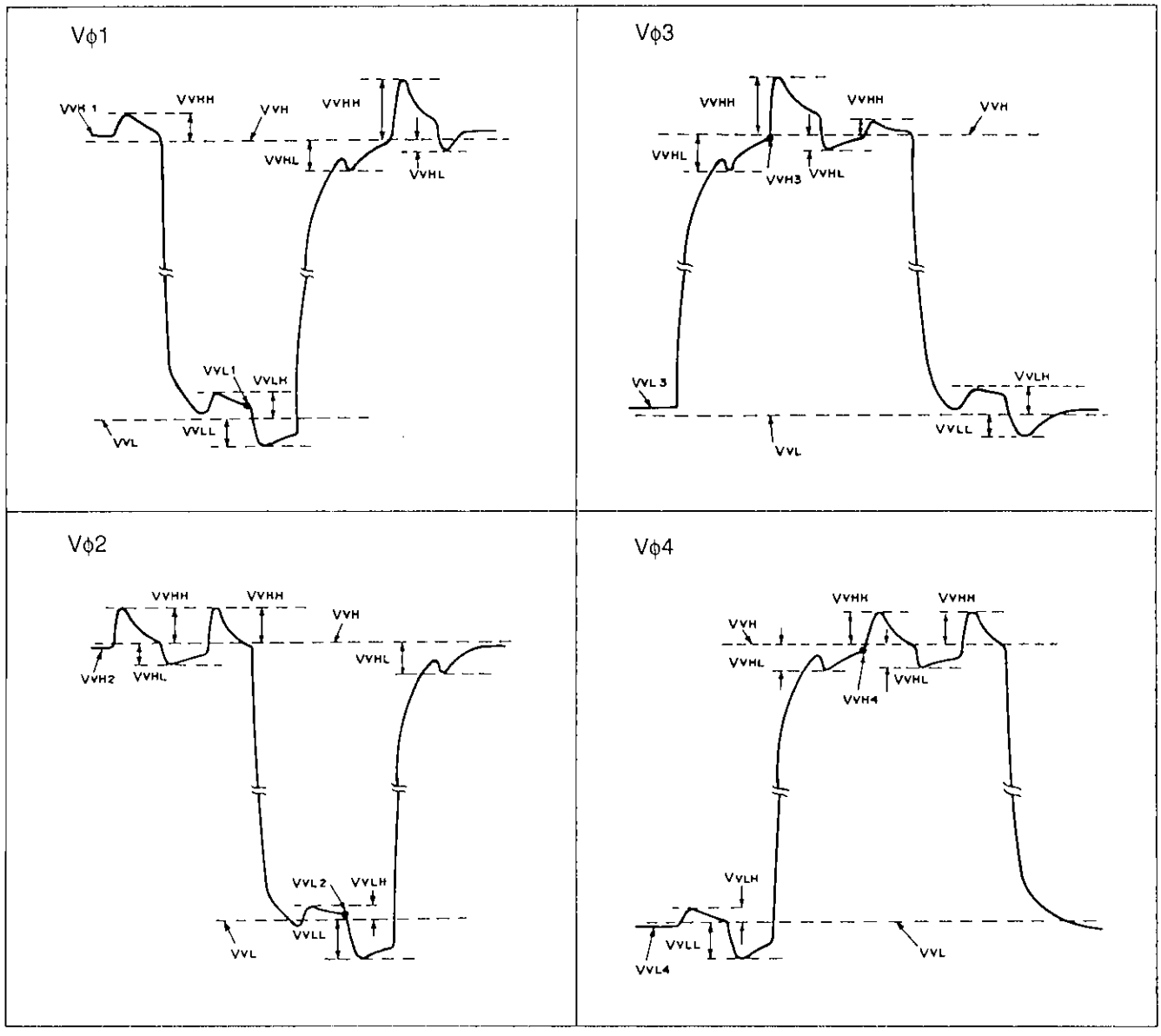
Horizontal trasfer clock equivalent circuit

Drive Clock Waveform Conditions

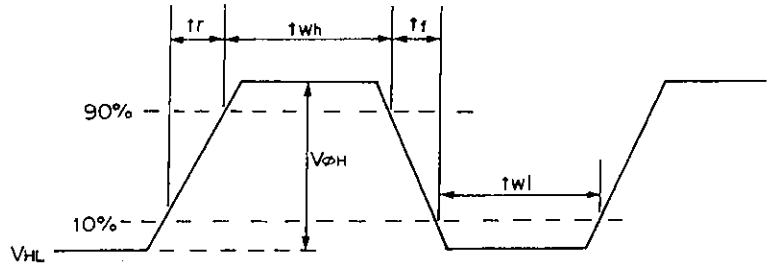
1. Read out clock waveform



2. Vertical transfer clock waveform



3. Horizontal transfer clock waveform



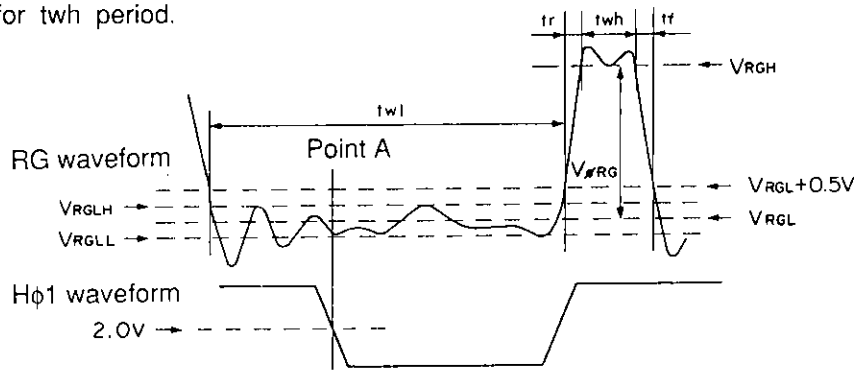
4. Reset gate clock waveform

VRGLH is the maximum value and VRGLL the minimum value of the coupling waveform of the period from Point A, in the diagram above, up to RG rise. VRGL is the mean value for VRGLH and VRGLL.

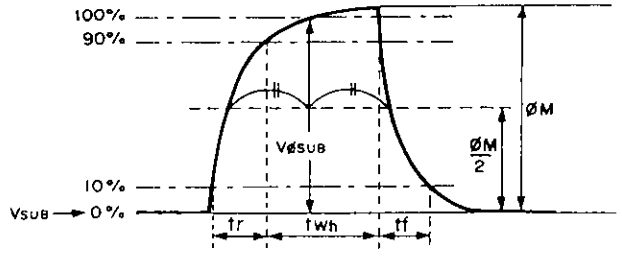
VRGL = (VRGLH + VRGLL)/2

VRGH is the minimum value for twh period.

VφRG = VRGH − VRGL



5. Substrate clock waveform



Item	Symbol	twh			twl			tr			tf			Unit	Remarks
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.		
Read out clock	VT	1.5	1.85							0.5			0.5	μs	During read out
Vertical transfer clock	Vφ1,Vφ2,Vφ3,Vφ4									0.45	0.015		0.25	μs	*1
Horizontal transfer clock	Hφ	35	40		38	40			14	17	8	12	15	ns	During imaging *2
Horizontal transfer clock	Hφ1		5.6						0.014			0.012		μs	During parallel serial conversion.
Horizontal transfer clock	Hφ2					5.6			0.014			0.012		μs	During parallel serial conversion.
Reset gate clock	φRG	14	15		76	80			6.5			4.5		ns	
Substrate clock	φSUB	1.5	2.1							0.5			0.5	μs	During charge drain.

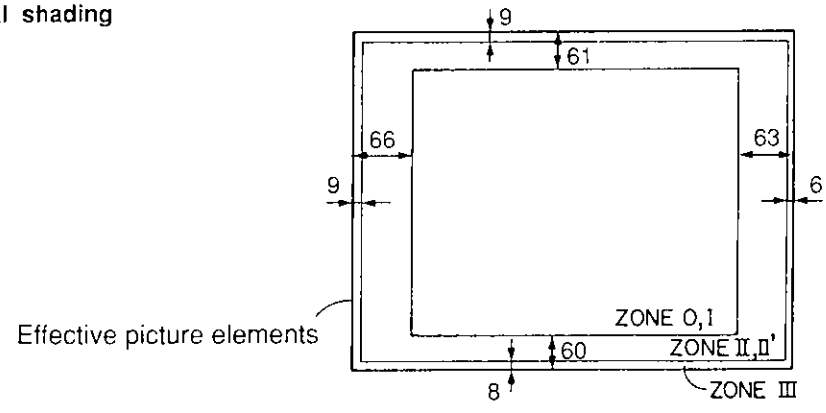
*1) When vertical transfer clock driver CXD1250 is in use. tr and tf are defined as the rising and falling time of 10% to 90% the period between VVL and VVH.

*2) Where, tr-tf is < 4ns, the waveform crosspoint voltage (Vcr) of Hφ1 and Hφ2, is taken as 2.3V<Vcr<2.7V.

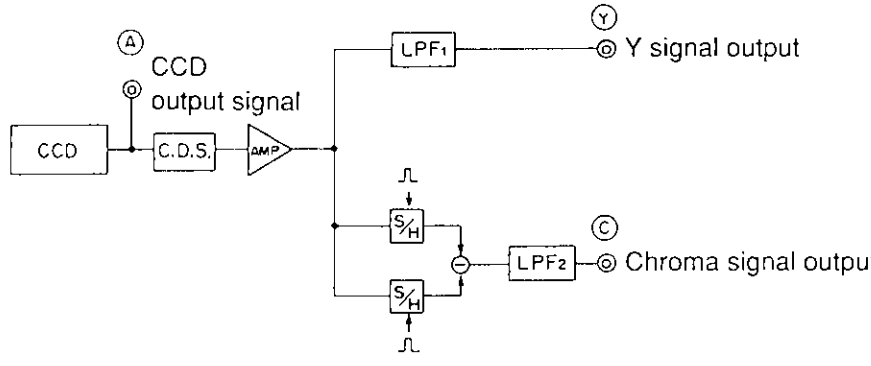
Operating Characteristics Ta = 25°C

Item	Symbol	Min.	Typ.	Max.	Unit	Test method	Remarks
Sensitivity	S	240	320		mV	1	
Saturation signal	Ysat	450			mV	2	Ta=60°C
Smear	SM		0.005	0.015	%	3	
Blooming margin		1000			times	4	
Video signal shading	SHy			20	%	5	Zone0, I
				25	%	5	Zone0, I to II, II'
Uniformity between signal channels	ΔSr			10	%	6	
	ΔSb			10	%	6	
Dark signal	Ydt			2	mV	7	Ta=60°C
Dark signal shading	ΔYdt			1	mV	8	Ta=60°C
Flicker Y	Fy			2	%	9	
Flicker R-Y	Fcr			5	%	9	
Flicker B-Y	Fcb			5	%	9	
Horizontal stripes R	Lcr			4	%	10	
Horizontal stripes G	Lcg			4	%	10	
Horizontal stripes B	Lcb			4	%	10	
Horizontal stripes W	Lcw			4	%	10	
Lag	ΔYlag			0.5	%	11	

Zone chart of Video signal shading



Testing System



Note) Adjust AMP amplifier so that total gains between A and Y and between A and C equal 1.

Test Method

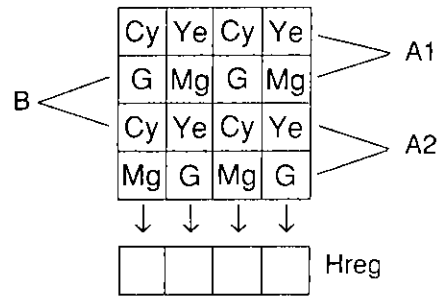
Test conditions

1) Through the following tests the substrate voltage should set to the value displayed on the device, while the device drive conditions should be kept within the range of the bias and clock voltage conditions.

2) Through the following tests defects are excluded, and unless otherwise specified the optical black level (Hence forth referred to as OPB) is set as the reference for the signal output which is taken as the Y signal output or the Chroma signal output of the testing system.

Color coding of CFA (Color Filter Array) & Composition of luminance (Y) and chrominance (C) signals.

CFA of this image sensor is shown in the Figure. This complementary CFA is used with a "field integration mode", where all of the photosites are read out during each video field. Signals from two vertically adjacent photosites, such as line A1 or A2 for field A, are summed when the image charge is transferred into the vertical storage columns. The readout line pairing is shifted down one line for field B. The sensor output signals through the horizontal shift register (H reg.) at line A1 are



Color Coding Diagram

[G+Cy], [Mg+Ye], [G+Cy], [Mg+Ye].

These signals are processed in order to compose Y and C signals. By adding the two adjacent signals at line A1, Y signal is formed as follows:

$$Y = \{(G+Cy) + (Mg+Ye)\} \times 1/2$$
$$= 1/2\ \{2B+3G+2R\}$$

C signal is composed by subtracting the two adjacent signals at line A1.

$$R - Y = \{(Mg+Ye) - (G+Cy)\}$$
$$= \{2R-G\}$$

Next, the signals through H reg. at line A2 are

[Mg+Cy], [G+Ye], [Mg+Cy], [G+Ye]

Similarly, Y and C signals are composed at line A2.

$$Y = \{(G+Ye) + (Mg+Cy)\} \times 1/2$$
$$= 1/2\ \{2B+3G+2R\}$$

$$-(B-Y) = \{(G+Ye) - (Mg+Cy)\}$$
$$= -\{2B-G\}$$

Accordingly, Y signal is balanced in relation to the scanning lines, and C signal takes the form of R–Y and –(B–Y) on alternate lines.
It is the same for B field.

Definition of standard imaging conditions

①Standard imaging condition I: (As imaging device) Use a pattern box (luminance 706 cd/m^2 3200K Halogen source), at F5.6 with a typical test lens, and CM-500S (t=1.0 mm) for IR cut filter.

②Standard imaging condition II: Use a light source with uniformity within 2%, color temperature of 3200K and CM-500S (t=1.0 mm) as IR cut filter. The light intensity is adjusted in accordance with the average value of Y signals (Y_A) indicated in each item.

1) Set to standard imaging condition I and measure Y signal (S) at the center of the screen.

2) Set to imaging condition II. Adjust light intensity to 10 times when Y signal output average value Y_A=150mV. Then test Y signal Min. value.

3) Set to imaging condition II. Adjust light intensity to 500 times when Y signal output average value Y_A=150mV. Stop Read out clock. When the charge drain executed by the electronic shutter at the respective H blankings takes place, test the Max. value Y_{SM} of Y signal output.

$$SM = (Y_{SM}/Y_A) \times 1/500 \times 1/10 \times 100\ (\%) \quad (1/10V)$$

4) Set to imaging condition II. Adjust light intensity to 1000 times when Y signal output average value Y_A=150mV. Then check that there is no blooming.

5) Video signal shading SHy
Set to standard imaging condition II. Test Y signal Max. (Y max.) and Min. (Y min.) values. Adjust light intensity to obtain a Y signal output average value (Y_A) of about 150mV.

$$SHy = (Ymax - Ymin)/Y_A \times 100\ (\%)$$

6) Set to standard imaging condition II. Adjust light intensity to obtain a Y signal output average value (Y_A) of 150mV. Test the Max. (Cr max. and Cb max.) and Min. (Cr min. and Cb min.) values of C signals from R-Y and B-Y channels.

$$\Delta Sr = |\ (Cr\ max. - Cr\ min.)/Y_A\ | \times 100\ (\%)$$
$$\Delta Sb = |\ (Cb\ max. - Cb\ min.)/Y_A\ | \times 100\ (\%)$$

7) Test the average Y signal voltage when the device ambient temperature is at 60°C and light is obstructed with horizontal idle transfer level as reference.

8) Following 7, test Max. (Yd max.) and Min. (Yd min.) values of Y signal output. Only keep spot defects out of this range.

$$\Delta Ydt = Yd\ max - Yd\ min$$

9) ① Fy
Set to standard imaging condition II. Adjust light intensity to obtain a Y signal output average value (Y_A) of 150 mV. Test the Y signal difference (ΔYf) between even field and odd field.

$Fy = (\Delta Yf/Y_A) \times 100$ (%)

② Fcr, Fcb
Set to standard imaging condition II. Insert R and B filter respectively, and test the C signal difference (ΔCr, ΔCb) between even field and odd field and the C signal output average value (C_{Ar}, C_{Ab}). At that time, adjust light intensity to obtain a Y signal output average value (Y_A) of 100 mV.

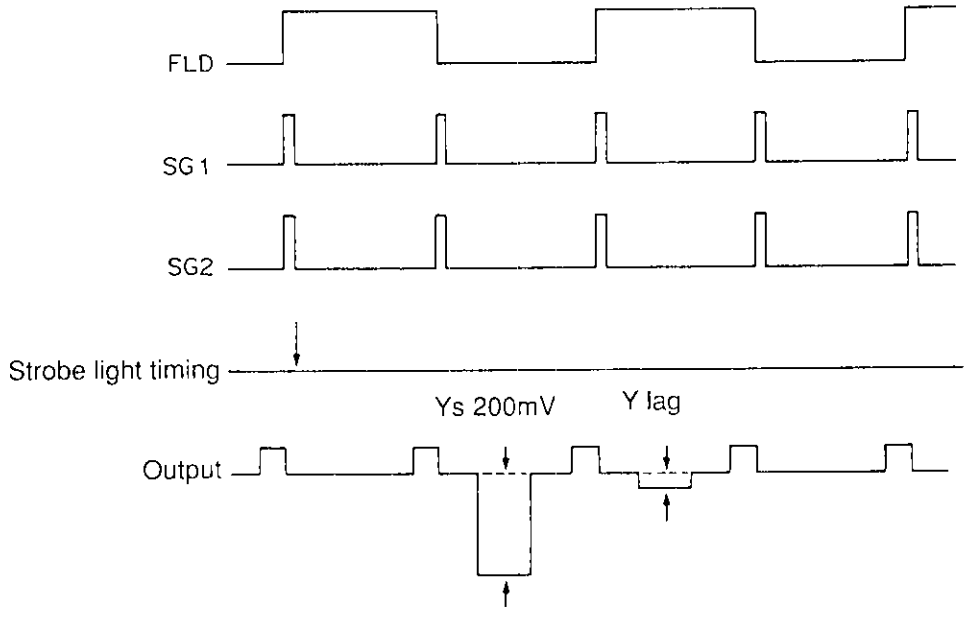
$Fci = (\Delta Ci/C_{Ai}) \times 100$ (%) (i = r, b)

10) Set to standard imaging condition II. Insert W, R, G and B filters respectively, and test the signal difference (ΔYlw, ΔYlr, ΔYlg, ΔYlb) between Y signal lines of the same field. At that time, adjust light intensity to obtain a Y signal output average value (Y_A) of 100 mV.

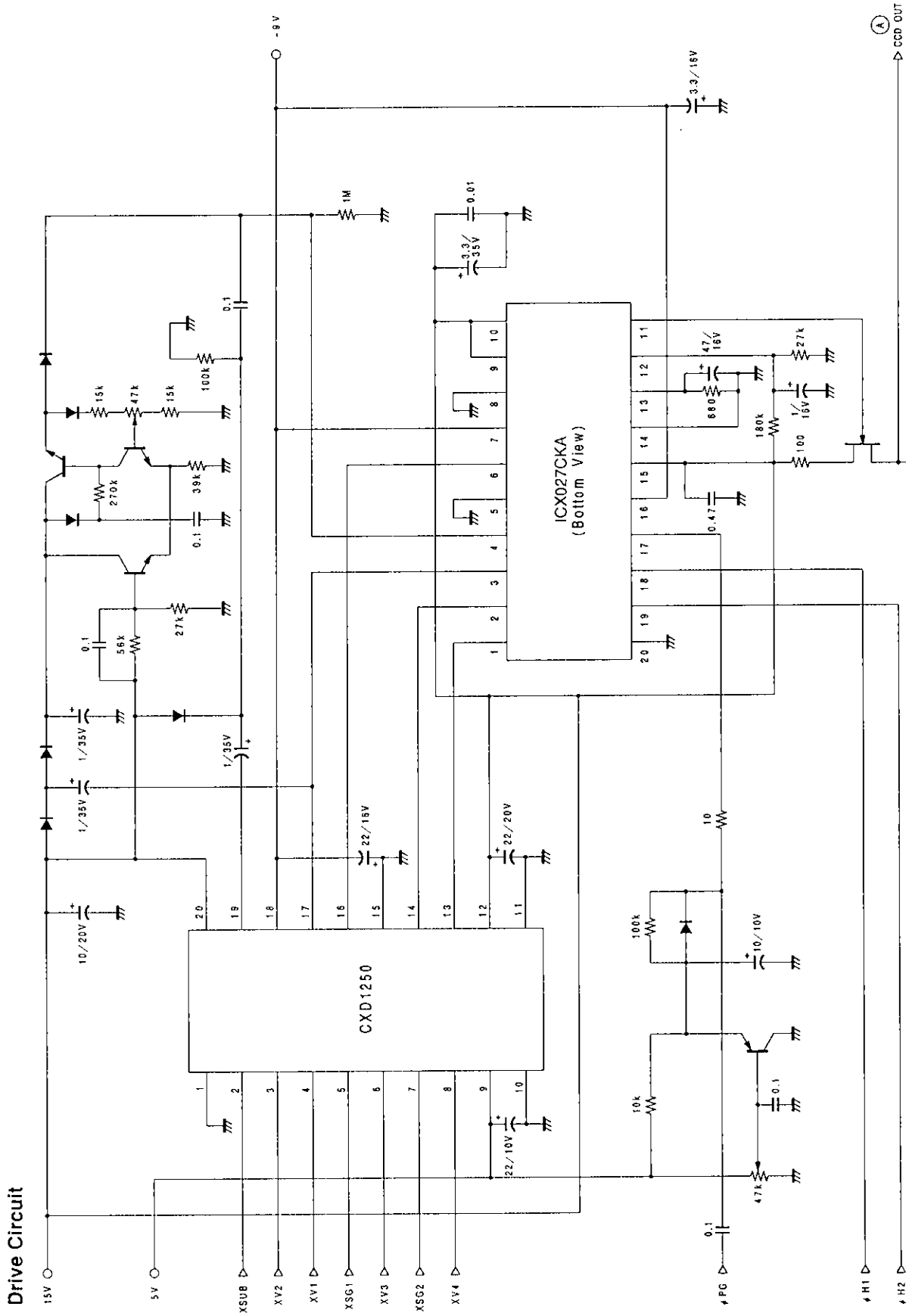
$Lci = (\Delta Yli/Y_A) \times 100$ (%) (i = w, r, g, b)

11) Light a stroboscopic tube with the following timing and test the lag.

$\Delta Ylag = (Ylag/Ys) \times 100$ (%)



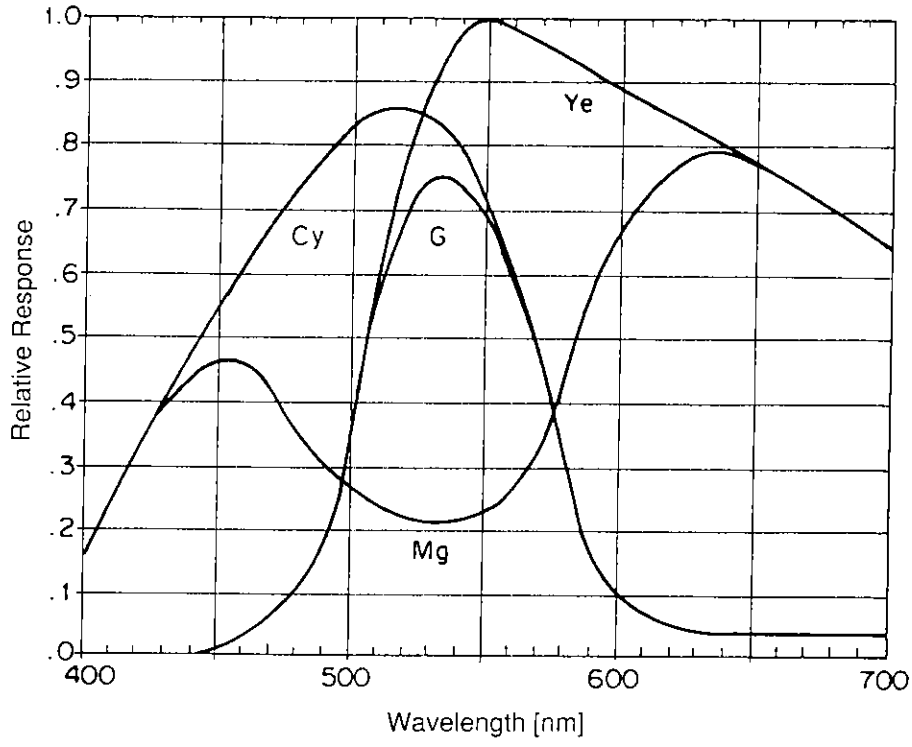
Drive Circuit



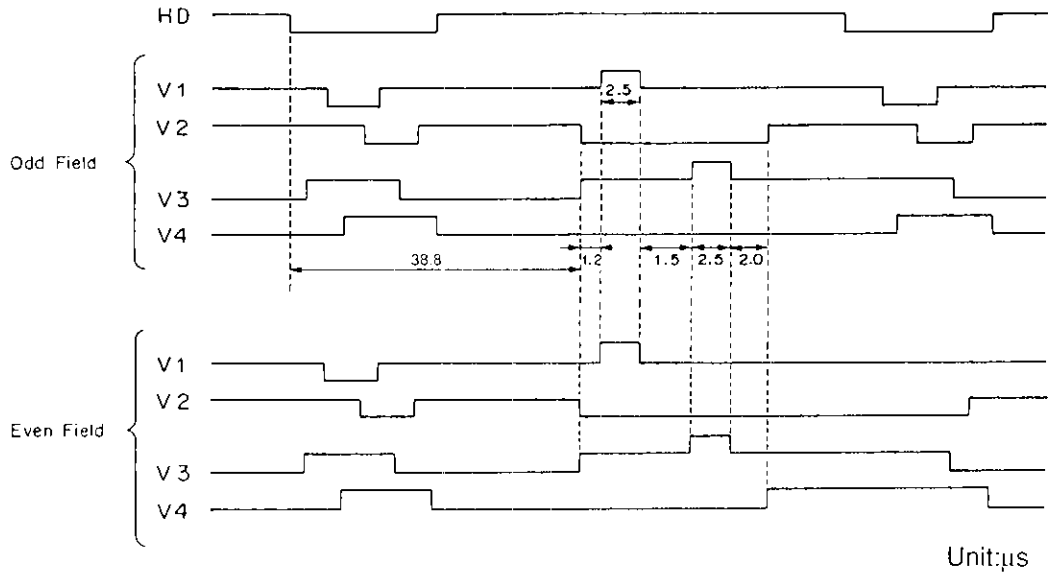
Application circuits shown are typical examples illustrating the operation of the devices. Sony cannot assume responsibility for any problems arising out of the use of these circuits or for any infringement of third party patent and other right due to same.

Spectral Sensitivity Characteristics

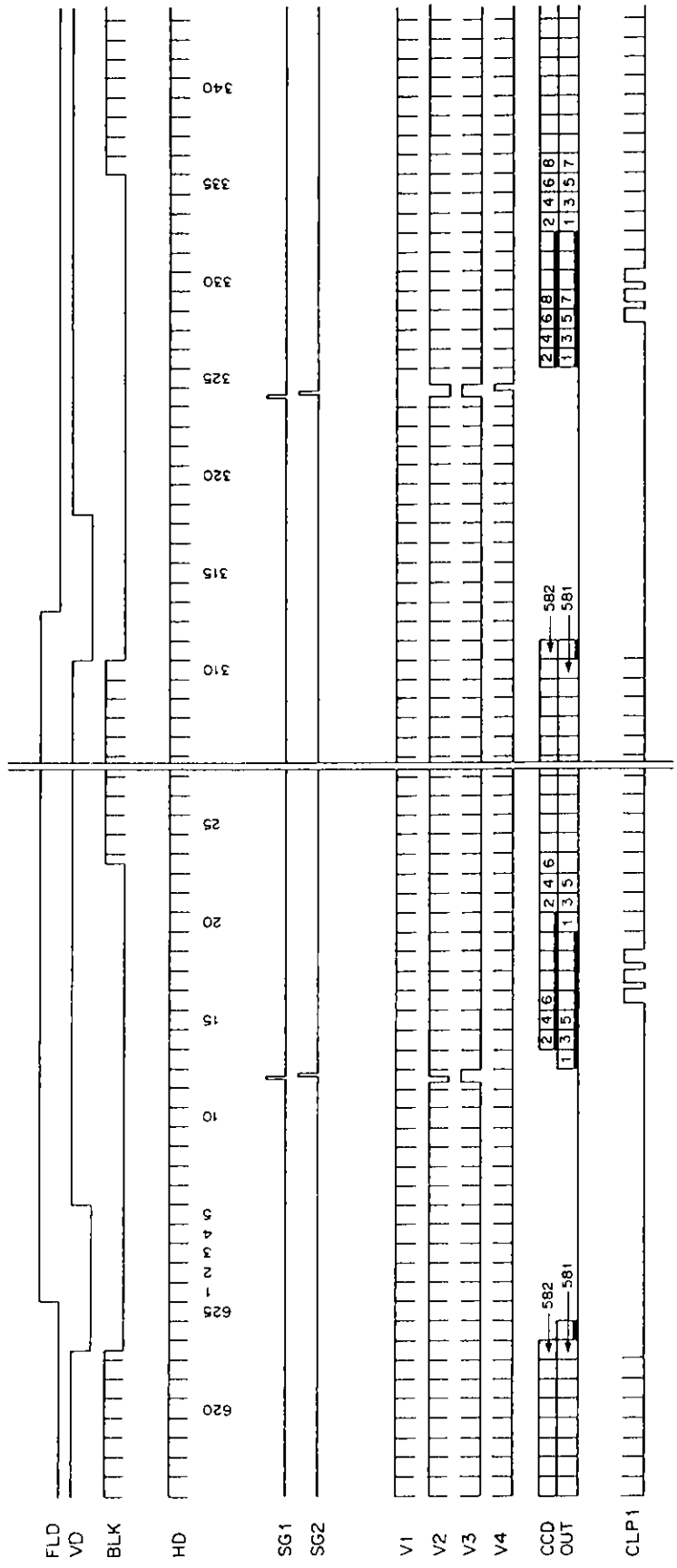
(Excluding light source characteristics, including lens characteristics)



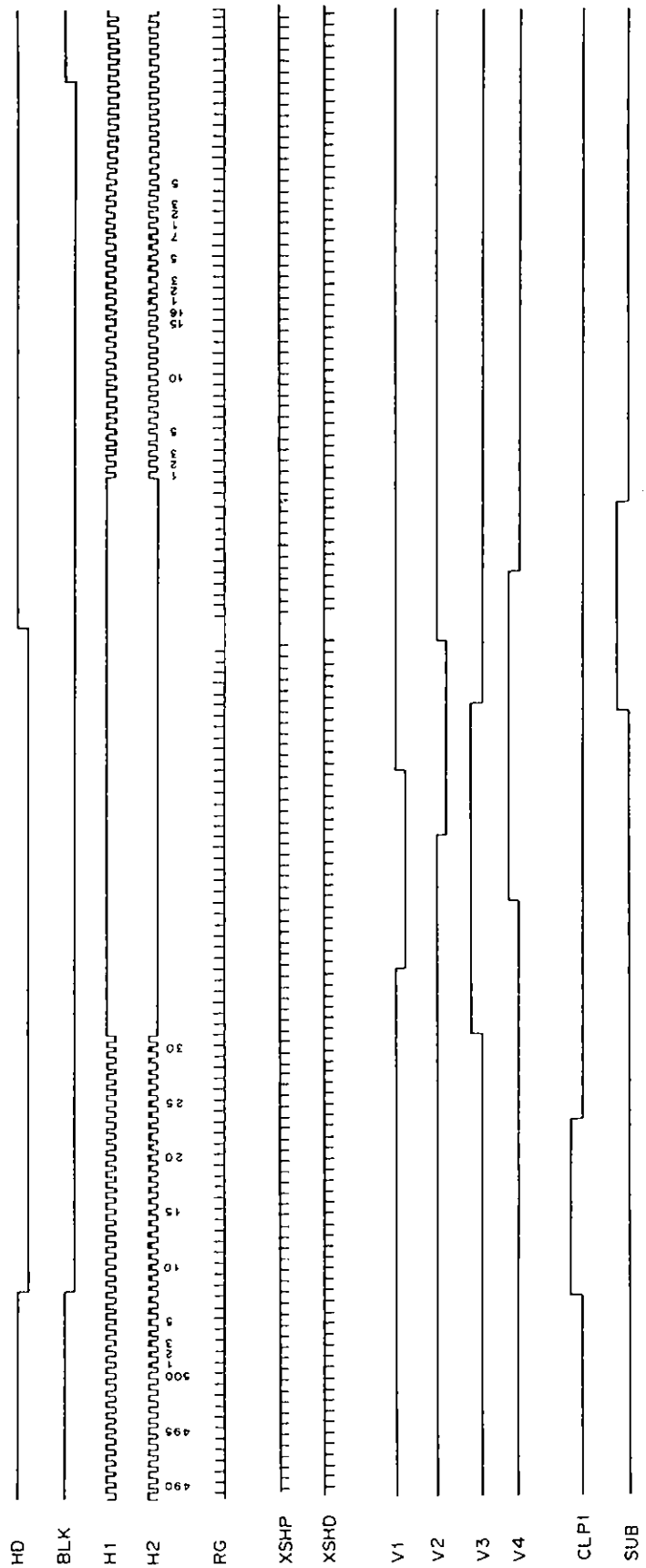
Using read out clock timing chart



Drive Timing Chart (Vertical sync)



Drive Timing Chart (Horizontal sync)



(During electronic shutter operation)

Handling Instructions

1) Static charge prevention
CCD image sensor are easily damaged by static discharge. Before handling be sure to take the following protective measures.
a) Either handle bare handed or use non chargeable gloves, clothes or material. Also use conductive shoes.
b) When handling directly use an earth band.
c) Install a conductive mat on the floor or working table to prevent the generation of static electricity.
d) Ionized air is recommended for discharge when handling CCD image sensor.
e) For the shipment of mounted substrates use boxes treated for the prevention of static charges.

2) Soldering
a) Make sure the package temperature does not exceed 80°C.
b) Solder dipping in a mounting furnace causes damage to the glass and other defects. Use a grounded 30W soldering iron and solder each pin in less than 2 seconds. For repairs and remount cool sufficiently.
c) To dismount an imaging device do not use a solder pult. When using an electric desoldering tool use a thermal controller of the zero cross On/Off type and connect to ground.

3) Dust and dirt protection
a) Operate in clean environments (around class 1000 will be appropriate).
b) Do not either touch glass plates by hand or have any object come in contact with glass surfaces. Should dirt stick to a glass surface blow it off with an air blow. (For dirt stuck through static electricity ionized air is recommended)
c) Clean with a cotton bud and ethyl alcohol if the glass surface is grease stained. Be careful not to scratch the glass.
d) Keep in case to protect from dust and dirt. To prevent dew condensation, preheat or precool when moving to a room with great temperature differences.
e) When a protective tape is applied before shipping, just before use remove the tape applied for electrostatic protection. Do not reuse the tape.

4) Do not expose to strong light (sun rays) for long periods, color filters are discolored.

5) Exposure to high temperatures or humidity will affect the characteristics. Accordingly avoid storage or usage in such conditions.

6) CCD image sensor are precise optical equipment that should not be subject to mechanical shocks.