HARRIS Semiconductor

IH6201

April 1999

Dual CMOS Driver/Voltage Translator

Features

- Driven Direct from TTL or CMOS Logic
- Translates Logic Levels Up to 30V Levels
- Switches $20V_{ACPP}$ Signals When Used in Conjunction with the IH401A Varafet (As An Analog Gate)
- $t_{ON} \leq 300ns$ & $t_{OFF} \leq 200ns$ for 30V Level Shifts
- Quiescent Supply Current $\leq 100\mu A$ for Any State (DC)
- Provides Both Normal & Inverted Outputs

Part Number Information

PART NUMBER	TEMP. RANGE (^oC)	PACKAGE
IH6201CJE	0 to 70	16 Ld CerDIP
IH6201MJE	-55 to 125	16 Ld CerDIP
IH6201CPE	0 to 70	16 Ld PDIP

Description

The IH6201 is a CMOS, Monolithic, Dual Voltage Translator; it takes low level TTL or CMOS logic signals and converts them to higher levels (i.e. to ±15V swings). This translator is typically used in making solid state switches, or analog gates.

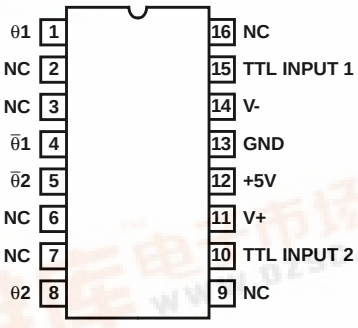
When used in conjunction with the IH401A Varafets, the combination makes a complete solid state switch capable of switching signals up to $22V_{P-P}$ and up to 20MHz in frequency. This switch is a "break-before-make" type (i.e. t_{OFF} time < t_{ON} time). The combination has typical $t_{OFF} \approx$ 80ns and typical $t_{ON} \approx$ 200ns for signals up to $20V_{P-P}$ in amplitude.

A TTL "1" input strobe will force the θ driver output up to V+ level; the $\overline{\theta}$ output will be driven down to the V- level. When the TTL input goes to "0", the θ output goes to V- and $\overline{\theta}$ goes to V+; thus θ and $\overline{\theta}$ are 180^o out of phase with each other. These complementary outputs can be used to create a wide variety of functions such as SPDT and DPDT switches, etc.; alternatively the complementary outputs can be used to drive N and P channel MOSFETs, to make a complete CMOS analog gate.

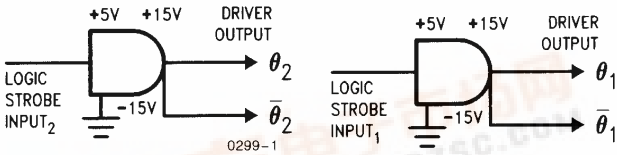
The driver typically uses +5V and ±15V power supplies, however a wide range of V+ and V- is also possible. It is necessary that V+ > 5V for the driver to work properly, however.

Pinout

IH6201
(OUTLINE DWGS, JE, PE)
TOP VIEW



Functional Diagram



Absolute Maximum Ratings

Supply Voltage (V+ to V-) 35V
V+ 35V
V- 35V
V+ to V_{IN} 40V

Thermal Information

Storage Temperature Range . . . . . -65^oC to 150^oC
Lead Temperature (Soldering, 10s) . . . . . 300^oC

Operating Conditions

Temperature Range . . . . . -55^oC to 125^oC

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Electrical Specifications V+ = +15V, V- = -15V, V_L = +5V

PARAMETER	TEST CONDITIONS	IH6201CJE, CPE			IH6201MJE			UNITS
		0^oC	25^oC	70^oC	-55^oC	25^oC	125^oC	
θ or $\overline{\theta}$ Driver Output Swing	V_{IN} = 0V ⎍ + 3V, Figure 3B	-	28	-	-	28	-	V_{P-P}
V_{IN} Strobe Level ("1") for Proper Translation	$\theta \geq 14V$, $\overline{\theta} \geq -14V$	3.0	3.0	3.0	-	2.4	-	V_{DC}
V_{IN} Strobe Level ("0") for Proper Translation	$\theta \geq -14V$, $\overline{\theta} \geq 14V$	0.4	0.4	0.4	-	0.8	-	V_{DC}
I_{IN} Input Strobe Current Draw (for 0V - 5V Range)	V_{IN} = 0V or +5V	±1	±1	10	±1	±1	10	µA
t_{ON} Time	V_{IN} = 0V ⎍ C_L = 30pF Switching Turn-on Time, Figure 3B	-	500	-	-	500	-	ns
t_{OFF} Time	V_{IN} = 0V ⎍ C_L = 30pF Switching Turn-off Time, Figure 3B	-	500	-	-	500	-	ns
I+ (V+) Power Supply Quiescent Current	V_{IN} = 0V or +5V	100	100	100	100	100	100	µA
I- (V-) Power Supply Quiescent Current	V_{IN} = 0V or +5V	100	100	100	100	100	100	µA
I_L (V_L) Power Supply Quiescent Current	V_{IN} = 0V or +5V	100	100	100	100	100	100	µA

Schematic Diagram

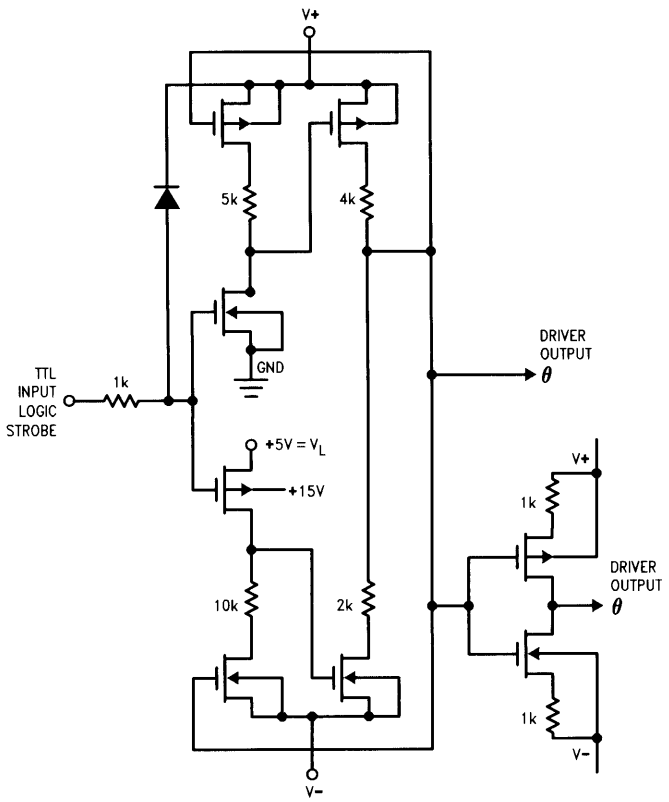


FIGURE 1. SCHEMATIC DIAGRAM (ONE CHANNEL)

Applications

Input Drive Capability

The strobe input lines are designed to be driven from TTL logic levels; this means 0.8V to 2.4V levels max. and min. respectively. For those users who require 0.8V to 2.0V operation, a pull-up resistor is recommended from the TTL output to +5V line. This resister is not critical and can be in the 1kΩ to 10kΩ range.

When using 4000 series CMOS logic, the input strobe is connected direct to the 4000 series gate output and no pull up resistors, or any other interface is necessary.

When the input strobe voltage level goes below GND (i.e. to -15V) the circuit is unaffected as long as V+ to V_{IN} does not exceed absolute maximum rating.

Output Drive Capability

The translator output is designed to drive the IH401A Varafets; these are N-channel JFETS with built-in driver diodes. Driver diodes are necessary to isolate the signal source from the driver/translator output; this prevents a forward bias condition between the signal input and the $+V_{CC}$ supply. The IH6201 will drive any JFET provided some sort of isolation is added.

You will notice in Figure 2 that a “referral” resistor has been added from 2N4391 gate to its source. This resistor is needed to compensate for the inadequate charge area curve for isolation diode i.e. if C vs. V plot for diode ≤ 2 [C vs. V plot for output JFET] switch won’t function; then adding this resistor overcomes this condition. The “referral” resistor is normally in the 100kΩ to 1MΩ range and is not tool critical.

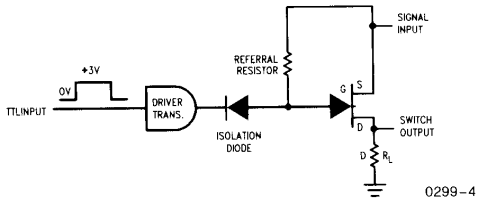


FIGURE 2.

Making a Complete Solid State Switch that Can Handle $20V_{P-P}$ Signals

The limitation on signal handling capability comes from the output gating device. When a JFET is used, the pinch-off of the JFET acting with the V- supply does the limiting. In fact max. signal handling capability = 2 (V_P + (V-)) V_{P-P} where V_P = pinch-off voltage of JFET chosen. i.e. V_P = 7V, V- = -15V: max. signal handling = 2(7V + (-15V)) V_{P-P} = 2 (7V - 15) V_{P-P} = 2(-8V_{P-P}) = 16V_{P-P}. Obviously to get ≥ 20V_{P-P}, V_P ≥ 5V with V- = -15V. Another simple way to get 20V_{P-P} with V_P = 7V, is to increase V- to -17V. In fact using V+ = +12V or +15V and setting V- = -18V allows one to switch 20V_{P-P} with the IH401A. The advantage of using the V_P = 7V pinch-off (along with unsymmetrical supplies), over the V_P = 5V pinch-off (and

±15V supplies), is that you will have a much lower $R_{DS(ON)}$ for the V_P = 7 JFET (i.e. for the 2N4391).

$r_{DS(ON)} \approx 22\Omega$, $R_{DS(ON)} \approx 35\Omega$

$V_P = 7V$ $V_P = 5V$

The IH6201 is a dual translator, each containing 4 CMOS FET pairs. The schematic of one-half of an IH6201, driving one-quarter of an IH401A, is shown in Figure 3A.

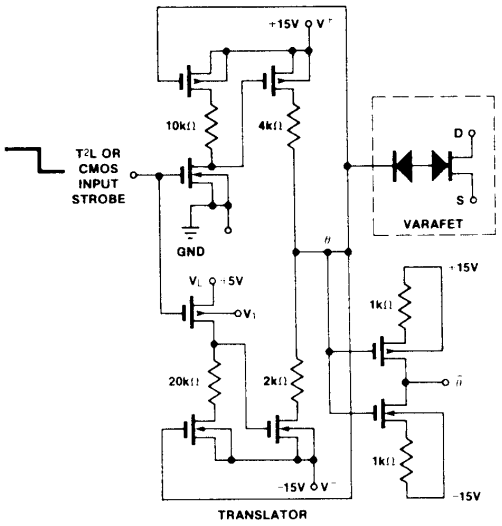


FIGURE 3A.

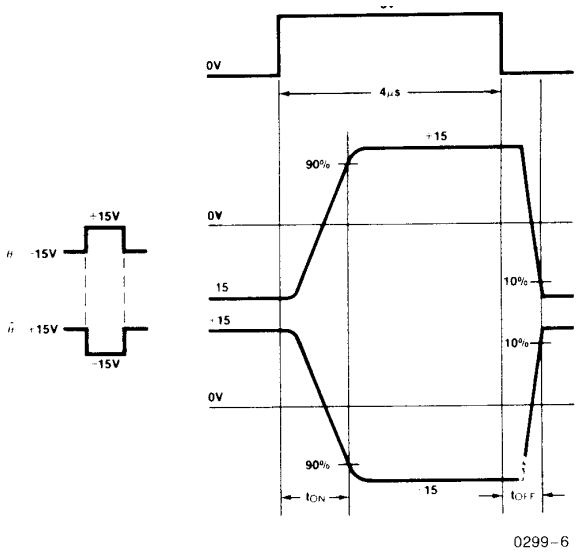


FIGURE 3B.

NOTE: Each translator output has a θ and $\bar{\theta}$ output, θ is just the inverse of $\bar{\theta}$.

A very useful feature of this system is that one-half of an IH6201 and one-half of an IH401A can combine to make a SPDT switch, or an IH6201 plus an IH401A can make a dual SPDT analog switch (See Figure 6).

Switches

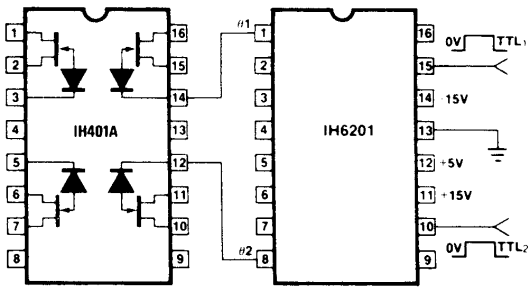


FIGURE 4. DUAL SPST ANALOG SWITCH

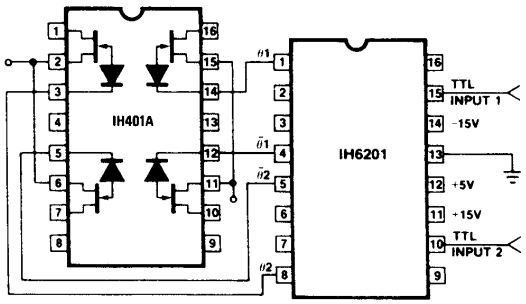


FIGURE 5. DPDT ANALOG SWITCH

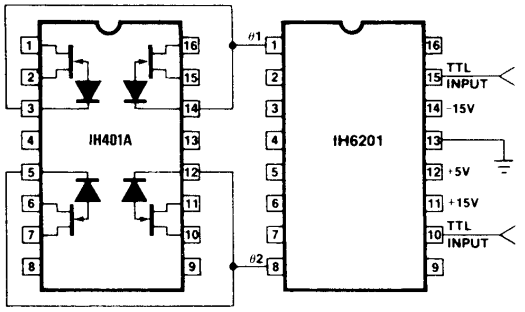


FIGURE 6. DUAL SPDT

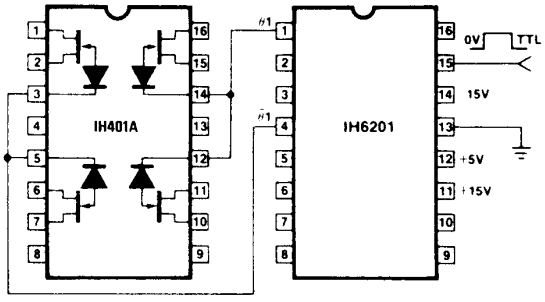


FIGURE 7. DUAL DPST